Compact modeling of advanced bulk CMOS using EKV3 – linearity, RF and noise performance trends

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Outline

• Physics-based, charge-based compact MOSFET model – EKV3 model
• DC to RF modeling
• IV, CV, Y-parameters
• Linearity
• RF figures of merit – evolution with technology
• Thermal noise
• Conclusions
EKV3 scalable model for high frequency

- Scalability vs. channel length, number of fingers, bias
  - Gate- and substrate- parasitics scale with multi-finger layout
  - Layout-dependent stress effects
- Non quasi-static model (NQS)
  - channel segmentation
  - consistent AC/transient
- Thermal noise
  - Induced gate & substrate noise
  - Velocity saturation, CLM
  - Carrier heating
EKV3 configurations, channel-segmentation for NQS

- Simple model – only internal accounting for (S,D) series resistance
- Simple model with external series resistance
- Simple RF model with gate and substrate resistance
- Full RF model with substrate resistivity network
- Full RF & NQS (channel segmentation) model.
Channel-segmentation for NQS effects

Multifinger device NMOS Lg = 2 um, saturation (110 nm CMOS)

--- QS and —— NQS EKV3 model, 45 MHz - 20 GHz
Layout-dependent parasitics

\[ R_G = R_{G_{top}} + R_{G_{ext}} + R_{G_{via}} + R_{G_{con}} \]

\[ R_G = \begin{cases} \frac{1}{4} \cdot \frac{W_F}{N_F L_F} R_{G_{[,]}} & \text{two - sided} \\ \frac{1}{3} \cdot \frac{W_F}{N_F L_F} R_{G_{[,]}} & \text{one - sided} \end{cases} \]
Multi-finger RF MOSFETs

- Layout of RF multi-finger MOSFET
  - Number of fingers – $N_F$
  - Finger Width – $W_f$
  - Gate Length – $L$

- Ground-Signal-Ground (GSG) RF Pads
  - 2 port configuration
- Open-Short de-embedding structures
Layout dependence: STI stress in multi-finger RF MOSFETs

- NMOS, L=180nm, W_f=2μm
- Stress effects due to shallow-trench isolation (STI)
  - Threshold voltage $V_T$ vs. $N_F$
  - Max. drain current $I_D / N_F$ vs. $N_F$

$V_{DS} = 50m, 0.5, 1V$

- EKV3 □ meas.
Edge conduction effect

- Edge conduction effect dominant in Weak – Moderate Inversion
- Leakage dramatically increased
- $G_m/I_D$ is strongly affected – MI
- EKV3 only available CM to cover this effect
- $L=2\text{um}$, $W=3\text{um}$ and $V_{DS}=1.2\text{V}$
Static characteristics NMOS – EKV3 model

- NMOS, L=180nm, W_f=2μm, N_F=4
- I_D-V_G, g_m-V_G, g_m*U_T/I_D – I_D
- I_D-V_D, g_ds-V_D
Static characteristics PMOS – EKV3 model

- PMOS, L=180nm, W_f=2µm, N_F=4
- I_D-V_G, g_m-V_G, g_m-U_T/I_D – I_D
- I_D-V_D, g_{ds}-V_D

- V_{DS}=50m, 0.5, 1V
- V_{GS}=0.4, 0.6, 0.8, 1, 1.2V

- EKV3 □ meas.
I-V NMOS; \( W_F = 2\mu m; L_F = 65\text{nm}; N_F = 40 \)

**\( I_D, g_m \text{ vs. } V_G \) (saturation)**

**\( I_D, g_m \text{ vs. } V_G \) (linear)**

**\( I_D, g_{ds} \text{ vs. } V_D \)**

Measurements / EKV3 / BSIM4

WMF: Physics-Based NL CM for mm-Wave Applications
I-V PMOS: $W_F = 2\mu m$; $L_F = 65\text{nm}$; $N_F = 40$

**$I_D, g_m$ vs. $V_G$**

(saturation)

**$I_D, g_m$ vs. $V_G$**

(linear)

**$I_D, g_{ds}$ vs. $V_D$**

$g_m/I_D$ vs. $I_D$

Measurements / EKV3
Capacitance-voltage characteristics, EKV3 model

- Long/short (L=10um, 90nm) gate and inversion capacitance, NMOS, PMOS.

M. Bucher e.a. Int. J. RF and Microwave CAE, 2008
Approximate Y-Parameters

• Assuming $\omega R_g C_{gg} \ll 1$

$$Y_{11} \approx \omega^2 R_g C_{gg}^2 + j \omega C_{gg}$$
$$Y_{12} \approx -\omega^2 R_g C_{gg} C_{gd} - j \omega C_{gd}$$
$$Y_{21} \approx g_m - \omega^2 R_g C_{gg} \left(C_m + C_{gd}\right) - j \omega \left(C_m + C_{gd}\right)$$
$$Y_{22} \approx g_{ds} + \omega^2 R_g C_{gg} \left(C_{bd} + C_{gd}\right) + j \omega \left(C_{bd} + C_{gd}\right)$$

$$C_{gg} \equiv C_{gs} + C_{gd} + C_{gb}$$

• Can be used for direct extraction
Y-parameters vs. frequency – NMOS

- Real & Imaginary 2-port Y-parameters up to 30GHz
- NMOS, $L=180\text{nm}$, $W_{f}=2\mu\text{m}$, $N_{F}=9$

$V_{DS}=0.3$, $V_{GS}=0.3, 0.6, 1.2V$

EKV3
□ meas.

Y parameters vs. frequency – PMOS

- Real & Imaginary 2-port Y-parameters up to 30GHz
- \( L=180\,\text{nm}, \, W_f=2\,\mu\text{m}, \, N_F=9 \)

\[ V_{DS}=-1.2\,\text{V}, \, -V_{GS}=0.3, \, 0.6, \, 1.2\,\text{V} \]

Scalability with channel length – NMOS

- Y parameters for NMOS
  - L=110 nm, 180 nm, 250 nm, 450 nm, 1 um, 2 um
  - W=5 um, NF=10
  - VG=0.6V, VD=0.5V

M. Bucher e.a. Int. J. RF and Microwave CAE, 2008
Scalability with channel length – PMOS

- **Y parameters for PMOS**
  - $L = 110\, \text{nm}, 180\, \text{nm}, 250\, \text{nm}, 450\, \text{nm}, 1\, \text{um}, 2\, \text{um}$
  - $W = 5\, \text{um}, NF = 10$
  - $VG = 0.6\, \text{V}, VD = 0.5\, \text{V}$

M. Bucher e.a. Int. J. RF and Microwave CAE, 2008
Y-parameters NMOS; \( W_F = 2\mu m; \ L_F = 65\text{nm}; \ N_F = 40 \)

\[ V_{GS} = 0.8V; \ V_{DS} = \{0.4, 0.6, 0.8\}V; \ V_{SB} = 0V \]

\[
\begin{align*}
Y_{11} & \quad Y_{12} & \quad Y_{21} & \quad Y_{22} \\
\text{(Real)} & \quad \text{(Imaginary)} & \quad \text{(Real)} & \quad \text{(Imaginary)}
\end{align*}
\]

Measurements / EKV3 / BSIM4
Y-parameters PMOS, $W_F = 2\mu m$, $L_F = 65\text{nm}$; $N_F = 40$

$|V_{GS}| = 0.8V; |V_{DS}| = \{0.4, 0.6, 0.8\}V; V_{SB} = 0V$

Measurements / EKV3
Linearity – small signal

Measured ($W = 40 \times 2\, \mu m, \, V_{DS} = 1\, V, \, \Omega f = 1.1\, GHz$)

- $G_m$, $G_{m2}$, $G_{m3}$, $P_{IP3}$, $V_{IP3}$ vs. $I_D/I_{spec}$
- “Sweet Spot” is moving to lower levels of inversion with lower $L$!
Linearity – small signal

TCAD ($W = 10 \times 2 \mu m$, $V_{DS} = 0.9 V$)

Evolution of $P_{1dB}$, $P_{IP3}$, vs. $I_D/I_{spec}$ for technology nodes to 22nm

- “Sweet Spot” is moving to lower levels of inversion with lower $L$!
- Good news: better linearity closer to $V_T$. 
Linearity – large signal (load-pull)

\[ V_{GS} = 0.8 \text{ V}, \quad V_{DS} = 0.8 \text{ V}, \quad V, \quad V_{SB} = 0, \quad V_{P_{in}} = 5 \text{ dBm} \]

\[ P_{out} & \text{ Contours} \]

\[ Z_L = 50 \text{ Ohm}, \quad P_{in} = -20\ldots5 \text{ dBm} \]

\[ \text{NMOS: } L = 65\text{nm}, \quad W = 2\text{um}, \quad NF = 10, \quad \text{Freq} = 5.8\text{GHz} \]
General RF parameters

- **Unity gain frequency** ($f_T$)
  - Frequency where current gain of a CS amplifier falls to unity
  
  $$f_T = \frac{f_{\text{spot}}}{\text{Imag}(\frac{Y_{11}}{Y_{21}})}$$

  - Can be extrapolated from $h_{21}$ in S.I., saturation, where the slope is $-20 \text{dB/dec}$

- **Maximum oscillation frequency** ($f_{\text{max}}$)
  - Calculated through unilateral gain
  - Maximum available gain assuming neutralized device

  $$U = \frac{|Y_{21} - Y_{12}|^2}{4[\text{real}(Y_{11}) \text{Real}(Y_{22}) - \text{real}(Y_{12}) \text{Real}(Y_{21})]}$$

  $$f_{\text{max}} = \sqrt{U} f_{\text{spot}}$$

  - Can be extrapolated from $U$, in S.I., saturation

- **Transconductance efficiency** ($G_m/I_D$)

  $$\frac{G_m U_T}{I_D} = \frac{2}{n(\sqrt{4kT} + 1)}$$

  - Maximum in W.I.
High-frequency parameters @5GHz vs. $I_D$ – NMOS

- $|H_{21}|$, $U$, $F_T$, $F_{\text{max}}$, $\text{Re}(Y_{21})$, $\text{Re}(Y_{22})$ vs. $I_D$
- $L=180\text{nm}$, $W_f=2\mu\text{m}$, $N_F=9$

$V_{DS}=0.5, 1.2, 1.3\text{V}$

High-frequency parameters @5GHz vs. $I_D$ – PMOS

- $|H_{21}|$, U, $F_T$, $F_{\text{max}}$, $\text{Re}(Y_{21})$, $\text{Re}(Y_{22})$ vs. $I_D$
- $L=180\text{nm}$, $W_f=2\mu\text{m}$, $N_F=9$

$-V_{DS}=0.5, 1.2, 1.3\text{V}$

- EKV3 □ meas.
High-frequency parameters NMOS vs. $V_G$

\[ U = \frac{|H_{21} - H_{12}|^2}{4 \cdot \text{re}(H_{11}) \cdot \text{re}(H_{22}) - \text{re}(H_{12}) \cdot \text{re}(H_{21})} \]

Unilateral Gain vs. $V_G$

- $R_G = 30 \, \Omega$
- $C_{GD} = 7.5 \, \text{fF}$
- $C_{GS} = 7.5 \, \text{fF}$
- $R_B = 103 \, \Omega$
- $C_{JD} = 11 \, \text{fF}$

MSG vs. $V_G$

\[ \text{MSG} = \left| \frac{S_{21}}{S_{12}} \right| \]

$f_{\text{max}}$ vs. $V_G$

\[ f_{\text{max}} = U(f) \cdot f \]

$f_T$ vs. $V_G$

\[ f_T = \frac{f}{\text{Im} \left( \frac{Y_{11}}{Y_{21}} \right)} \]

NMOS: $L = 65\,\text{nm}$, $W = 2\,\mu\text{m}$, $NF = 10$, $F = 5\,\text{GHz}$, $V_{GS} = [0.2, \ldots, 1.2] \, \text{V}$, $V_{DS} = [0.2, \ldots, 1.2] \, \text{V}$
High-frequency parameters NMOS vs. $V_G$

NMOS: $L = 65\text{nm}$, $W = 2\text{um}$, $NF = 10$, $F = 5 \text{GHz}$, $V_{GS} = [0.2, \ldots, 1.2] \text{V}$, $V_{DS} = [0.2, \ldots, 1.2] \text{V}$
$F_T$ and $F_{max}$ evolution with technology

TCAD and measured ($W = 10 \times 2 \, \mu m$, $V_{DS} = 0.9 \, V$)
\( \frac{G_M}{I_D \cdot F_T}, \quad \frac{G_M^2}{I_D} \quad \text{and} \quad \left[ \frac{G_M}{G_{DS} \cdot \frac{G_M}{I_D} F_T} \right] \)

The different FoMs behave in a similar way:

Maximum in moderate inversion!

Trend towards lower levels (within moderate inversion)
$G_M/I_D \cdot F_T$ and $[G_M/G_{DS} \cdot G_M/I_D \cdot F_T]$ evolution

- TCAD and measured ($W = 10 \times 2 \, \mu m$, $V_{DS} = 0.9 \, V$)
Thermal noise in MOSTs – EKV3 model

Velocity Saturation (VS) and Carrier Heating (CH)

- Electrons and holes have a characteristic $E_c$ and $u_{car}$
- When $E_x$ becomes comparable to $E_c$ then $u_{drift}$ starts to saturate
- High lateral electric field
  - Carriers gain higher energy
  - Random collisions w. lattice
  - Carrier temperature increases w. electric field
- VS and CH, interdependent phenomena
- EKV3 accounts for both
  - Critical field parameter
  - $\lambda_c = \frac{2UT}{L_{eff} E_c}$
  - The higher the $\lambda_c$, the stronger the SCB

Channel Length Modulation (CLM)

- In S.I. as $V_{DS}$ increases the channel pinches off
- Channel is split into two regions
  - Non-saturated region ($L_{eff}$)
  - VS region, $\Delta L$
- Carriers in VS region
  - Maximum velocity
  - Noise voltage fluctuations do not propagate to drain
- Only the active region contributes to channel thermal noise
Thermal noise in MOSTs – EKV3 model

Thermal noise due to local random fluctuations of the carrier velocity
- Transferred to the device terminals
- Modeled as a random current added to the DC local current

Modeling approach
- Local noisy source
- $x$ and $x+\Delta x$ from Source
- $L-x$ and $L-(x+\Delta x)$ from Drain
- Noisy current source in parallel with $\Delta R$
- Transistor is split into T1 and T2
- Channel conductance: $\frac{1}{G_{ch}} = \frac{1}{G_1} + \frac{1}{G_2}$
- Drain fluctuation due to local noise source: $\delta I_{nD} = G_{ch} \Delta R \delta I_n$
- PSD of drain current due to all noisy sources:

$$S_{\Delta I_{nD}^2}(\omega) = \int_0^L G_{ch}^2 \Delta R^2 \frac{S_{\delta I_n^2}(\omega,x)}{\Delta x} \, dx$$
Short channel effects on thermal noise – EKV3 model

- Incorporating SCE in PSD of drain noise current (Roy and Enz, TED 2005)
  - S.I. assumption (SCE dominant)
  - Two transistor approach
  - Effective mobility $\mu_{\text{eff}}$ varies w. $E_X$

- Thermal noise conductance
  $$G_{nD} = M \frac{W}{L_{\text{eff}}} \int_0^{L_{\text{eff}}} \mu_z \frac{T_C}{T_L} (-Q_i(x)) \, dx$$
  $$L_{\text{eff}} = \begin{cases} 
  L, & \text{for } V_D < V_{D\text{sat}} \\
  L - \Delta L, & \text{for } V_D \geq V_{D\text{sat}}
  \end{cases}$$
  $$V_{D\text{eff}} = \begin{cases} 
  V_D, & \text{for } V_D < V_{D\text{sat}} \\
  V_{D\text{sat}}, & \text{for } V_D \geq V_{D\text{sat}}
  \end{cases}$$
  $$M = \frac{1}{(1 - \frac{V_{D\text{eff}} - V_S}{2L_{\text{eff}}E_C})^2}$$
  - Analytical expression
Thermal noise parameters

- Thermal noise parameter: $\delta = \frac{G_{nD}}{G_{ds0}}$
  - $G_{nD}$ and $G_{ds0}$ calculated at different operating points
  - Less relevant for circuit design

- Thermal noise excess factor: $\gamma = \frac{G_{nD}}{G_m}$
  - $G_{nD}$ and $G_m$ calculated at the same operating points
  - Characterizes noise performance of transconductors
  - Used in noise calculation of cascode LNA: $F_{min} = 1 + 2\gamma \frac{w}{\omega_T} \sqrt{\frac{\beta C}{T}} (1-c)^2$
  - The smaller $\gamma$, the better the noise performance
  - Dramatically increases in linear operation

Importance of $\gamma$ underestimated by scientific community
- Not validated w. measurements
- $\delta$ instead of $\gamma$
Noise in 2-port devices

- Noise generated by any two-port device
  - Noiseless network w. two partially correlated noise sources
  - 4 noise parameters

\[
F = F_{min} + \frac{R_n}{G_z} | Y_s - Y_{opt} |^2
\]

- Minimum noise figure, $F_{min}$
- Noise resistance, $R_n$
- Optimum source reflection coefficient, $\Gamma_{opt}$
- $Y_{opt} = Y_0 \frac{1-\Gamma_{opt}}{1+\Gamma_{opt}}$

- Noise matching when
  - $G_S = G_{opt}$ and $B_S = B_{opt}$
Noise parameters vs. frequency – EKV3 model

NMOS ($L = 100\, \text{nm}$, $W = 40 \times 2\, \text{um}$, $V_{GS} = 0.65\, \text{V}$, $V_{DS} = 1.2\, \text{V}$)

NMOS ($L = 240\, \text{nm}$, $W = 40 \times 2\, \text{um}$, $V_{GS} = 0.65\, \text{V}$, $V_{DS} = 1.2\, \text{V}$)
Noise parameters vs. bias – EKV3 model

NMOS ($W = 40 \times 2\mu m$, $V_{DS} = 1.2\,V$, $f = 10\,GHz$)

Antonopoulos et al., RFIC Symp. 2013
Thermal noise vs. bias & channel length – EKV3 model

NMOS (W = 40x2μm, V_DS = 1.2V, f = 10GHz)

Antonopoulos et al., TED 2013
Induced gate noise – EKV3 model

NMOS ($W = 40 \times 2 \mu m$, $V_{DS} = 1.2 V$)

Correlation factor: $c = \frac{S_{igt}}{\sqrt{S_{ig} S_{itd}}}$

$S_{ig}$ vs. Frequency (GHz)

$S_{ig}$ vs. $V_{GS}$ (V)

$\text{Imag}(c)$ vs. Frequency (GHz)

Antonopoulos et al., TED 2013
Thermal noise parameters – EKV3 model

NMOS ($W = 40 \times 2\mu m$, $V_{DS} = 1.2\,V$, $f = 10\,GHz$)

Antonopoulos et al., TED 2013
Conclusions

• EKV3: analog/RF IC design-oriented, charge-based, compact model

• Model covers all aspects from DC to RF
  – Fully scalable with L, W, NF, bias, f, technology
  – Small/large signal including NQS
  – Noise
  – Simple model structure & parameter extraction

• RF model validations
  – Vs. measurements in 180 – 110 – 90 – 65 nm CMOS.
  – Vs. TCAD to 22nm CMOS.
  – Implementations in: Spectre, ELDO, Smash, HSPICE (underway)
Conclusions

• Relation to advanced analog/RF IC design
  – Trend towards moderate inversion: optimum $G_m/I_D$, $F_T$, best noise/gain/linearity performance

• Optimal RF CMOS (for LV-LP RFIC) performance shifted to lower levels of inversion (near-threshold) with CMOS technology approaching 22nm.

• EKV3 model incorporates all necessary short-channel effects for correct RF Noise at mm-waves.
EKV3 publications

EKV3 model, RFCMOS papers
EKV3 publications

EKV3 model, general papers


Thank you for your attention

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