ANGELOS ANTONOPOULOS

Date of Birth: May 31, 1981 ◇ Nationality: Greek
Address: Marathonodromou 103, Marousi, 15125, Greece
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RESEARCH INTERESTS

- Security and trustworthiness of analog/RF integrated circuits and systems
- Machine learning-based test and calibration of analog/RF integrated circuits
- Design oriented compact modeling of advanced CMOS technologies
- Low power analog/RF integrated circuits design

EDUCATION

Ph.D. *February 2014*
School of Electronics & Computer Engineering, Technical University of Crete
PhD Thesis: *Nanoscale RF CMOS Transceiver Design*
Advisor: Prof. Matthias Bucher

MSc. *May 2008*
School of Electronics & Computer Engineering, Technical University of Crete
MSc Thesis: *System Level Analysis of a Direct Conversion WiMAX Receiver at 5.3GHz and Corresponding Mixer Design*
Advisor: Prof. Matthias Bucher

Engineering Diploma (5-year program) *September 2005*
School of Electronics & Computer Engineering, Technical University of Crete

PROFESSIONAL EXPERIENCE

Patent Engineer January 2018 - present
u-blox Athens S.A. *Voreiou Ipeirou 74, Marousi, 15125, Greece*

- Identifying new opportunities and/or directions for patenting with R&D
- Conducting novelty searches and establishing patentability of patent proposals
- Coordinating efforts of patent attorneys to assure drafted patent specifications meet requirements and are timely filed
- Supporting and guiding the prosecution of u-blox's patent filings by providing technical and strategic input
- Undertaking "Freedom-to-Operate" investigations in conjunction with project management to ensure conflicts are avoided

Postdoctoral Research Associate April 2015 - January 2018
University of Texas at Dallas *Richardson, TX*

- Conducting research in the area of *Trusted and Reliable Analog/RF Integrated Circuits and Systems*
- Co-supervising 5 PhD candidates
- Writing NSF and AFRL research proposals

Researcher September 2010 - March 2015
Telecommunications Systems Institute *Chania, Greece*

- `R&D Project Dedicated RF Model for 55nm CMOS:` DC, CV and RF characterization and modeling of a 55nm RF CMOS process for weasic Microelectronics SA. Evaluation of BSIM6 model and comparison with the delivered EKV3 model
- `R&D Project EKV3.0 and EKV2.6 MOST modeling in ALP018D:` EM 0.18μm CMOS process with embedded FLASH: Measurements, characterization and modeling of a 0.18μm CMOS process for EM Microelectronic SA with EKV2.6 and EKV3 models
- `R&D Project EKV3.0 modeling in ALP018B: EM 0.18`μ`m logic CMOS process:` Measurements, characterization and modeling of a 0.18μm CMOS process for EM Microelectronic SA with EKV3 model
- `R&D Project Multigate MOSFET nanotransistors:` Compact models for current and noise. Development of automated design tools for nanoelectronics
- `R&D Project Next Generation Millimeter Wave Backhaul Radio:` Tapeout of a test chip including a 30GHz LNA as well as DC, CV and RF MOS devices with different geometrical characteristics. Measurements, characterization and modeling of the test chip with the EKV3 model
- `R&D Project ALP018B LV and MV MOST modeling:` EM 0.18μm logic CMOS process: Measurements, characterization and modeling of a 0.18μm CMOS process for EM Microelectronic SA with EKV2.6 and EKV3 models

Teaching Assistant March 2007 - January 2014
Technical University of Crete *Chania, Greece*

- Teaching exercises and laboratories in undergraduate courses including: Electronics II, Analog CMOS Design, Digital Computers, Digital Logic Design

Special Scientist March 2013 - December 2014
Greek Army (Mandatory Service) *Chania, Greece*

- Software and hardware engineer. Responsible for servers maintenance and data base development

AWARDS

- Best Hardware Demo Award: *"Performance Randomization for Preventing Hardware Trojan Attacks in Analog/RF Circuits"*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2018

SCHOLARSHIPS

- Heracleitus II program co-financed by the European Social Fund (ESF) and Greek national funds, through the operational program "Education and Lifelong Learning", within the National Strategic Reference Framework (NSRF)

PUBLICATIONS

Book Chapters

B1. S. Bhunia and M. Tehranipoor (Editors), The Hardware Trojan War: Attacks, Myths, and Defenses, Springer, 2018 (**A. Antonopoulos**, C. Kapatsori, Y. Makris, *"Hardware Trojans in Analog, Mixed-Signal and RF ICs,"*) (invited)

Journals

J1. K. Subramani **A. Antonopoulos**, A. Abotabl, A. Nosratinia, Y. Makris, *"Demonstrating and Mitigating the Risk of a FEC-based Hardware Trojan in Wireless Networks,"* IEEE Transactions on Information Forensics and Security, accepted

J2. M. Bidmeshki, **A. Antonopoulos**, Y. Makris, *"Proof-Carrying Hardware-based Information Flow Tracking in Analog/Mixed-Signal Designs,"* IEEE Transactions on Very Large Scale Integration (VLSI) Systems, submitted

J3. **A. Antonopoulos**, C. Kapatsori, Y. Makris, *"Trusted Analog/Mixed-Signal/RF ICs: A Survey and a Perspective,"* IEEE Design and Test, vol. 34, no. 6, pp. 63-76, December 2017

J4. G. Volanis, **A. Antonopoulos**, A. Hatzopoulos, Y. Makris, *"Towards Silicon-Based Neuoromorphic ICs - A Survey,"* IEEE Design and Test, Vol. 33, No. 3, pp. 91-102, May 2016

J5. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Makris, N. Mavredakis, R. K. Sharma, P. Sakalas, M. Schroter, *"Modeling of High Frequency Noise of Silicon MOS Transistors for RFIC Design,"* International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, special issue on Modeling of high-frequency silicon transistors, Vol. 27, No. 5-6, pp. 802-811, September 2014

J6. W. Grabinski, M. Brinson, P. Nenzi, F. Lannutti, N. Makris, **A. Antonopoulos**, M. Bucher, *"Open source circuit simulation tools for RF compact semiconductor device modelling,"* International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, special issue on Modeling of highfrequency silicon transistors, Vol. 27, No. 5-6, pp. 761-779, September 2014

J7. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Mavredakis, N. Makris, R. K. Sharma, P. Sakalas, M. Schroter, *"CMOS Small-Signal and Thermal Noise Modeling at High Frequencies,"* IEEE Trans. Electron Devices, Vol. 60, No. 11, pp. 3726-3733, November 2013

Conferences

C1. G. Volanis, Y. Lu, S. Nimmalapudi, **A. Antonopoulos**, A. Marshall, Y. Makris, *"Analog Performance Locking through Neural Network-Based Biasing,"*, IEEE VLSI Test Symposium (VTS), 2019, accepted

C2. C. Kapatsori, Y. Liu, **A. Antonopoulos**, Y. Makris, *"Hardware Dithering: A Run-Time Method for Trojan Neutralization in Wireless Cryptographic ICs,"* IEEE International Test Conference (ITC), pp. 1-7, 2018

C3. K. Subramani, **A. Antonopoulos**, A. Abotabl, A. Nosratinia, Y. Makris, *"ACE: Adaptive Channel Estimation for Detecting Analog/RF Trojans in WLAN Transceivers,"* IEEE International Conference On Computer Aided Design (ICCAD), pp. 722-727, 2017

C4. **A. Antonopoulos**, C. Kapatsori, Y. Makris, *"Security and Trust in the Analog/Mixed-Signal/RF Domain: A Survey and a Perspective,"* IEEE European Test Symposium (ETS), pp. 1-10, 2017

C5. K. Subramani, **A. Antonopoulos**, A. Abotabl, A. Nosratinia, Y. Makris, *"INFECT: INcospicuous FEC-based Trojan: a Hardware Attack on an 802.11a/g Wireless Network,"* IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 90-94, 2017

C6. Y. Lu, G. Volanis, K. S. Subramani, **A. Antonopoulos**, Y. Makris, *"Knob Non-Idealities in Learning-Based Post-Production Tuning of Analog/RF ICs: Impact & Remedies,"*IEEE VLSI Test Symposium (VTS), pp. 1-6, 2017

C7. M. Bidmeshki, **A. Antonopoulos**, Y. Makris, *"Information Flow Tracking in Analog/Mixed-Signal Designs through Proof-Carrying Hardware IP,"* IEEE Design Automation and Test in Europe Conference (DATE), pp. 1703-1708, 2017

C8. G. Volanis, D. Maliuk, Y. Lu, K. S. Subramani, **A. Antonopoulos**, Y. Makris, *"On-Die Learning-Based Self-Calibration of Analog/RF ICs,"* IEEE VLSI Test Symposium (VTS), pp. 1-6, 2016

C9. K. Papathanasiou, N. Makris, **A. Antonopoulos**, M. Bucher, *"Moderate inversion: analog and RF benchmarking of the EKV3 compact model,"* International Conference on Microelectronics (MIEL), pp. 205-208, 2014

C10. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Makris, R. K. Sharma, P. Sakalas, M. Schroter, *"CMOS RF Noise, Scaling, and Compact Modeling for RFIC Design,"* IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 53-56, 2013

C11. R.K Sharma, **A. Antonopoulos**, N. Mavredakis, M. Bucher, *"Impact of Design Engineering on RF Linearity and Noise Performance of Nanoscale DG SOI MOSFETs,"* International Conference on Ultimate Integration on Silicon (ULIS), pp. 145-148, 2013

C12. **A. Antonopoulos**, K. Papathanasiou, M. Bucher, K. Papathanasiou, *"CMOS LNA Design at 30 GHz - A Case Study,"* International Caribbean Conference on Devices Circuits and Systems (ICCDCS), pp.1-4, 2012

C13. R. K. Sharma, **A. Antonopoulos**, N. Mavredakis, M. Bucher, *"Analog/RF Figures of Merit of Advanced DG MOSFETs,"* International Caribbean Conference on Devices Circuits and Systems (ICCDCS), pp.1-4, 2012

C14. N. Mavredakis, **A. Antonopoulos**, M. Bucher, *"Measurement and Modelling of 1/f Noise in NMOS and PMOS Devices,"* European Conference on Circuits and Systems for Communications (ECCSC), pp.86-89, 2010

C15. N. Mavredakis, **A. Antonopoulos**, M. Bucher, *"Bias Dependence of Low Frequency Noise in 90nm CMOS,"* Workshop on Compact Modeling, Micro-Nanotech, pp. 805-808, 2010

C16. **A. Antonopoulos**, N. Mavredakis, N. Makris, M. Bucher, *"System Level Analysis of a Direct Conversion WiMAX Receiver at 5.3 GHz and Corresponding Mixer Design,"* International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 291-296, 2008

Workshops

W1. K. S. Subramani, **A. Antonopoulos**, A. Nosratinia, Y. Makris, *"Hardware-Induced Security and Privacy Vulnerabilities in the Internet of Things,"* IEEE End to End Trust and Security Workshop for the Internet of Things, Washington DC, 2016

W2. M. Bucher, **A. Antonopoulos**, *"Compact modeling of advanced bulk CMOS using EKV3-linearity, RF and noise performance trends,"* Physics-based nonlinear compact transistor modeling for mm-wave applications Workshop, International Microwave Symposium (IMS), Florida, 2014

W3. M. Bucher, **A. Antonopoulos**, *"Compact modelling of RF small-signal and noise performance with EKV3 MOS transistor model,"* Modeling of Systems and Parameter Extraction Working Group (MOS-AK) Workshop, London, 2014

TECHNICAL SKILLS

IC design	Amplifiers, mixers, oscillators, LNAs, current mirrors, voltage references
Measurements	On Wafer (Cascade Prober) DC (HP4142 , HP4145) and RF (HP 8510C)
Tools	Cadence Virtuoso, ADS, ICCAP, Dolphin Smash, Matlab
Software	Linux, Administration duties for Cadence and Agilent products

PROFESSIONAL ACTIVITIES

Memberships

· Institute of Electrical and Electronic Engineering (IEEE), Member

Reviewer for

· IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
· IEEE Transactions on Circuits and Systems I: Regular Papers
· Microelectronics Journal (Elsevier)
· International Journal of Numerical Modelling: Electronic Networks, Devices and Fields (Wiley)
· International Journal of Electronics (Taylor & Francis)

LANGUAGES

English	C2 level (Michigan Proficiency Certificate in English)
Greek	Native language

REFERENCES

· Yiorgos Makris, Professor
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· Matthias Bucher, Associate Professor
Department of Electronic and Computer Engineering, Technical University of Crete, Greece
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· Aria Nosratinia, Professor
Department of Electrical and Computer Engineering, University of Texas at Dallas, USA
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