EE 1202 Experiment #8 – Circuit Design Problems

1. **Introduction and Goal**: Designing circuits is a large part of electrical engineering. After learning some basic circuit principles, it is time to try your hand at two designs. This exercise offers an opportunity to rate your progress in mastering the fundamentals covered in EE 1202.
2. **Equipment List**: The following instruments and components are required:

• Bench instruments, as req. • Prototyping board. • Resistors, 5%, ¼ Watt: 16Ω, 20 KΩ, 100 KΩ, and others.	• Inductor, 10 mH, (1). • Capacitors, 10 μF, 1 μF. • Connecting leads. • Student's calculator.

3. **Experimental Theory**: Today's design problems are (1) a resistive voltage divider and (2) a reactance reduction circuit. The theory required for the two exercises is covered below.

   3.1. A DC Voltage Divider: Passive voltage dividers (voltage dividers without amplifiers or active elements such as transistors) are not used extensively, but can be useful where (1) a small amount of power is required at a different voltage than is available, or (2) cost constraints are high, since a resistor voltage divider is simple and inexpensive.

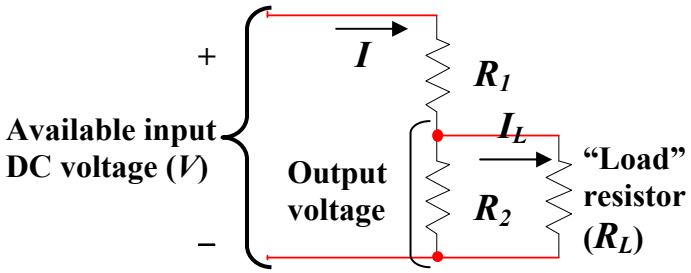

Fig. 1. Schematic of Voltage Divider Circuit.

   3.1.1. Fig. 1 above shows such a voltage divider. Say the voltage requirement is $0.3V$. The output voltage is $I \cdot R_2$; $I = V / (R_1 + R_2)$ (assuming R_L, as shown in Fig.1, is not yet connected). If 70% of the voltage drop is in the upper (R_1) resistor, the desired output voltage will be $0.3\ V$. Since total resistance R_T of the two resistors is $R_1 + R_2$, then to get $0.3\ V$ across the smaller resistor, we need $R_1 = 0.7R_T$, and $R_2 = 0.3R_T$. Clearly, if R_2 is 30% of the total resistance, then the voltage drop on R_2 is $0.3V$. That is, $(R_2 / [R_1 + R_2]) = 0.3$. Clearly, a voltage divider cannot **increase** a voltage.

   3.1.2. From Experiment 2, the parallel resistance of two resistors is **less than either**. When the load resistor is connected, the voltage drop across R_2 is no longer $0.3V$, but a lower voltage (since the parallel

resistance of R_2 and R_L is less than that of R_2).

3.1.3. The desired voltage is much lower for $R_L \le R_2$. In Fig. 2, for example, what if R_1 is 70Ω, R_2 is 30Ω, and R_L is 1Ω? Then without the load, the voltage across R_2 is $0.3V$, V the input voltage. But connect R_2 and R_L in parallel, and we know that the combined resistance will be less than 1Ω! The voltage across R_L will be ≈ 1.5% of V, or ~ 2% of the input voltage. The divider is useless.

3.1.4. The size of R_L is clearly important to the design. The divider must be designed so that with R_L in place, output voltage of the divider is in the desired range. This ability to maintain correct voltage under load is called "voltage regulation."

3.1.5. Thus a resistive voltage divider design has two specifications: First, an output voltage range is specified, (e.g., 0.45 V to 0.55 V, V the input voltage). Second, a resistance range for R_L is specified. If a load resistor is >> R_2 the parallel resistance of R_2 and R_L is ≈ R_2).

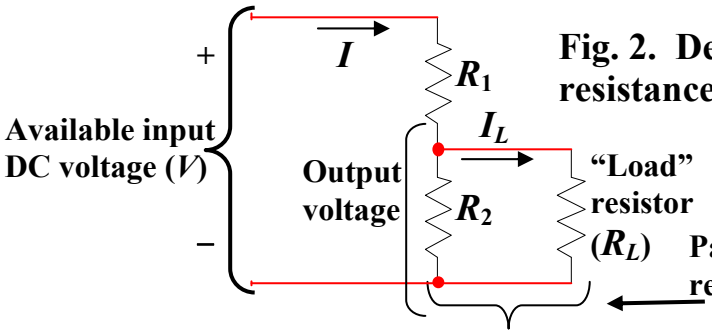

Fig. 2. Definition of parallel resistance.

3.1.6. In Fig. 2, assume the desired output voltage is $0.3V$, ±10%. Then regardless of the values for R_L, the output voltage must be between $0.27V$ to $0.33V$. Then R_1 and R_2 are chosen so that with the largest R_L in place (the largest parallel resistance of R_2 and R_L), the output voltage of the divider must ≤ $0.33V$. For the smallest R_L, (resulting in the lowest parallel resistance), the voltage must be ≥ $0.27V$.

3.1.7. Parallel resistance for R_2 and R_L: $\frac{1}{R_P} = \frac{1}{R_2} + \frac{1}{R_L} = \frac{R_L + R_2}{R_L \cdot R_2}$, or

$R_P = \frac{R_L \cdot R_2}{R_L + R_2}$. With R_P defined, for the output voltage to be in the required range, then:

3.1.8. $$\frac{R_{PMAX}}{R_1 + R_{PMAX}} = \frac{\frac{R_{LMAX} \cdot R_2}{R_{LMAX} + R_2}}{R_1 + \frac{R_{LMAX} \cdot R_2}{R_{LMAX} + R_2}} \le 0.33 ; \quad \frac{R_{PMIN}}{R_1 + R_{PMIN}} = \frac{\frac{R_{LMIN} \cdot R_2}{R_{LMIN} + R_2}}{R_1 + \frac{R_{LMIN} \cdot R_2}{R_{LMIN} + R_2}} \ge 0.27$$

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3.1.9. Rather than trying to solve for R_1 and R_2 in the inequalities above, the following steps make it easy to choose these resistors:

3.1.9.1. Determine the range of R_L.

3.1.9.2. For R_{LMIN} (low end of R_L), choose R_2 such that $\boxed{R_{LMIN} \geq 10R_2}$.

3.1.9.3. Now choose R_1 so that $(R_2 / (R_1 + R_2) \cdot V$ = desired voltage.

3.1.9.4. Example: Input voltage = 10V., desired voltage = 3 V. ±10% (or 2.7-3.3V.), and range of R_L = 10-50KΩ. Then, with R_{LMIN} = 10KΩ, using 3.1.9.2 above, choose R_2 = 1K. Then R_1 = 2333Ω. There are no standard resistors of that value, but there is a 2.2K standard value, which should be close enough. The result: R_2 = 1K, and R_1 = 2.2K.

3.1.9.5. To check this result, with the minimum load resistor value of 10K, the parallel resistance of R_2 and $R_L \approx$ 909Ω. This would give a minimum voltage of $(909 / [2200 + 909]) \cdot (10V) \approx 2.9V$, which is above the minimum allowable of 2.7V. With the maximum load = 50K, the parallel resistance of R_2 and $R_L \approx$ 980Ω. The maximum voltage is then $(980 / [2200 + 980]) \cdot (10V.)$, $\approx 3.1V$, well below the maximum 3.3V.

3.1.10. A last note: R_1 and R_2 must not only satisfy the equation in 3.1.9.2, but also not dissipate so much power that they burn up. That is, we would not want to use 2.2Ω and 1Ω resistors above instead of the 2.2K and 1K Ω resistors, if they were low-power resistors such as those in most of our experiments, because they would quickly burn up. Remember to choose reasonable resistor values since, in your lab problem, you will be using ¼ W resistors.

3.1.11. For the resistors chosen above? Remembering that $I=V/R$, the current in our divider with V = 10V would be 10/(1000+2200) ≈ 0.003A, or 3mA. Since power in a resistor = I^2R, then the power in the two resistors is (0.003)·(3200) = 0.026 Watts, well within the capacity of the two ¼ W resistors.

3.2. Bringing Current and Voltage Into Phase in an AC Circuit: In an inductive AC circuit (ref. Exp. #5), current lags voltage by some phase angle. For $|j\omega L| >> R$, the phase angle can $\rightarrow 90°$ for . Most companies use many AC motors (in air conditioners, on assembly lines, etc.), and electric motors work by virtue of inductive coils. Thus large industries present an inductive load to the power company.

3.3. This inductive load draws current. Inductive current is "imaginary" mathematically, but it is real insofar as the power company demands

that it be paid for! For a large AC power user, reducing inductive load (making the AC voltage and current as close to in-phase as possible) will reduce the power bill. The common name for reducing the phase angle is "making the power factor one." The "power factor" is *cos* θ, θ the voltage/current phase angle in an AC circuit. If the power factor = 1, then the phase angle = 0 (*cos* 0 = 1), and there is no reactive current.

3.3.1. In Fig. 3, the sinusoidal signal generator voltage is $v(t) = V\cos\omega t$.

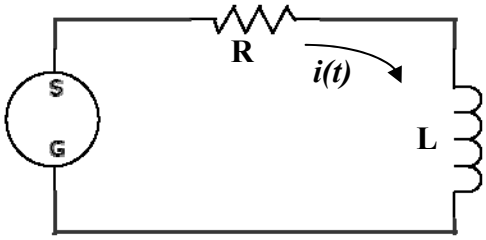


Fig. 3. RL Circuit.

3.3.2. Experiment 5 demonstrated that *V* and *I* are not in phase in this circuit; current lags voltage. Can we reduce the phase angle to 0?

3.3.3. Remember: Inductive impedance = $Z_L = jX_L = j\omega L$; Z_L is always a positive, imaginary value. Capacitive impedance = $Z_C = -jX_C = -j/\omega C$; Z_C is always a negative, imaginary number.

3.3.4. Since inductive and capacitive impedances are imaginary and of opposite sign, adding capacitive reactance of the same magnitude as the inductive reactance in a circuit would result in zero reactance and therefore no reactive current. In Worksheet #8 you will develop a formula to make circuit reactance = 0.

3.3.5. When adding capacitance to an inductive circuit, it may be necessary to use several capacitors to achieve desired capacitance. We saw in Experiment 5 that capacitors in series add reciprocally and inferentially, capacitors in parallel add directly.

3.3.6. For example, paralleling three 1-μF capacitors = 3 μF; 5 μF results from two series 10 μF capacitors. In Fig. 4, a correctly chosen capacitor could bring the power factor to 1 ($\theta = 0$).

3.3.7. For companies with a heavy inductive load, adding a capacitor bank can significantly reduce their electrical power bill.

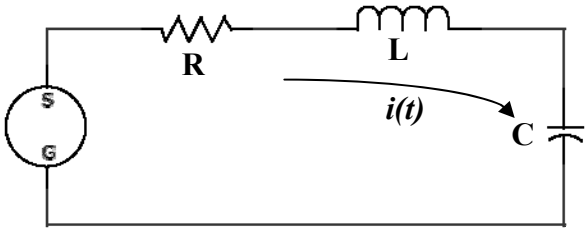


Fig. 4. RL Circuit with Compensating Capacitance to Reduce Phase Angle to 0.

4. Pre-Work: Prior to the lab, study this outline and review capacitive and inductive impedance. Complete formula derivations in Worksheet #8.

5. Design Problems: Design the circuits, as required, in 5.1 and 5.2, below.

5.1. A DC Voltage Divider Circuit: Design a voltage divider as follows:

5.1.1. Input voltage is 10 VDC; desired output of 4 VDC, ± 0.3 V. Use ¼-Watt resistors. Remember not to exceed the power rating of the resistor. The load range is 20-100 KΩ. Over this range, output voltage must be (3.7-4.3 V). That is, at 20 KΩ load, output voltage must be ≥ 3.7 V, and at 100 KΩ load, output voltage must be ≤ 4.3 V.

5.1.2. Construct the voltage divider on your prototype board. Demonstrate that output stays "in spec" over the range of R_L.

5.1.3. Enter required data in your data sheet.

5.2. An AC "Phase Compensated" Circuit:

5.2.1. Using a 10 mH inductor and a 16 Ω resistor, make a circuit as shown in Fig. 3, above. Measure *L* and R_L on the LC meter.

5.2.2. Using the signal generator and oscilloscope channel 1, set the voltage across the series *RL* circuit at 5V pp at 1000 Hz, sinusoidal.

5.2.3. Use oscilloscope channel 2 to measure the 16Ω resister voltage (which will be in phase with the current, as in Experiment #5), to measure the current phase angle.

5.2.4. Using the formula from worksheet #8, calculate capacitive reactance equal to the inductive reactance (based on measured inductance), then convert to capacitance.

5.2.5. Use capacitors from the parts kit in the proper combination to achieve the desired capacitance. Remember the parallel and series capacitance formulas. Due to circuit parameters not taken into account (such as wire lead resistance, etc.), some experimentation with series and parallel capacitors may be necessary. Combine capacitors in series and parallel to create the desired value, e.g., two 1 µF series caps = 0.5 µF, or two parallel 1 µF caps = 2 µF.

5.2.6. For each trial capacitance, check phase angle, as in Experiment #5. It may take some extra capacitance to get θ = 0.

5.2.7. When the *V-I* phase match is correct, demonstrate to the TA.

6. Laboratory Area Cleanup: When work is complete, clean up as usual.

7. Writing the Laboratory Report: There is no report for Experiment 8. Have the TA initial your data sheet. Turn in your Experiment #8 data sheet the next EE 1202 class period.

Experiment # 8 Data Sheet

Note: Complete this data sheet, have the lab TA sign it, and turn it in to verify that you completed Lab 8.

Problem 1 (Voltage Divider):

1. **Remember to estimate power dissipated in your voltage divider. Power dissipated is: $P = I \cdot V = I^2 R$. As your resistors are ¼ Watt, calculate power dissipation in each to assure that they will not be damaged.**

2. **Estimated values for R_1: _____ R_2: _____**

3. **Measured values of R_1: _____ R_2: _____**

4. **Measured values of 20KΩ _____ and 100KΩ _____ test load resistors.**
5. **Minimum load voltage (20K Ω resistor in place): _____ (must be ≥ 3.7 V.).**
6. **Maximum load voltage (100K Ω resistor in place): _____ (must be ≤ 4.3 V.).**

Problem 2 (Capacitor Bank):

7. **Formula you developed for capacitance to offset inductance: _____**

8. **10 mH inductor measured inductance: _____ resistance: _____**

9. **Measured value of nominal 16 Ω resistor : _____**

10. **Measured value of peak-to-peak voltage of ~1000 Hz signal: _____**

11. **Calculated inductive reactance: _____**

12. **Desired capacitance to offset inductive reactance in 11: _____ (calculated from formula developed in worksheet).**
13. **Measured value of capacitors used to reduce phase angle to 0 degrees (power factor =1); use as many spaces as needed:**

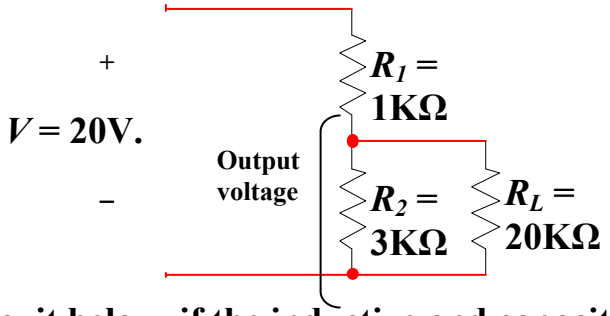
    _____ , _____ , _____ , _____ , _____ , _____ , _____
14. **Total value of capacitance used (remember to add parallel and series capacitances correctly!) _____**

Experiment #8 Worksheet

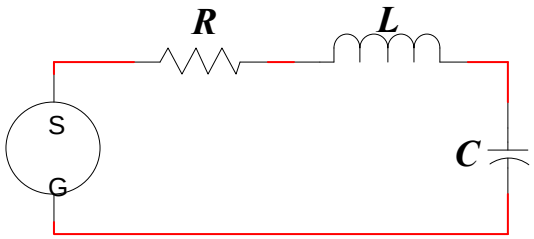
1. **What is the resistance of 3-10KΩ resistors:**

In series? _____ **In parallel?** _____

2. **Given the voltage divider circuit shown, with input voltage of 20V, R_1 = 1KΩ and R_2 = 3KΩ, and R_L = 20KΩ. Output voltage across R_2 should be 15V, ±0.1V. Can this voltage divider meet the specification as shown?**



3. **In the circuit below, if the inductive and capacitive impedances have the same magnitude, since they are opposite in sign, they will cancel each other out, and there will be no imaginary current in the circuit. That is, if we have: $1/j\omega C = -j\omega L$, then net reactance = 0. Based on this equation, solve for a value C in terms of L and ω, which will cancel the inductive impedance of L. You will use this formula in Experiment 8.**



4. **In the circuit above, if L is 20mH, find C such that $|j\omega L| = |1/j\omega C|$, if the radian frequency ω of the circuit is 1000 rad/sec.**

C = _____

5. **In the circuit above, if the signal frequency is 60 Hz, what must C be to ensure that the circuit reactance is zero, given the same L?**

C = _____