Instructions for Using 74LS195 as a Storage Register

For lab #4, the 74LS195 shift register can also be used as a 4 bit storage register. Here are instruction for utilizing SN74LS195 (from Motorola) as the register.

\[ \text{MR Master Reset (Active LOW) input} = +5V \]
\[ J \text{ input} = X \text{ (don’t need; simply ground it)} \]
\[ K \text{ input} = X \text{ (don’t need; simply ground it)} \]

\[ P0 \sim P3 = \text{Parallel data inputs} \]
\[ \overline{PE} \text{ Parallel enable – active low}(= 0V) \]

CP Clock – data clock; active hight (= 1), can use pulse switch

\[ Q0 \sim Q3 – \text{Parallel outputs (i.e., register outputs)} \]

Pin layout of 74LS195:

To store the P0-P3 inputs, a positive pulse on the CP input will store the 4 bits of data. Note: 74195 circuits from different companies work in the same way, but definition of the individual pins may be a bit different. If you want to check more information about this chip, please search for the datasheet on-line, which can explain the 74LS195 in detail.