Simple RS-Flip-Flops can be made from any two 2-input combinational logic gates plus some inverters. Design the following RS flip-flops, labeling S, R, Q, Q-Not (and clock, as necessary). Make sure you label the polarity of R and S when active (+ =1 or – =0)).

1. (CLO 4—Seq. Logic) Two OR gates, and inverters as needed. Inputs S and R are active low (0). Either of TWO answers are acceptable.

2. (CLO 4—Seq. Logic) An AND gate, an OR gate, and inverters as needed. Inputs S and R active low (0).

3. (CLO 4—Seq. Logic) Two NORs plus inverters as needed. Inputs must be active low (0). Note: you should need only FOUR (4) inverters. Think about it.

4. (CLO 4—Seq. Logic) A NOR and a NAND plus inverters as needed. Inputs must be active high (1).

Note: the NOR and NAND sections can be interchanged between top and bottom.
5. (CLO 4—Seq. Logic) Construct a clocked RS flip-flop using FOUR (4) OR gates and inverters. Note that Set and Reset are active in the high (1) state.

![Diagram of a clocked RS flip-flop using OR gates and inverters]

6. (CLO 4—Seq. Logic) Given the clocked RS flip-flop shown, plot the output Q versus clock, Set, and Reset as shown below. Remember that Set and Reset are active high (1).

![Diagram of clocked RS flip-flop with waveforms for Q, S, R, and Clock]

![Graph showing waveforms for Q, S, R, and Clock]