Evaluation of Circulating Current Suppression Methods for Parallel Interleaved Inverters

Ghanshyamsinh Gohil, Lorand Bede, Remus Teodorescu, Tamas Kerekes, Frede Blaabjerg
Department of Energy Technology, Aalborg University, Denmark
gvg@et.aau.dk

Abstract—**Two-level Voltage Source Converters (VSCs) are often connected in parallel to achieve desired current rating in multi-megawatt Wind Energy Conversion System (WECS). A multi-level converter can be realized by interleaving the carrier signals of the parallel VSCs. As a result, the harmonic performance of the WECS can be significantly improved. However, the interleaving of the carrier signals may lead to the flow of circulating current between parallel VSCs and it is highly desirable to avoid/suppress this unwanted circulating current. A comparative evaluation of the different methods to avoid/suppress the circulating current between the parallel interleaved VSCs is presented in this paper. The losses and the volume of the inductive components and the semiconductor losses are evaluated for the WECS with different circulating current suppression methods. Multi-objective optimizations of the inductive components have been also carried out. The design solutions, that are obtained using the optimization, have been compared on the basis of the volume of the inductive components and yearly energy loss for a given mission profile.**

Index Terms—**Voltage source converters (VSC), coupled inductor, circulating current, multi-objective optimization, harmonic filter, interleaving**

I. INTRODUCTION

A full scale power converter is typically used in modern Wind Energy Conversion System (WECS) due to its ability to meet the stringent grid-code requirements and it is often realized using three-phase two-level pulse width modulated Voltage Source Converter (VSC) [1]. The power rating of the WECS is continuously increasing, whereas the power processing capability of the existing Insulated Gate Bipolar Transistors (IGBTs) modules is limited. As a consequence, the two level VSCs are connected in parallel [2], [3] to match the high power rating of the wind turbine. For parallel connected VSCs, multi-level voltage waveforms can be achieved by interleaving the carrier signals of the parallel VSC legs [4], [5]. As a result, the harmonic quality of the resultant voltage waveform can be substantially improved, which can be utilized to achieve the following system level advantages:

1) Efficiency improvement, which can primarily be achieved by reducing the switching frequency.
2) Power density improvement, obtained by reducing the size of the harmonic filter components.

However, the circulating current flows between the parallel VSCs due to the hardware and control asymmetries. The problem related to the circulating current further aggravates when the carrier signals are interleaved. This unwanted circulating current increases the stress on the semiconductor switches and

causes additional losses. Therefore, it should be suppressed to some acceptable limits.

The circulating current can be avoided by providing galvanic isolation between the parallel VSCs using multiple winding line frequency transformer [6], [7]. Another approach is to suppress the circulating current to some acceptable limit by introducing impedance in the circulating current path. This can be achieved by

1) Using single phase harmonic filter inductor, which provides the functionalities of the boost inductor, as well as used for circulating current suppression.
2) Using Coupled Inductor (CI) to suppress the circulating current by providing magnetic coupling between the parallel interleaved legs of the corresponding phases [4], [8].

The selection of the circulating current suppression method has a significant influence on the system efficiency, power density, and the WECS control. However, from a system perspective, a comparative evaluation of the different circulating current suppression methods has not been reported so far. This paper is an attempt to bridge this gap. The impact of the selection of the circulating current suppression method on the system efficiency and volume is investigated in this paper. The semiconductor losses, the volume and the losses in the inductive components are evaluated and a mission profile based multi-objective optimization has been carried out. The optimized designs are finally compared on the basis of the yearly energy loss and the volume of the inductive components. The paper is organized as follows. The system specifications and the considered filter arrangement is presented in Section II. The loss models of the semiconductor switches and filter components, along with the volume models of the filter components are discussed in Section III. The system losses and volume of the given specifications are calculated and the comparative evaluation is presented in Section IV.

II. SYSTEM DESCRIPTION AND CONSIDERED TOPOLOGIES

The description of the considered WECS, basic operation of the parallel interleaved VSCs, and the considered filter arrangements are discussed in this section.

A. System Description

A grid-side converter of the WECS is considered and the system specifications are shown in Table I. The associated base values for the per-unit system is given in Table II. The

TABLE I
SYSTEM SPECIFICATIONS

Parameter	Rated power	Converter voltage	MV Grid voltage	Nominal frequency
Values	3.7 MVA	690 V	30 kV	50 Hz

TABLE II
BASE VALUES FOR PER-UNIT SYSTEM

Parameters	power	Voltage	Inductance	Capacitance
Base values	3.7 MVA	690 V	409 µH	24.7 mF
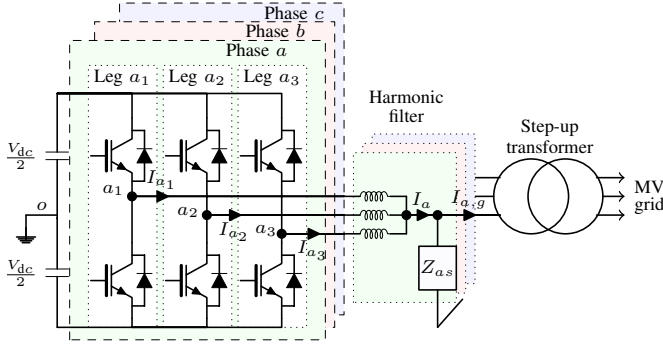
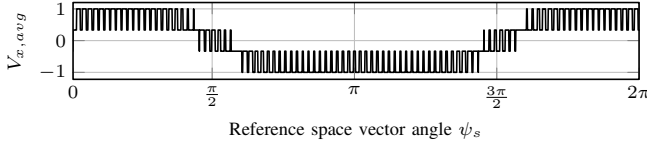Fig. 1. Grid-side converter, realized using three parallel two-level voltage source converters.

Fig. 2. Resultant switched output voltage of three parallel interleaved two-level voltage source converters. The voltage is normalized to half of the dc-link voltage $V_{dc}/2$.

WECS is considered to be connected to the 30 kV grid using a step-up transformer. The required power rating of 3.7 MVA is achieved by connecting three VSCs in parallel, with each having a power rating of 1.23 MVA. The switching frequency is taken to be 1050 Hz. The parallel VSCs with the common dc-link are considered in this paper and the dc-link voltage is set to 1100 V. The parallel VSCs with the synchronized gate pulses (without carrier interleaving) are shown in Fig. 1. For the parallel VSCs, the resultant switched output voltage $V_{x,avg}$ is the average of the switched output voltages of the individual VSCs and it determines the harmonic performance of the WECS.

Instead of using the synchronized carrier signals for the VSCs, they can be phase-shifted and a multi-level voltage waveform for the resultant switched output voltage $V_{x,avg}$ can be achieved as shown in Fig. 2. As a result, the harmonic performance can be significantly improved, which leads to reduction in the harmonic filtering requirement. However, the switched output voltages of the parallel legs of a given phase are shifted with respect to each other. This would drive large circulating current between the parallel legs. The flow of this unwanted circulating current increases the losses and demands unnecessary oversizing of the components which are present in

TABLE III
FILTER PARAMETERS

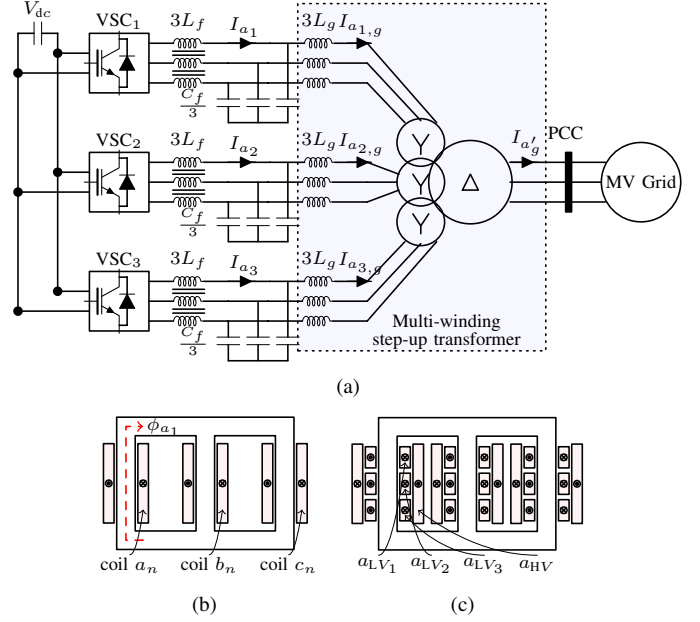| Filter	L_f	L_g	C_f	C_d
LCL filter	0.09 pu	0.085 pu	0.075 pu	0.075 pu

Fig. 3. (a) Grid-side converter configuration with three parallel interleaved VSCs. The simplified arrangement of the LCL filter is shown. Multiple isolated windings are used on the low-voltage side of the transformer to avoid the flow of the circulating current. (b) Magnetic structure of the converter-side inductor. $n \in \{1, 2, 3\}$, (c) Multi-winding step-up transformer.

the circulating current path. Therefore, the circulating current should be suppressed to some acceptable value to realize the full potential of the parallel interleaved VSCs.

B. Harmonic Filter

LCL filter with R_d/C_d damping branch is considered. The harmonic filter is designed to meet the harmonic current injection limits specified by the German Association of Energy and Water Industries (BDEW) [9] and the parameters of the harmonic filter are specified in Table III. The WECS is connected to the medium-voltage network using the step-up transformer and the leakage inductance of the transformer is considered to be a part of the grid-side inductor of the LCL filter. The per-unit values of the harmonic filter parameters are taken to be the same in all the considered cases.

C. Circulating Current Suppression

Three different methods for circulating current suppression are discussed hereafter.

1) Case I: With Multiple Isolated Transformer Windings:
The WECS is connected to the MV network using the step-up transformer. On the low voltage side of the transformer, three isolated windings can be used as shown in Fig. 3(a) and the circulating current can be avoided. Each of the VSCs has separate harmonic filter. The magnetic structures of the three-phase converter-side inductor and the multi-winding step-up transformer are shown in Fig. 3(b) and Fig. 3(c), respectively.
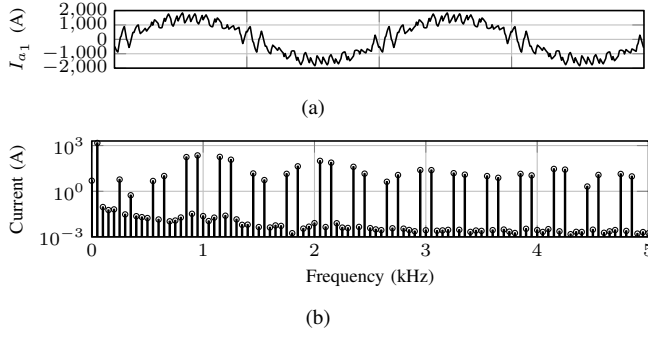
(a)

(b)

Fig. 4. Case I: with multiple isolated transformer windings (see Fig. 3). Switching frequency is 1050 Hz. (a) Simulated leg current of VSC1 I_{a_1}, (b) Harmonic spectrum of I_{a_1}.
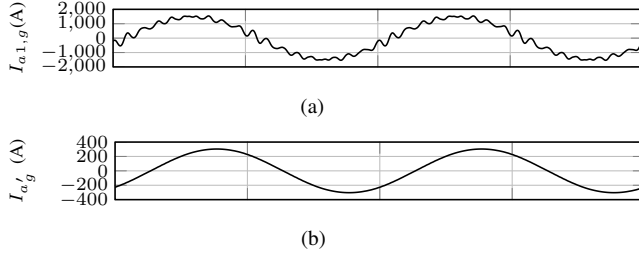

(a)

(b)

Fig. 5. Case I: with multiple isolated transformer windings (see Fig. 3). (a) Current through the low-voltage winding of the transformer, (b) Injected grid current on the medium-voltage side of the transformer.

Due to the interleaved carrier signals, some of the harmonic components in the switched output voltages of the individual components are phase-shifted with respect to each other. As a result, the harmonic components of the switched output voltages of the individual VSCs can be divided as:

1) In-phase harmonic components, concentrated around the carrier frequency harmonics $3j$ and their side-bands, where $j = 1$ to ∞.
2) Phase-shifted components, concentrated around the carrier frequencies harmonics $(3j - 1)$, $(3j - 2)$ and their side-bands.

When the phase-shifted voltage components are applied to the step-up transformer, the corresponding flux components are also phase-shifted and they are either completely canceled out or significantly reduced. Therefore, the phase-shifted harmonic components are absent in the induced voltages. This leads to significant improvement in the harmonic quality of the line current on the high-voltage side of the transformer. Since the phase-shifted harmonic components are also absent on the low-voltage side, the corresponding harmonic components of the switched output voltage of the individual VSCs appears across the harmonic filter.

The simulations of the system shown in Fig. 3(a) have been carried out using the PLECS simulation tool for the full load condition. The parameters used for the simulation study are given in Table I. The current flowing through the converter-side inductor is shown in Fig. 4(a) and the corresponding harmonic spectrum is also shown in Fig. 4(b). From Fig. 4(b), it is clear that the major harmonic component appear at the first carrier harmonic frequency. Since, the converter-side inductor
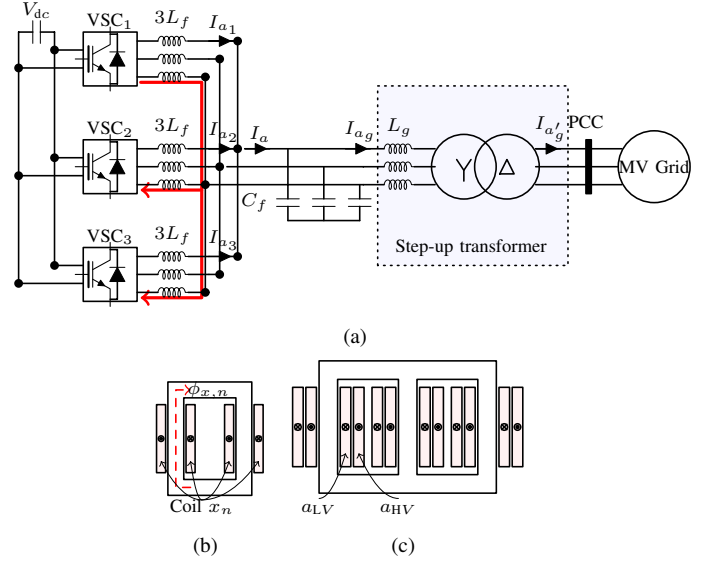

(a)

(b)   (c)

Fig. 6. (a) Grid-side converter configuration with three parallel interleaved VSCs with single-phase converter-side inductor. (b) Structure of the single-phase inductor, (c) Structure of the step-up transformer.

flux is proportional to this current, the flux also contains these harmonic frequency components. As a result, both the in-phase and the phase-shifted harmonic components contribute towards the core and copper losses of the converter-side inductor.

The current flowing through the low-voltage winding of the step-up transformer is shown in Fig. 5(a). It also contains the phase-shifted harmonic components, though their magnitude is reduced compared to the converter-side inductor current due to the filtering effect of the LCL harmonic filter. The presence of the phase-shifted harmonic frequency components in the low-voltage winding of the step-up transformer leads to increased copper losses. The injected grid current on the medium-voltage side of the transformer is also shown in Fig. 5(b). The phase-shifted harmonic frequency components are absent and desired current quality can be obtained, as it is seen from Fig. 5(b).

2) Case II: With Single-Phase Converter-side Inductor:
The other possible arrangement of the grid-side converter is shown in Fig. 6. Single-phase inductors are used as a converter-side inductor of the LCL filter. The magnetic structure of such inductor is shown in Fig. 6(b). The volume of three single-phase inductors may be higher than the volume of a single three-phase inductor. However, the three-phase inductor structure, as shown in Fig. 3(b), may not be used in this case since the common-mode circulating flux component, which is present due to the carrier interleaving, does not have a low reluctance magnetic path in three-phase magnetic structure. As a result, the inductance offered to the common-mode circulating current is very small and it is highly undesirable. To overcome this issue, single-phase inductors may be used, as shown in Fig. 6(a), where the circulating current path is also demonstrated. The single-phase inductor provides following functionalities:

1) Used as a converter-side inductor of the LCL filter.
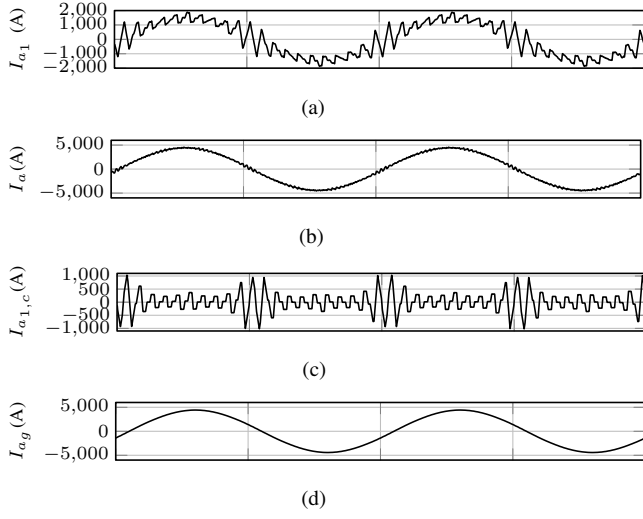2) Offers inductance to the circulating current.

Fig. 7. Case II: with single-phase converter-side inductor (see Fig. 6). switching frequency is 1050 Hz. (a) Simulated leg current of VSC1 I_{a_1}, (b) Total current $I_a = I_{a_1} + I_{a_2} + I_{a_3}$, (c) Circulating current $I_{a_{1,c}} = I_{a_1} - (I_a/3)$, (d) Current through the low-voltage winding of the transformer.

However, the major limitation with this approach is that the value of the inductor influences the dc-link voltage level requirement and the transient response of the system. Higher converter-side inductance demands more dc-link voltage, which leads to more switching losses. Moreover, the current response becomes more sluggish and the weight and the volume of the WECS increases. In addition, the inductance required for the harmonic current filtering may not be very effective in suppressing the circulating current.

The system was simulated with the same system parameters that were used for case I. The current flowing through the converter-side inductor is shown in Fig. 7. The leg current (converter-side inductor current) I_{x_n} can be split into two components:

1) A component contributing to the resultant line current $I_{x_{n,l}}$.
2) a circulating current component $I_{x_{n,c}}$.

and it can be represented as

$$I_{x_n} = I_{x_{n,l}} + I_{x_{n,c}} \tag{1}$$

where x represents phase ($x \in \{a, b, c\}$) and n represent the VCS ($n \in \{1, 2, 3\}$). The circulating current components $I_{x_{n,c}}$ only flows between the parallel VSCs and do not contribute to the resultant line current. Therefore, the resultant line current can be given as

$$I_x = \sum_{k=1}^{N} I_{x_{n,l}} \tag{2}$$

Assuming an equal line current sharing between the parallel VSCs, the common component of the leg current is obtained as $I_{x_{n,l}} = I_x/N$. The resultant line current of phase a is shown in Fig. 7(b). The circulating current is obtained using (1) and it is shown in Fig. 7(c). The circulating current has a major harmonic component at the 1st carrier harmonic frequency and its maximum peak amplitude is 980 A. The high value of the

(a)

coil x_1 coil x_2 coil x_3 coil a coil b coil c

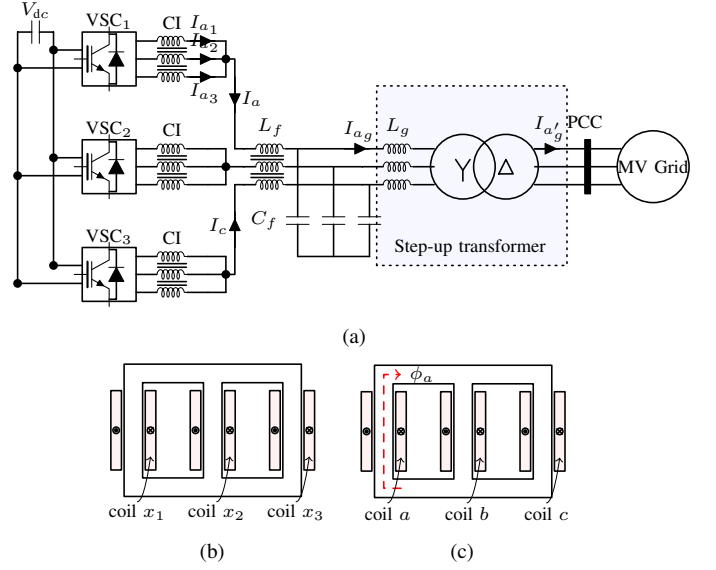(b)   (c)

Fig. 8. (a) Grid-side converter configuration with three parallel interleaved VSCs with coupled inductor for circulating current suppression and three-phase inductor as a converter-side inductor. (b) Coupled inductor (CI), $x \in \{a, b, c\}$, (c) Converter-side inductor L_f.

maximum peak amplitude demonstrates that the single-phase inductor is not very effective in suppressing the circulating current.

Since the single-phase inductor is subjected to phase-shifted flux component, the use of the 0.35 mm grain oriented silicon steel leads to significant core losses. The current through the low-voltage winding of the step-up transformer is shown in Fig. 7(d). This current is almost harmonic free. As a result, lower copper losses in the transformer can be achieved compared to case I. Moreover, standard two-winding transformer is required, compared to the multi-winding transformer in Case I.

3) Case III: With Coupled Inductor (CI) and Three-Phase Converter-side Inductor: The CI offers high inductance to the circulating current component [4], [8], [10], [11], while its effect on the line current component is minimal (assuming negligible leakage flux). Therefore, the disadvantages of case II, such as high dc-link voltage requirement, sluggish response, and high circulating current, can be overcome by using CI. The schematic of the WECS is shown in Fig. 8(a), where the individual CI for each phase is used.

The magnetic structure of the CI is shown in Fig. 8(b). It consists of three magnetic limbs, around which the coils are placed. All the coils are wound in the same direction and the limbs are magnetically coupled to each other using the top and bottom yokes. The start terminal of each of the coils is connected to the corresponding output terminals of the VSC legs, whereas the other terminal of all the coils is connected to the common point, as shown in Fig. 8(a). The CI offers small leakage inductance, which in addition with the three-phase inductor L_f forms the converter-side inductor of the LCL filter. A three-phase inductor, shown in Fig. 8(c), is used as converter-side inductor. The magnetic core of the CI mainly
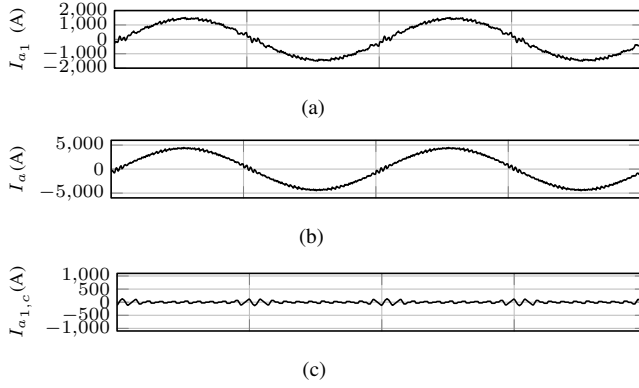
Fig. 9. Case III: with coupled inductor and three-phase converter-side inductor (see Fig. 8). switching frequency is 1050 Hz. (a) Simulated leg current of VSC1 I_{a_1}, (b) Resultant current $I_a = I_{a_1} + I_{a_2} + I_{a_3}$, (c) Circulating current $I_{a_1,c} = I_{a_1} - (I_a/3)$.

TABLE IV
DESCRIPTION OF THE IGBT MODULES

Manufacturer	Part No.	V_{CES}	$I_{c_{nom}}$
Infineon	FF1000R17IE4	1700 V	1000 A
Infineon	FF1400R17IP4P	1700 V	1400 A

experiences high frequency flux excitation (flux reversal at the switching frequency). Therefore to reduce losses, amorphous alloy 2605SA1 is considered as a magnetic material for CI, whereas 0.35 mm grain oriented silicon steel is considered as a core material for the three-phase inductor.

The simulated currents are shown in Fig. 9. The circulating current is shown in Fig. 9(c), where the maximum peak amplitude is 120 A against 980 A in the case II. As a result, the associated copper loss and semiconductor loss can be reduced. The current through the converter-side inductor is shown in Fig. 9(b). The harmonic components are significantly smaller compared to the previous cases. As a result, the copper losses and the core losses in converter-side inductor are significantly lower compared to the other cases.

III. ACTIVE AND PASSIVE COMPONENT MODELING

The loss and volume models of the active and passive components are presented in this section.

A. Semiconductor Losses

The IGBT modules considered in this study are given in Table IV.

1) Conduction Losses: The conduction losses in the transistor and the diode are calculated for each of the sampling interval for the positive half cycle of the line current. For the kth sampling interval, the transistor and diode conduction losses are given as

$$p_{\text{con},T_k} = V_{CE0_k} i_{\text{avg},T_k} + r_{CE_k} i_{\text{rms},T_k}^2 \tag{3a}$$

$$p_{\text{con},D_k} = V_{F0_k} i_{\text{avg},D_k} + r_{D_k} i_{\text{rms},D_k}^2 \tag{3b}$$

where V_{CE0_k} and V_{F0_k} are the bias voltage for kth sampling interval for transistor and diode, respectively. r_{CE_k} and r_{D_k} are the dynamic resistance of the transistor and diode, respectively. The bias voltage and the dynamic resistance
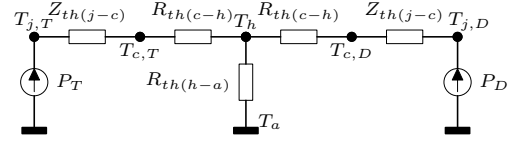

Fig. 10. Simplified thermal model of transistor and diode. P_T and P_D are the transistor and diode power losses, respectively.

are dependent on the junction temperature and the current flowing through the device. The on-state characteristic of the transistor and the forward characteristic of the diode are acquired from the manufacturer datasheet and the bias voltage and the dynamic resistance for a given sampling interval are obtained using the linear interpolation. The total conduction losses are obtained by averaging the local conduction losses of the sampling intervals during the fundamental frequency cycle and it is given as

$$P_{\text{con},T} = \frac{f_0}{2f_c} \sum_{k=1}^{\frac{f_c}{f_0}} p_{\text{con},T_k}; \quad P_{\text{con},D} = \frac{f_0}{2f_c} \sum_{k=1}^{\frac{f_c}{f_0}} p_{\text{con},D_k} \tag{4}$$

2) Switching losses: The switching losses are calculated locally for each of the switching transition during the positive half cycle of the line current. Assuming linear dependency of the switching energies on the dc-link voltage, the switching energies for the specified dc-link voltage for the kth sampling interval are given as

$$E_{\text{on}_k}(i, T_{j,T}, V_{dc}) = E_{\text{on}_k}(i, T_{j,T}, V_{\text{nom}}) \frac{V_{dc}}{V_{\text{nom}}} \tag{5a}$$

$$E_{\text{off}_k}(i, T_{j,T}, V_{dc}) = E_{\text{off}_k}(i, T_{j,T}, V_{\text{nom}}) \frac{V_{dc}}{V_{\text{nom}}} \tag{5b}$$

where V_{dc} is the dc-link voltage, V_{nom} is nominal dc-link voltage at which the switching energies are specified. E_{on_k} and E_{off_k} are the switching energy during the turn-on and turn-off transition, respectively. $T_{j,T}$ is the junction temperature of the transistor. The switching losses are calculated by averaging the local switching energies of the switching transitions that occur during the positive half cycle of the line current and it is given as

$$P_{sw,T} = \frac{f_0}{2f_c} \sum_{k=1}^{\frac{f_c}{f_0}} [E_{\text{on}_k}(i, T_{j,T}, V_{dc}) + E_{\text{off}_k}(i, T_{j,T}, V_{dc})] \tag{6}$$

Similarly, the diode reverse recovery losses $P_{sw,D}$ are also obtained by the same method.

3) Thermal Model: The loss model needs the information of the junction temperatures $T_{j,T}$ and $T_{j,D}$ and they are obtained by using the simplified thermal model shown in Fig. 10. The junction-to-case thermal impedance $Z_{th(j-c)}$ is generally modeled as a 4th order Foster network and can be described as

$$Z_{th(j-c)} = \sum_{i=1}^{4} R_i(1 - e^{-t/\tau_i}) \tag{7}$$
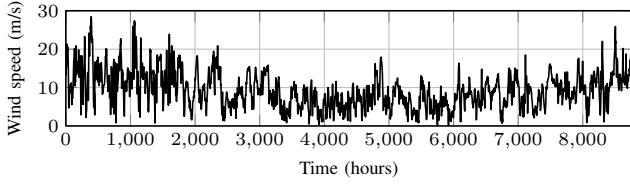
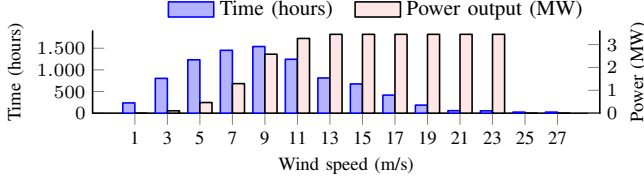Fig. 11. Recorded wind data over a year with three hourly sampling rate.

Fig. 12. Assumed wind speed distribution and power produced. The total energy production in a year is 18195 MWh for 3.45 MW wind turbine.

where $Z_{th(j-c)}$ is the junction-to-case thermal impedance. The parameters of the foster network R_i and τ_i are extracted from the manufacturer datasheet.

B. Winding and Core Losses in Inductive Components

The loss model for the CI, converter-side inductor, and step-up transformer are presented hereafter.

1) Copper Loss: The copper loss is evaluated by considering the ac resistance of the winding, which takes into account the skin and proximity effects [12]. The winding loss of a given coil is

$$P_{cu} = R_{dc} \sum_{h=1}^{\infty} k_{p_h} I_{w_h}^2 \qquad (8)$$

where

$$k_{p_h} = \sqrt{h}\Delta \left[\frac{\sinh(2\sqrt{h}\Delta) + \sin(2\sqrt{h}\Delta)}{\cosh(2\sqrt{h}\Delta) - \cos(2\sqrt{h}\Delta)} \right. $$
$$ \left. + \frac{2}{3}(m^2 - 1)\frac{\sinh(\sqrt{h}\Delta) - \sin(\sqrt{h}\Delta)}{\cosh(\sqrt{h}\Delta) + \cos(\sqrt{h}\Delta)} \right] \qquad (9)$$

and $\Delta = T_c/\delta$ and R_{dc} and R_{ac} are the dc and the ac resistance of the coil, respectively. m is the number of layers in the coil, T_c is the thickness of the conductor, and δ is the skin depth. I_{w_h} is the hth harmonic frequency component of the current flowing through that coil.

2) Core Losses: The core losses are calculated using the Steinmetz equation. The core losses per unit volume is given as

$$P_{fe,v} = k_i f^\alpha \hat{B}^\beta \qquad (10)$$

where k_i, α, and β are the Steinmetz parameters.

IV. COMPARATIVE EVALUATION

All three cases are evaluated for the 3.45 MW WECS. The recorded wind speed data at Aalborg University over a one year period with three hourly sampling rate is shown in Fig. 11. Since the wind speed varies in a large range, the power processed by the WECS also varies in wide range, as shown in Fig. 12. Therefore, the energy loss for a given mission profile is evaluated and compared instead of comparing the losses at a specific loading condition.
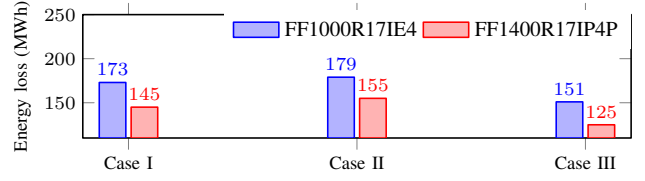

Fig. 13. Semiconductor energy loss over a one year time period. Two IGBT modules from Infineon are considered and the data are given in Table IV.

A. Semiconductor Energy Loss

The total semiconductor losses ($P_{con,T} + P_{con,D} + P_{sw,T} + P_{sw,D}$) are evaluated for each of the loading conditions shown in Fig. 12 and the total energy losses of all the semiconductor switches are obtained as

$$E_s = 18 \times \sum_{i=1}^{j} (P_{con,T} + P_{con,D} + P_{sw,T} + P_{sw,D})T_i \quad (11)$$

The semiconductor energy loss of the whole system over a one year time period for the different cases are shown in Fig. 13. Single-phase inductor, used in case II, is not effective in suppressing the circulating current. Since the unwanted circulating current flows through the semiconductor switches, it leads to higher semiconductor losses and therefore the highest semiconductor energy loss in all three cases, as shown in Fig. 13. In case I, the phase-shifted components are zero in the induced voltages across the step-up transformer windings. Therefore, the phase-shifted harmonic components present in the switched output voltage appears across the harmonic filter and the their current magnitude depends on the impedance offered by the harmonic filter, which is relatively small for the multi-level converter realized using the carrier interleaving. As a result, the magnitude of the phase-shifted harmonic current components is significant (see Fig. 4) and leads to more semiconductor losses, as shown in Fig. 13. On the other hand, the CI effectively suppresses the circulating current. As a result, the semiconductor energy loss is significantly smaller in case III. For the Infineon IGBT module FF1000R17IE4, the semiconductor energy loss in case III is 151 MWh, as against 173 MWh and 179 MWh in case I and case II, respectively.

B. Energy Loss and Volume of Inductive Components

To compare the volume and energy losses of the magnetic components, multi-objective optimization of the magnetic components is carried out for the load profile shown in Fig. 11. The multi-objective optimization minimizes a vector of objectives $F(X)$ and returns the optimal values of the design variables X.

$$\min F(X) \qquad (12)$$

where

$$F(X) = [F_1(X), F_2(X)] \qquad (13)$$

where $F_1(X)$ returns the energy loss (MWh) and $F_2(X)$ return the volume of the active parts in Ltr. The non-inferior (Pareto optimal) solutions are obtained using the multi-objective optimization. Out of these several possible design solutions, one
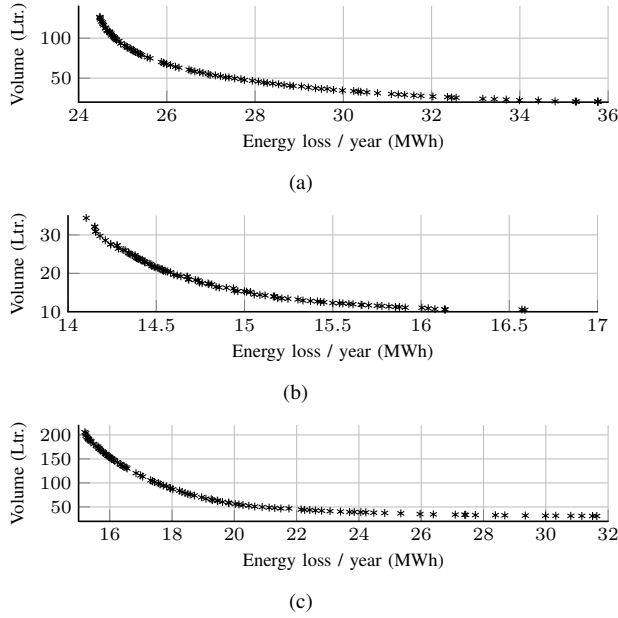
Fig. 14. Calculated volume and energy loss of the converter-side inductor for different Pareto optimal solutions. (a) Case I: 118.5 μH, 1032 A, three-phase inductor, (b) Case II: 118.5 μH, 1032 A, single-phase inductor, (c) Case III: 30 μH, 3096 A, three-phase inductor.
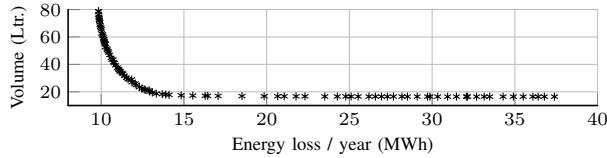

Fig. 15. Calculated volume and energy loss of the coupled inductor for different Pareto optimal solutions.

suitable solution has been selected for each of the magnetic components for the comparison.

1) Converter-side Inductor: The converter-side inductor is assumed to be realized using the standard laminated steel and the coils are wound using the copper foil winding. The stacking factor is assumed to be 0.96. To limit the air gap fringing flux, several small air gaps are employed. This is achieved by using the discrete core blocks. For each design solutions, core and copper losses are evaluated at the rated load conditions and the results are fed to the thermal network derived in [13]. By solving the thermal network, the temperature of the core and the coil are obtained. This gives the worst case temperature rise. If the temperature rise is above 80°C, the solution is discarded and the optimization steps are again executed for a new set of free variables.

The Pareto-optimal solutions for converter-side inductor for all the considered cases are shown in Fig. 14, where the reduction in the energy loss requires increase in the volume.

2) Coupled Inductor: Considering equal current sharing between the parallel VSCs, the fundamental component of the flux in the CI is absent. As a result, the CI only experiences switching frequency flux excitation. Since amorphous alloy is very suitable for medium frequency, it is considered as a magnetic material for CI. Copper foil winding is considered

for coils. The losses and the volume of the CI are evaluated and multi-objective optimization has been carried out. Pareto-optimal solutions for CI are shown in Fig. 15.

3) Step-up Transformer: Four stepped cruciform grain oriented silicon steel is considered, where the net core area is 78% of the area of the circumscribing circle. The low voltage winding is placed around the core and it is wound using the copper foil. The foil winding is also considered for the medium-voltage winding due to its uniform and superior electrical stress of the inter-turn insulation. The creepage clearance for the medium-voltage winding is taken to be 30 mm.

The Pareto optimal solutions for the step-up transformer and multi-winding step-up transformer are shown in Fig. 16. The power handled by the step-up transformer in the WECS varies in a wide range. In this case, the energy loss in the transformer can be reduced by ensuring lower core losses (fixed losses). This can be achieved by reducing the core volume by employing more number of turns. For case I, the current flowing through the low-voltage coils of the step-up transformer comprises significant harmonic components, as shown in Fig. 5. On the other hand, the current through the low-voltage coils in case II and case III is almost sinusoidal. Therefore for a given volume, the higher harmonic content in the low-voltage winding in case I leads to significant higher copper losses compared to the case II and case III, as shown in Fig. 16.

C. System Volume and Energy Loss

The Pareto optimal solutions are the non-inferior design solutions. Out of these non-inferior designs, one suitable design is selected for each of the components. The selection was carried out in such manner that the total volume of the inductive components in each cases are the same. The design parameters of the selected designs of the converter-side inductor are given in Table V. Similarly, the design parameters of the multi-winding step-up transformer and two-winding step-up transformer are given in Table VI. The total volume of the inductive components, including step-up transformer is
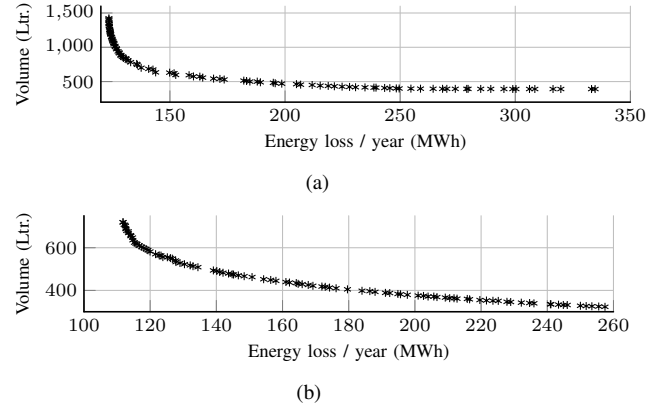

Fig. 16. Calculated volume and energy loss of the step-up transformer for different Pareto optimal solutions. (a) Multi-winding step-up transformer considered in case I, (b) Step-up transformer considered in case II and case III.

Parameters	Case I	Case II	Case III	
			L_f	CI
Inductance (µH)	118.5	118.5	30	970 (L_σ=9.5)
Current rating (A)	1032	1032	3096	1032 A
No. of turns	28	39	7	15
Core cross-section (cm^2)	78.8	50.92	187.9	61
Coil cross-section (mm^2)	486	542	2334	390
Volume (Ltr.)	50.85	20.29	105.54	24.97
Energy loss/year (MWh)	27.4	14.58	17.31	12.11
No. of inductors	3	9	1	3

Parameters	Multi-winding transformer	Two winding transformer
Core cross-section (cm^2)	752	763
No. of turns in primary	16	16
Coil cross-section of primary (mm^2)	355	1206
No. of turns in secondary	1204	1204
Coil cross-section of primary (mm^2)	12	17
Volume (Ltr.)	619.6	595.1
Energy loss/year (MWh)	151.6	118.5

Item	Volume (Ltr.)			Energy loss/year (MWh)		
	Case I	Case II	Case III	Case I	Case II	Case III
Semiconductor	-	-	-	173	179	151
Inductor L_f	152.5	182.6	105.5	82.2	131.2	17.3
CI	-	-	74.9	-	-	36.3
Transformer	619.6	595.1	595.1	151.6	118.5	118.5
Total	772.1	777.7	775.5	406.8	428.7	323.1

given in Table VII for all the considered cases. As mentioned, the designs are chosen to ensure that the volumes of the inductive components are the same in all the cases. Under this case, the total energy loss (including semiconductor energy loss) of the WECS for all three cases are also given in Table VII. The WECS energy loss is highest in case II, whereas it is lowest in case III.

V. CONCLUSION

A comparison between the circulating current suppression methods for parallel interleaved VSCs are presented in this paper. The use of the LCL harmonic filter is considered and it is designed to meet the harmonic injection limit specified by the BDEW. The values of the harmonic filter components are taken to be the same in all the cases. Models for evaluating the losses in the both active and passive components and the volume of the inductive components (converter-side inductor, step-up transformer, and CI) are derived. These models are used to carry out the multi-objective optimization of the inductive components, where the energy loss and volume of the inductive components are minimized. Several non-inferior design solutions are obtained and out of these non-inferior design solutions, a suitable design for each of the component is chosen such that the total volume of the inductive component is the same in all cases. For the given volume, the energy loss

in case I is highest. On the other hand, the CI is very effective in suppressing the circulating current and leads to the lowest energy losses in all the considered cases.

Multi-objective optimization has been carried out for the 3.45 MW, 690 V WECS with three parallel interleaved VSCs. The design parameters of the inductive components are chosen such that the total volume of the inductive components is the same (approximately 775 Ltr.) in all cases. Yearly energy loss in case III is 323.1 MWh, compared to 406.8 MWh and 428.7 MWh in case I and case II, respectively. As a result, the losses in the case III are 20.5% lower compared to the case I. The losses in both case I and case II can be reduced by using higher value of converter-side inductor than the required one. However, it may lead to sluggish transient response and should be avoided.

REFERENCES

[1] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 708–719, March 2012.

[2] B. Andresen and J. Birk, "A high power density converter system for the gamesa G10x 4,5 MW wind turbine," in *Proc. European Conference on Power Electronics and Applications*, Sept 2007, pp. 1–8.

[3] J. Birk and B. Andresen, "Parallel-connected converters for optimizing efficiency, reliability and grid harmonics in a wind turbine," in *Proc. European Conference on Power Electronics and Applications*, Sept 2007, pp. 1–7.

[4] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[5] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[6] H. Akagi, A. Nabae, and S. Atoh, "Control strategy of active power filters using multiple voltage-source PWM converters," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 3, pp. 460–465, 1986.

[7] R. Wagoner, A. Ritter, and A. Klodowski, "Wind turbine with parallel converters utilizing a plurality of isolated generator windings," Apr. 19 2011, US Patent 7,928,592. [Online]. Available: https://www.google.com/patents/US7928592

[8] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170.

[9] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[10] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[11] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved three-phase voltage source converters," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3400–3414, May 2016.

[12] P. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers,*, vol. 113, no. 8, pp. 1387–1394, August 1966.

[13] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Optimized integrated harmonic filter inductor for dual-converter fed open-end transformer topology," *IEEE Trans. Power Electron.*, [Online early access], DOI: 10.1109/TPEL.2016.2562679.