

Flux Balancing Scheme for PD Modulated Parallel Interleaved Inverters

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Abstract—A simple scheme to realize Phase-Disposition carrier Pulse Width Modulation (PD PWM) for parallel Two-Level Voltage Source Converters (2L-VSCs) is presented in this paper. The proposed implementation only uses a single carrier signal and can easily be implemented using a digital signal processor. The operation of the parallel VSCs with the Coupled Inductor (CI), under the PD PWM is briefly discussed and the associated dc flux injection problem is investigated. A CI saturation issue during the band transition under the PD PWM scheme is also explored and the strategy to avoid this problem is presented. In addition, the proposed strategy also maintains a volt-sec balance to synthesize desired reference space voltage vector during the band transition. As a result, a smooth transition from one modulation band to the other is ensured without causing disturbances in the line-to-line voltage. The switching losses and the harmonic performance of the proposed implementation are also compared with the commonly used Phase-Shifted carrier Pulse Width Modulation (PS PWM). The implementation issues are discussed and the experimental results are also presented.

Index Terms—Voltage source converters (VSC), parallel, interleaving, coupled inductor, pulse width modulation, PD modulation, phase disposition modulation, parallel inverters

I. INTRODUCTION

Three-phase Two-Level Voltage Source Converters (2L-VSC) are often connected in parallel to increase the current handling capability in the MW-level converter systems. The typical Silicon Insulated Gate Bipolar Transistors (Si-IGBT) that are used in such applications suffer from excessive losses if the switching frequency is increased beyond few kHz. As a result, large passive filter components are generally employed to comply with the stringent power quality requirements, which lead to increased cost, size and losses. Therefore the efforts are being made to reduce both the size of filter components and the switching frequency. One of the ways to achieve this contradictory requirements is to employ a multi-level VSC.

For the parallel connected 2L-VSCs, multi-level voltage waveforms can be achieved by a sequential switching of the parallel VSC legs. For example, four-level converter can be realized by the sequential switching of the three parallel 2L-VSCs, shown in Fig. 1. The Coupled Inductors (CIs) are used to suppress the circulating current that flows between the parallel VSCs due to the sequential switching. One of the ways to achieve the sequential switching is to use phase-shifted carrier signals [1]–[13]. Each of the 2L-VSC is independently modulated to synthesize the reference space voltage vector having a magnitude $|V_s^*|$ (normalized with respect to the dc-link voltage V_{dc}) and angle ψ_s . This scheme is commonly

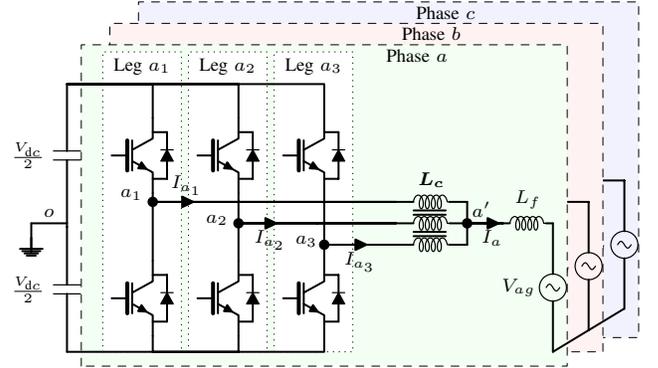


Fig. 1. Four-level converter, realized using three parallel two-level voltage source converters. A Coupled Inductor (CI) is used for suppressing the circulating current.

referred to as the Phase-Shifted Pulse Width Modulation (PS PWM) scheme.

In PS PWM, the carrier signals of the VSCs are symmetrically phase-shifted with an interleaving angle of $360^\circ/N$, where N is the number of VSCs. The switched output voltages of phase a under the PS PWM for $N = 3$ (for $|V_s^*| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$) are shown in Fig. 2(a), where T_i represents the dwell time of the i th voltage vector \vec{V}_i of the two-level VSC. By neglecting the resistance of the coils and the leakage flux, the resultant switched output voltage is given as (refer Appendix)

$$V_{x'o} = \frac{1}{N} \sum_{k=1}^N V_{x_k o} \quad (1)$$

where subscript x represents phases a , b , and c . $V_{x_k o}$ is the switched output voltage of phase x of k th VSC, where $k = \{1, 2, \dots, N\}$. The resultant switched output voltages of all the phases are also shown in Fig. 2(c), which demonstrate four-level voltage waveforms. The switching sequences 220–210–310–311–310–210–220 are employed, where each of the digit represents the voltage level of the resultant output voltage of the phase a , b and c , respectively (e.g. 210 represents that voltage levels of phase a , phase b , and phase c are level 2, level 1, and level 0, respectively).

For N parallel 2L-VSCs, the resultant switched output voltage $V_{x'o}$ has $(N+1)$ levels. For the three parallel VSCs, the V_s^* can be projected on the space vector diagram of the four-level converter, as shown in Fig. 3, where the reference space voltage vector is located in the triangle Δ_s . The harmonic profile of the synthesized voltage can be improved by using

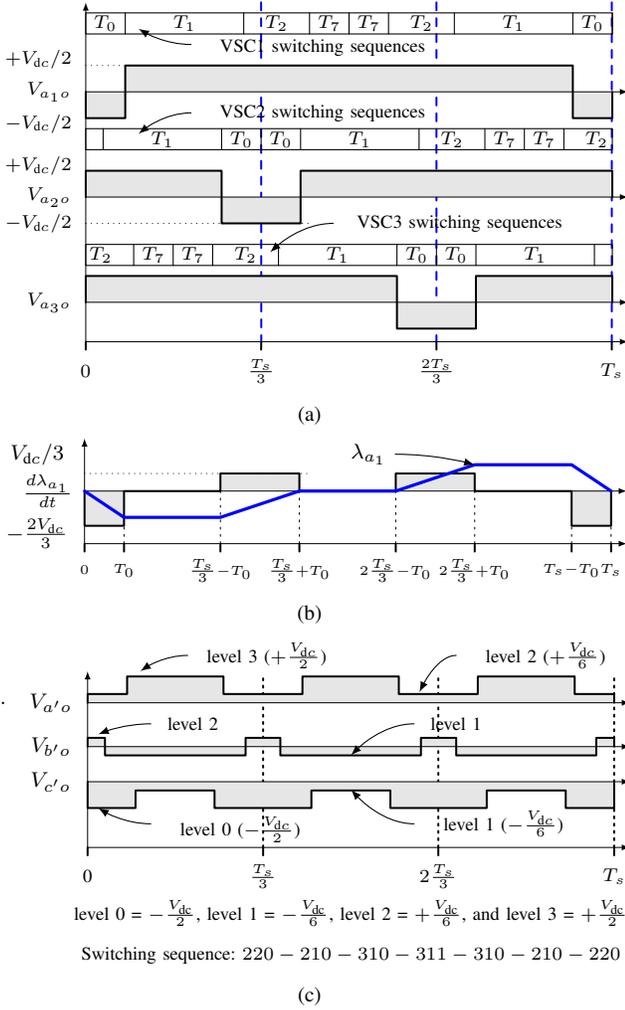


Fig. 2. Switched output voltages for $|V_s^*| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$. Each of the VSCs are modulated using two-level space vector modulation. T_0 , T_1 , T_2 , and T_7 represent the dwell time of the voltage state vectors \bar{V}_0 , \bar{V}_1 , \bar{V}_2 , and \bar{V}_7 , respectively. (a) Switched output voltage of phase a of all three VSCs, (b) Flux linking with the coil a_1 (λ_{a1}) of the CI, (c) Resultant switched output voltages of all three phases.

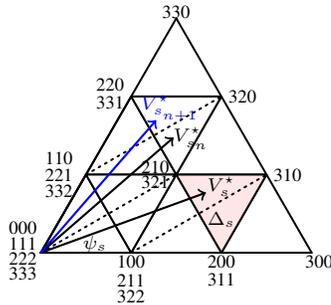


Fig. 3. Projection of the reference space voltage vector $V_s^* = 3\sqrt{3}/8\angle 20^\circ$ in the first sextant of the space vector diagram of the four-level converter.

the Nearest Three Vector (NTV) [14]–[16], which are located on the vertices of the triangle Δ_s (210-310-311). However, in PS PWM, symmetrically phase-shifted carrier signals are used to modulate individual VSCs and common offset voltage is added to the reference signals to align the active state vectors

in the center of the switching interval [14] for each of the VSCs so that the harmonic performance of the individual VSCs can be optimized. For the parallel VSCs, the resultant voltage is the average of the switched output voltages of the VSCs and the resultant switched output voltages of all three phases are shown in Fig. 2(c). By projecting them on the space vector diagram of the four-level VSC, it can be observed that the nearest three vectors (210 – 310 – 311) along with the additional voltage vector 220 are employed to synthesize the reference space voltage vector V_s^* . The use of the voltage vector other than the nearest three vectors deteriorates the harmonic performance. Therefore, it is evident that the PS PWM optimizes the harmonic performance of the individual VSCs but it is not an optimal solution for the modulation of the parallel VSCs.

An optimal PWM scheme to improve the harmonic performance of the parallel 2L-VSCs under the PS PWM is presented in [9]. The effect of the combination of the several switching sequences and the phase-shift between the carrier signals on the harmonic quality is investigated and optimal combination has been identified for all possible values of the $|V_s^*|$ and ψ_s . This information is then used to select the optimal combination of the switching sequences and the phase-shift during each sampling interval. Several combinations of the switching sequences and the phase-shift are used in one fundamental cycle. This would substantially increase the complexity and make it difficult to implement. Moreover, the CI could saturate during the transition from one combination to another.

For the multi-level converters, the use of the Phase Disposition carrier modulation (PD PWM) results in the lowest harmonic distortion [14], [17], [18] amongst other carrier modulation schemes. However, a conventional PD modulator can not be used for the parallel VSCs, as switching of all the parallel legs is not uniform and it could lead to the saturation of the CI. This issue is addressed in this paper. Moreover, a dc flux is injected during the transition from one modulation band to the other. The effect of the PD PWM on the operation of the CI is investigated and the band transition strategy to avoid the saturation of the CI is designed. A simple implementation using a Digital Signal Processor (DSP) is also proposed.

This paper is organized as follows. Section II describes the problems related to the use of the PD PWM for modulation of the parallel interleaved VSCs. The proposed scheme is then presented in Section III and the implementation using the DSP is discussed in Section IV. A comparative evaluation and performance verification through the experimental studies are included in Section V.

II. PD MODULATION OF THE PARALLEL INTERLEAVED VSCS AND ASSOCIATED ISSUES

In this section, the operating principle of parallel interleaved VSCs with the CI is briefly discussed and the issues related to the PD PWM of this converter are examined.

A. Operation of Parallel Interleaved VSCs

Parallel 2L-VSCs with a common dc-link is shown in Fig. 1 ($N = 3$ in this illustration). In this case, multi-level voltage

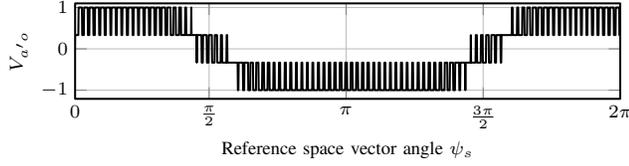


Fig. 4. Resultant switched output voltage of three parallel interleaved two-level voltage source converters. The voltage is normalized to half of the dc-link voltage $V_{dc}/2$.

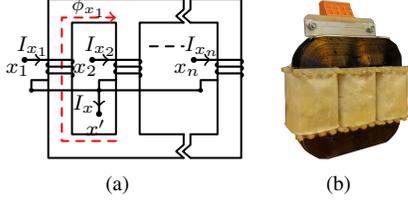


Fig. 5. (a) Magnetic structure of the coupled inductor that is used to suppress the circulating current between N parallel interleaved voltage source converters, (b) Photo of the realized coupled inductor for one of the phase for three parallel VSCs $N = 3$.

waveforms can be achieved by sequential switching of these VSCs, as shown in Fig. 4. The switched output voltages of the parallel legs of a given phase are shifted with respect to each other due to the sequential switching (cf. Fig. 2(a)) and would drive large circulating current between the parallel legs. The flow of this unwanted circulating current increases losses and demands unnecessary oversizing of the components present in the circulating current path. Therefore, the circulating current should be suppressed to some acceptable value to realize the full potential of the parallel interleaved VSCs.

The circulating current can be suppressed by introducing impedance in the circulating current path. This can be achieved by using single-phase (uncoupled) inductors. The uncoupled inductor offers inductance to both the resultant line current and the circulating current. In order to achieve reasonable suppression of the circulating current, high value of the inductance in the circulating current path is required. For the uncoupled inductor case this implies that the large inductance in the line current path is also present. This leads to significant voltage drop across the inductor due to the flow of the line current component, which is not desirable as it demands high dc-link voltage level. In addition, it also leads to slow transient response. On the other hand, CI offers high inductance to the circulating current component [1], [19]–[26], while its effect on the line current component is minimal (assuming negligible leakage flux). Therefore, the use of the CI is considered in this paper. However, the analysis and the proposed modulation scheme are also applicable to the parallel interleaved VSCs with uncoupled inductor.

The magnetic structure of the CI for N parallel VSCs is shown in Fig. 5(a). It consists of N magnetic limbs around which the coils are placed. All the coils are wound in the same direction and the limbs are magnetically coupled to each other using the top and bottom yokes. The start terminal of each of the coils is connected to the corresponding output terminal of the VSC legs, whereas the other terminal of all the coils

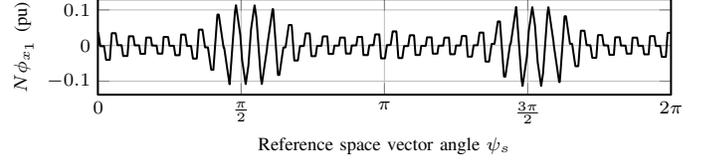


Fig. 6. Flux linkage in a fundamental frequency cycle when the phase-shifted carrier modulation is used to synthesize $|V_s^*| = 3\sqrt{3}/8$ for three parallel voltage source converters. The flux linkage is normalized with respect to $V_{dc}T_s$.

is connected together to the common point (x'), as shown in Fig. 5(a).

The resultant line current of a particular phase is the sum of all leg currents of that phase and it is given as

$$I_x = \sum_{k=1}^N I_{x_k} \quad (2)$$

For the parallel interleaved VSCs, the leg current I_{x_k} can be split into two components:

- 1) Component contributing to the resultant line current $I_{x_k,l}$
- 2) The circulating current $I_{x_k,c}$

and it can be represented as

$$I_{x_k} = I_{x_k,l} + I_{x_k,c} \quad (3)$$

The circulating current components $I_{x_k,c}$ only flows between the parallel VSCs and do not contribute to the resultant line current. Therefore, (2) can be re-written as

$$I_x = \sum_{k=1}^N I_{x_k,l} \quad (4)$$

Assuming an equal line current sharing between the parallel VSCs, the common component of the leg current is obtained as $I_{x_k,l} = I_x/N$. With this assumption and neglecting the leakage flux, the flux that links with k th coil is given as [12]

$$\phi_{x_k}(t) = \frac{1}{N_{CI}} \left(\frac{N-1}{N} \int V_{x_{k0}} dt - \frac{1}{N} \sum_{\substack{j=1 \\ j \neq k}}^N \int V_{x_{j0}} dt \right) \quad (5)$$

where N_{CI} is the number of turns in each of the coils. The flux linking with the coil can be obtained using (5). For $N = 3$, the flux linking with the coil x_1 of the CI under PS PWM for one switching cycle is shown in Fig. 2(b). The CI is subjected to the switching frequency flux excitation as shown in Fig. 6, where the flux linkage over a fundamental frequency cycle is depicted. The peak amplitude of the flux linkage is different in every switching cycle due to the change in the dwell times of the voltage vectors due to the variation in the space voltage vector angle ψ_s . The maximum value of the peak flux linkage is independent of the load and only depends on the dc-link voltage, switching frequency, and the modulation scheme. The maximum value of the peak flux linkage occurs at $\psi_s = 90^\circ$ and $\psi_s = 270^\circ$ and it is given as [12]

$$N_{CI}\phi_{a_k, max} = \frac{V_{dc}}{9f_c}, \quad \forall M \quad (6)$$

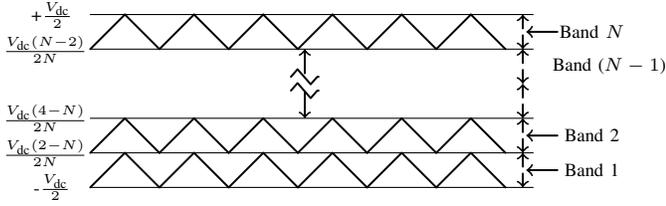


Fig. 7. Arrangement of the carrier signals in the conventional phase disposition modulation scheme [14].

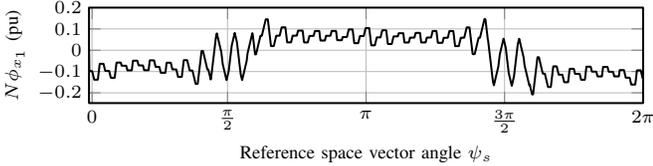


Fig. 8. Flux linkage in a fundamental frequency cycle when the PD PWM with an even commutation distribution proposed in [27] is used to synthesize $|V_s^*| = 3\sqrt{3}/8$. The flux linkage is normalized with respect to $V_{dc}T_s$.

In order to prevent the oversizing (or to avoid the saturation) of the CI, the operation of the CI under flux balance condition, i.e. with zero dc flux component must be ensured. The natural flux balancing is obtained when PS PWM is used to modulate the parallel VSCs [12], as shown in Fig. 6. As evident from Fig. 6, the dc flux component is absent. However, this is not the case when PD PWM is employed and the related issues are discussed in the following subsection.

B. Coupled Inductor Saturation Under PD PWM

The PD PWM of N parallel VSCs is realized by arranging N carrier signals, which are in phase and level-shifted in order to occupy the linear modulation range, as shown in Fig. 7. In the conventional PD PWM implementation, each carrier signal is responsible for the modulation of one of the legs (i.e. carrier that spans in band k would be responsible for the modulation of leg k). This would introduce a dc flux injection and would saturate the CI. The similar problem has been observed in the Flying Capacitor (FC) multi-level converter, where the conventional PD PWM implementation would lead to a capacitor voltage unbalance. Several strategies have been proposed to ensure natural voltage balancing of PD modulated FC multi-level converter [27]–[30]. Even though these schemes can ensure even commutation distribution between the parallel VSCs, dc flux injection still happens during the band transition, as shown in Fig. 8. Therefore, these schemes can not be readily applicable to the parallel VSCs.

The enhanced modulator for the parallel interleaved 2L-VSCs is proposed in [31]. It uses two sets of the evenly phase-shifted carrier signals that are dynamically allocated using multiplexer, which makes it difficult to implement. Moreover, this implementation is equivalent to the PD PWM and CI saturation during the band transition could still happen. The PD carrier modulation scheme for the two parallel VSCs is presented in [32]. It uses a state machine to select the switching states. However, the complexity in this case increases with the increase in the number of parallel VSCs.

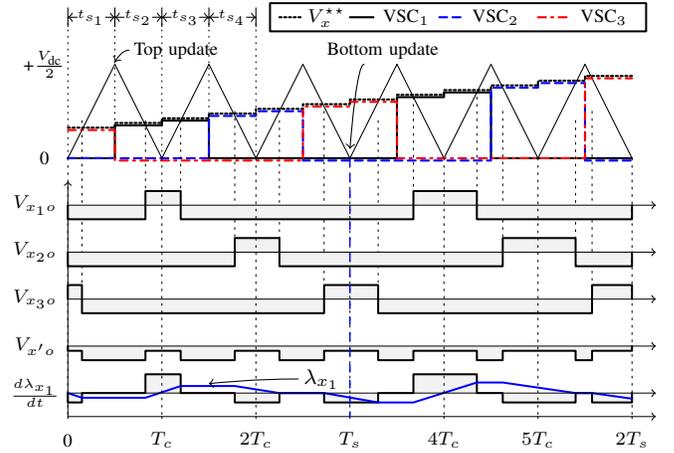


Fig. 9. Phase disposition modulation using the carrier comparison and the associated switched voltages waveforms when the command reference signal lies in Band 1. Solid blue line represents the flux linkage of coil x_1 .

The strategy to avoid the CI saturation during the transition from the positive value of the command reference signal to the negative value of the command reference signal and vice-versa has been proposed for the two parallel VSCs. However, it does not ensure volt-sec balance to synthesize V_s^* during the band transition and introduces a disturbance in the line-to-line voltage of the three-phase system, which is highly undesirable.

A PWM scheme to ensure an even commutation distribution between the parallel VSCs is presented in this paper. The strategy ensures flux balancing in the CI and the volt-sec balance to synthesize the reference voltage space vector V_s^* , even during the band transition.

III. MODULATION ALGORITHM

In the proposed implementation, a single carrier is used with the frequency of $f_c = N \times f_{sw}$, where f_{sw} is the switching frequency of each of the VSCs, i.e. for three parallel VSCs, the carrier frequency is three times the switching frequency of each of the VSCs. The amplitude of the carrier signal is taken to be $+V_{dc}/2$ (which occupies the region from 0 to $+V_{dc}/2$). An appropriate processing and scaling of the command reference signals (V_a^* , V_b^* , V_c^*) are first performed to accommodate the modified reference signals in the carrier region spanning from 0 to $+V_{dc}/2$ and it is obtained as

$$V_x^{**} = \frac{N}{2} \text{mod}\left(\left(V_x^* + \frac{V_{dc}}{2}\right), \frac{V_{dc}}{N}\right) \quad (7)$$

where mod is a function and it returns the remainder after a division. The band in which the reference signal is located can be obtained by using the ceiling function as

$$B_x = \left\lceil \frac{V_x^* + \frac{V_{dc}}{2}}{\frac{V_{dc}}{N}} \right\rceil \quad (8)$$

A. Modulation Under Steady-state Conditions

The steady-state condition refers to the case when the band in which the reference signal is located is the same in the current (n th) sampling interval and previous ($n-1$)th sampling

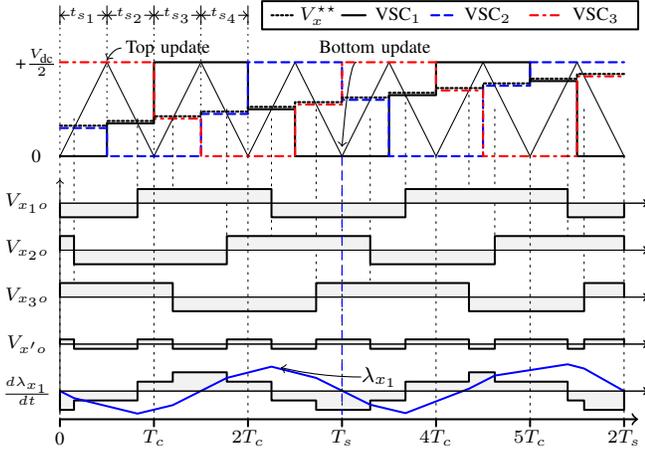


Fig. 10. Carrier comparison and the associated switched voltages waveforms when the command reference signal is located in Band 2. Solid blue line represents the flux linkage of coil x_1 .

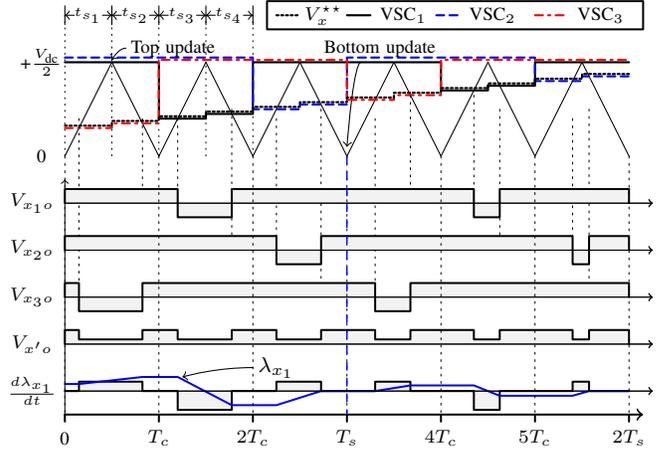


Fig. 11. Carrier comparison and the associated switched voltages waveforms when the command reference signal is located in band 3. Solid blue line represents the flux linkage of coil x_1 .

interval. The parallel VSCs are modulated to achieve the $(B_x - 1)$ and B_x voltage levels by taking into account the information of the band in which the command reference signal is located.

1) *Modulation in Band 1*: The VSCs are switched in a round-robin manner. During each sampling interval, the VSCs are categorized as:

- 1) Active VSC: which is being switched in a given sampling interval.
- 2) Passive VSCs: remaining $(N - 1)$ VSCs, which are latched to the previous switching state.

The modified reference V_x^{**} is used for the carrier comparison of the active VSCs, whereas the zero value is used for the passive VSCs. The proposed PWM scheme is exemplified by considering the case of three parallel VSCs ($N = 3$). However, the same procedure can be applied to N parallel VSCs.

The carrier comparison scheme and the associated switched output voltages for three parallel VSCs are shown in Fig. 9. In the sampling interval t_{s1} , VSC₃ is an active VSC and VSC₁ and VSC₂ are the passive VSCs. Similarly in the interval t_{s2} and t_{s3} , VSC₁ is an active VSC and VSC₂ and VSC₃ are termed as the passive VSCs. The state of each of the VSCs remain active for two consecutive sampling intervals $(N - 1)$ consecutive sampling intervals for N VSCs). The transition from the active state to the passive state for each of the VSCs happens at the top update, as shown in Fig. 9.

The resultant switched output voltage $V_{x'o}$ has a transition from voltage level 0 to voltage level 1 and vice-versa during each switch transition, as shown in Fig. 9. Even commutation distribution is ensured thanks to the sequential switching of the parallel VSCs. Therefore, the dc flux component in the CI during the steady-state is avoided, which is evident from the flux linkage waveform of the coil x_1 (λ_{x1}), shown in Fig. 9.

2) *Modulation in Band 2*: The carrier comparison of the parallel VSCs in band 2 and the associated switched output voltages are shown in Fig. 10. Each of the VSCs remains in the active state for only one sampling interval, followed by the passive state in the next two consecutive sampling intervals. In a given sampling interval, the modified reference V_x^{**} is used

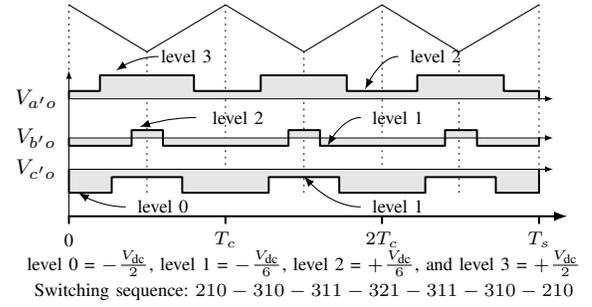


Fig. 12. Resultant switched output voltages for $|V_s^*| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$ with the proposed implementation.

for the carrier comparison of the active VSCs, whereas zero and $+V_{dc}/2$ are used for the carrier comparison of the passive VSCs, as shown in Fig. 10. For example, in the sampling interval t_{s1} , V_x^{**} is used for the carrier comparison for VSC₂ (active VSC), whereas zero and $+V_{dc}/2$ are used for the VSC₁ and VSC₃, respectively. During the top update, the state of the passive VSC with the zero compare value is changed to active state (and vice-versa), whereas the state of the passive VSC with the $+V_{dc}/2$ compare value is changed to the active state (and vice-versa) at the bottom update.

3) *Modulation in Band 3*: The operation in band 3 is similar to the operation in band 1. The only difference is that the value assigned to the passive VSCs for the carrier comparison is $+V_{dc}/2$ (whereas it was zero in band 1) and the transition from active state to passive state for each of the VSCs happens at the bottom update, as shown in Fig. 11.

The resultant switched output voltages of all the three phases for $V_s^* = 3\sqrt{3}/8 \angle 20^\circ$ are shown in Fig. 12. The switching sequences 210-310-311-321 are used, which are the nearest three vectors, as shown in Fig. 3. As a result, compared to PS PWM, significant improvement in the harmonic quality of the voltage waveforms can be achieved. Moreover, the balance between the positive and negative volt-sec for the CI during a switching period is also maintained in the steady-state operation. This is achieved by the sequential switching

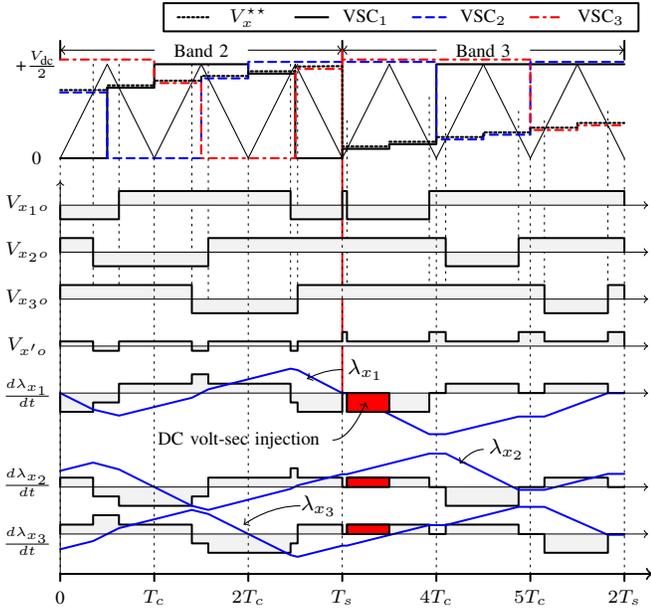


Fig. 13. DC voltage injection during the transition from the band 2 to the band 3. Solid blue lines represent the flux linkages. The volt-sec that introduces the dc flux component is shown by the red rectangular block.

of the VSCs. As a result, the CI only experiences switching frequency flux excitation and the dc component in the flux is zero during the steady-state. However, the positive and negative volt-sec is not balanced within a switching period that follows the band transition, as shown in Fig. 13, where the transition from the band 2 to band 3 is illustrated. The dc volt-sec is injected during the first sampling interval that follows the band transition. This may lead to the saturation or unnecessary oversizing of the CI. The flux balancing scheme to avoid this problem is discussed hereafter.

B. Modulation Under Band Transition

$2(N-1)$ band transition instances are encountered in every fundamental cycle for N parallel VSCs (assuming that the modulation index is high enough). For three parallel VSCs, four band transitions instances are:

- Transition from band 1 to band 2 and vice-versa.
- Transition from band 2 to band 3 and vice-versa.

1) *Transition from band 2 to band 3*: The flux balancing scheme is illustrated for the case in which the transition happens from band 2 to band 3. However, the same strategy can be applied to the remaining cases as well. As shown in Fig. 13, the dc volt-sec is injected during the first sampling interval after the band transition. This will introduce dc component in the flux and may lead to CI saturation. Therefore, in the proposed scheme, the band transition events are detected and additional commutations are introduced in a very first sampling interval that follows the band transition event. This additional commutations are required to ensure that the positive and negative volt-secs are balanced during that sampling interval. As a result, the dc flux component is ensured to be zero and the CI saturation is avoided.

TABLE I
TRANSITION FROM BAND 2 TO BAND 3 AT BOTTOM UPDATE (BU) (BAND TRANSITION DETECTION AT TOP UPDATE): VALUES USED FOR THE CARRIER COMPARISON IN THE $n+1$ TH SAMPLING INTERVAL.

Leg	Leg b_1 (VSC $_{b1L} = 2$)		Leg b_2 (VSC $_{b2L} = 3$)		Leg b_3 (VSC $_{b3L} = 1$)	
	OFF	ON	OFF	ON	OFF	ON
Values	$\frac{V_{dc}+V_b^{**}}{3}$	$\frac{V_{dc}+4V_b^{**}}{6}$	V_b^{**}	$\frac{V_{dc}+V_b^{**}}{3}$	$\frac{V_{dc}+4V_b^{**}}{6}$	

The switching sequences that should be used to synthesize V_s^* depend on the carrier signal, as shown in Fig. 12. For example, in the sampling interval during which the carrier signal rises from 0 value to $V_{dc}/2$ (sampling interval that follows the Bottom Update (BU)), switching sequences 321 – 311 – 310 – 210 are employed, whereas switching sequences 210 – 310 – 311 – 321 are used during the sampling interval when the carrier signal falls from $V_{dc}/2$ to 0 (sampling interval that follows the top update (TU)). Therefore the band transition strategy also takes into account the TU and BU. For example, in order to synthesize $|V_s^*| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$, the voltage level of the phase a should be two at the top update (to realize 210 – 310 – 311 – 321) whereas it should be three at the bottom update (to realize 321 – 311 – 310 – 210) (refer Fig. 12 and Fig. 13).

a) *Band Transition at Bottom Update*: The instant when the transition from the band 2 to the band 3 occurs for the phase b is shown in Fig. 3, where $V_{s_n}^*$ represents the sampled reference space vector just before the transition and $V_{s_{n+1}}^*$ is the sampled reference space vector for the next sampling interval, which occurs just after the transition. The pivot vector changes from 210/321 to 220/331 during band transition. So if the transition occurs at the bottom update, the switching sequence in the $n+1$ th sampling interval (first sampling interval after the transition) should be 331 – 321 – 320 – 220.

The strategy for the band transition occurring at the bottom update is shown in Fig. 14. It is important to note that the delay of one sampling interval exists due to the digital modulator, i.e. the band transition in the reference signal is detected at the top update (during n th sampling interval). The dc flux injection in the $(n+1)$ th sampling interval is avoided by introducing an extra commutation in two legs (leg b_2 and leg b_3 as shown in Fig. 14). The magnified version of the $(n+1)$ th sampling interval is shown in Fig. 14(b). The values for the carrier comparison and the switching logic are given in Table I. This ensures that the volt-sec balance is maintained to synthesize the sampled reference space vector V_s^* . As shown in Fig. 14(b), all three legs are turned on at the start of the sampling interval for the duration of $\frac{V_b^{**}}{V_{dc}}T_c$, where T_c is the time period of the carrier signal. As a result, voltage level 3 is achieved for the desired time duration. The remaining duration of the sampling period $\frac{V_{dc}-2V_b^{**}}{2V_{dc}}T_c$ is divided into three equal intervals and the parallel legs are sequentially turned off for the duration of $\frac{V_{dc}-2V_b^{**}}{6V_{dc}}T_c$ each, to achieve the voltage level 2. The resultant switched output voltages of the phase a and phase c are also shown in Fig. 14, which demonstrates that the nearest three vectors are used during the $(n+1)$ th sampling interval. As a result, a disturbance in the line-to-line voltage

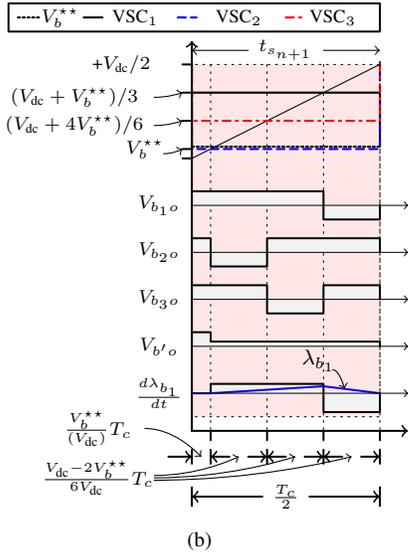
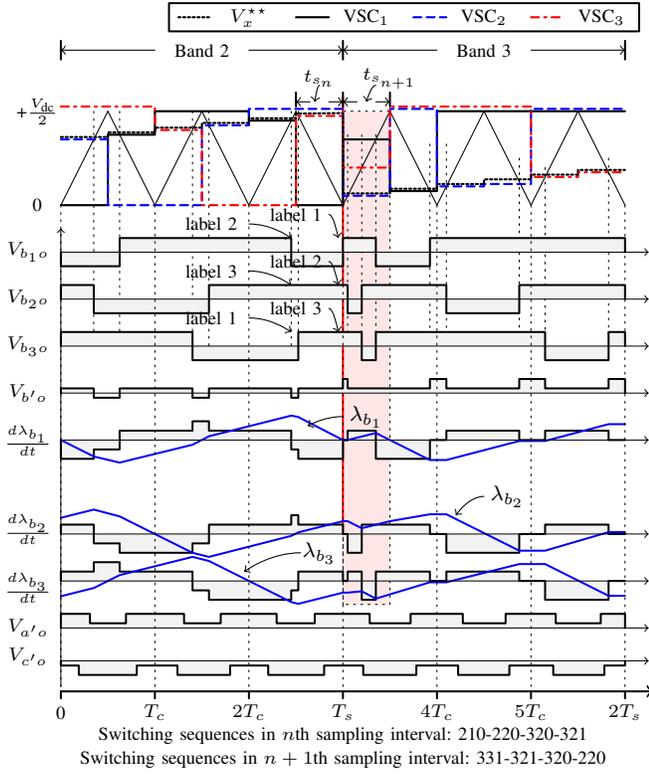
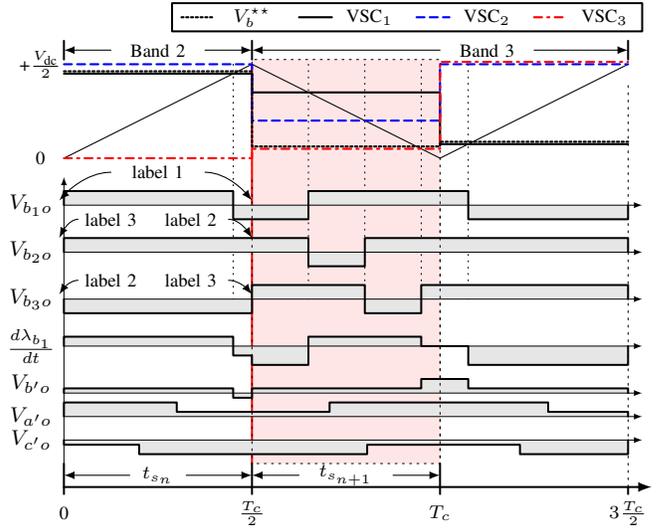


Fig. 14. Flux balancing strategy for the band transition that occurs at the bottom update (and the band transition is detected one sampling cycle before the actual transition happens). Solid blue lines represent the flux linkages.

is avoided.

The flux linkage associated with each of the coils of the phase b is also shown in Fig. 14. During the $(n+1)$ th sampling interval, positive dc voltage of $V_{dc}/3$ appears for the interval of $\frac{V_{dc}-2V_b^{**}}{3V_{dc}}T_c$, which has been balanced by the negative voltage of $2V_{dc}/3$ with duration $\frac{V_{dc}-2V_b^{**}}{6V_{dc}}T_c$. As a result, the dc flux injection in the $(n+1)$ th sampling interval is assured to be zero. From the $(n+2)$ nd sampling interval onwards, all the VSCs operate in steady-state in modulation



Switching sequences in n th sampling interval: 321-320-220-210
Switching sequences in $n+1$ th sampling interval: 220-320-321-331

Fig. 15. Flux balancing strategy for the band transition occurring at the top update.

TABLE II
TRANSITION FROM BAND 2 TO BAND 3 AT TOP UPDATE (TU) (BAND TRANSITION DETECTION AT BOTTOM UPDATE): VALUES USED FOR THE CARRIER COMPARISON IN THE $n+1$ ST SAMPLING INTERVAL.

Leg	Leg b_1 (VSC $_{b1L} = 1$)	Leg b_2 (VSC $_{b2L} = 3$)	Leg b_3 (VSC $_{b3L} = 2$)
	ON	ON	ON
	OFF	OFF	OFF
Values	$\frac{V_{dc}+V_b^{**}}{3}$	$\frac{V_{dc}+4V_b^{**}}{6}$	$\frac{V_{dc}+V_b^{**}}{3}$
	V_b^{**}	$\frac{V_{dc}-2V_b^{**}}{6}$	$\frac{V_{dc}+4V_b^{**}}{6}$

band 3. The sequences in which VSC legs are switched in band 3 ($(n+2)$ nd sampling interval onwards) is decided based on the information of the active and passive VSCs in the n th sampling interval.

Same approach can be applied during the transition from band $(N-1)$ to band N for N number of parallel VSCs. All legs should be turned on at the start of the sampling interval for the duration of $\frac{V_b^{**}}{V_{dc}}T_c$, whereas they should be sequentially turned off for the duration of $\frac{V_{dc}-2V_b^{**}}{2NV_{dc}}T_c$.

b) Band Transition at Top Update: In this case, all the VSC legs corresponding to phase b are switched to obtain the voltage level 2 at the start of the $(n+1)$ th sampling interval, whereas level 3 is obtained at the end, as shown in Fig. 15. The values that are used for the carrier comparison are given in Table II. The flux balancing is maintained and the nearest three vectors are used to synthesize the reference space voltage vector.

2) Transition in Other Cases: The strategy that is used for the transition from band 2 to band 3 is also applied to other cases as well. The values used for the carrier comparison in $(n+1)$ th sampling interval in case of the transition from the band 3 to the band 2, from the band 2 to the band 1, and from band 1 to the band 2 are given in Table III, Table IV, and Table V, respectively.

TABLE III
TRANSITION FROM BAND 3 TO BAND 2: VALUES USED FOR THE CARRIER COMPARISON IN THE $n+1$ TH SAMPLING INTERVAL.

Leg	Leg b_1		Leg b_2		Leg b_3	
	OFF (BU) /ON (TU)	ON	OFF	ON	OFF	ON
BU	$\frac{V_{dc}+2V_x^{**}}{3}$	$\frac{V_{dc}+2V_x^{**}}{6}$	$\frac{4V_x^{**}-V_{dc}}{6}$	$\frac{4V_x^{**}-V_{dc}}{6}$	$\frac{V_x^{**}}{3}$	$\frac{4V_x^{**}-V_{dc}}{6}$
TU	$\frac{V_{dc}+2V_x^{**}}{3}$	$\frac{4V_x^{**}-V_{dc}}{6}$	$\frac{V_{dc}+2V_x^{**}}{3}$	V_x^{**}	$\frac{4V_x^{**}-V_{dc}}{6}$	$\frac{4V_x^{**}-V_{dc}}{6}$

TABLE IV
TRANSITION FROM BAND 2 TO BAND 1: VALUES USED FOR THE CARRIER COMPARISON IN THE $n+1$ TH SAMPLING INTERVAL.

Leg	Leg b_1		Leg b_2		Leg b_3	
	OFF (BU)/ON (TU)	ON	OFF	ON	OFF	ON
BU	$\frac{V_x^{**}}{3}$	$\frac{2V_x^{**}}{3}$	$\frac{V_x^{**}}{3}$	$\frac{2V_x^{**}}{3}$	$\frac{V_x^{**}}{3}$	$\frac{2V_x^{**}}{3}$
TU	$\frac{V_x^{**}}{3}$	$\frac{2V_x^{**}}{3}$	$\frac{V_x^{**}}{3}$	V_x^{**}	$\frac{2V_x^{**}}{3}$	$\frac{2V_x^{**}}{3}$

TABLE V
TRANSITION FROM BAND 2 TO BAND 1: VALUES USED FOR THE CARRIER COMPARISON IN THE $n+1$ TH SAMPLING INTERVAL.

Leg	Leg b_1		Leg b_2		Leg b_3	
	OFF (BU) /ON (TU)	ON	OFF	ON	OFF	ON
BU	$\frac{V_{dc}+2V_x^{**}}{6}$	$\frac{V_{dc}+2V_x^{**}}{6}$	$\frac{V_{dc}+2V_x^{**}}{3}$	$\frac{V_{dc}+2V_x^{**}}{3}$	$\frac{V_x^{**}}{3}$	$\frac{V_{dc}+2V_x^{**}}{3}$
TU	$\frac{V_{dc}+2V_x^{**}}{6}$	$\frac{V_{dc}+2V_x^{**}}{3}$	$\frac{V_{dc}+2V_x^{**}}{6}$	V_x^{**}	$\frac{V_{dc}+2V_x^{**}}{3}$	$\frac{V_{dc}+2V_x^{**}}{3}$

IV. IMPLEMENTATION OF THE PROPOSED MODULATION

The algorithm for the operation under the steady-state condition for three parallel VSCs is shown in Fig. 16. Each of the VSC legs is labeled using the variable VSC_{xk_L} , where subscript x represents one of the phases ($x = \{a, b, c\}$) and subscript k represents VSC ($k = \{1, 2, 3\}$). The VSC label VSC_{xk_L} takes any integer value from one to three. This label is used to determine the sequence in which the VSC legs are switched. i.e. VSC leg with label one ($VSC_{xk_L} = 1$) is termed as an active VSC and it is always switched in a given sampling interval, whereas the VSC legs with label two and label three are clamped either to the positive dc bus or to the negative dc bus. The VSC leg is clamped to the positive dc bus by setting the value used for the carrier comparison equal to $V_{dc}/2$ ($CMPR_{xk} = V_{dc}/2$), whereas zero value is used to clamp the VSC leg to the negative dc bus ($CMPR_{xk} = 0$). During the steady-state operation, the active VSC, i.e. the VSC leg with the label equal to one ($VSC_{xk_L} = 1$) is assigned V_x^{**} for the carrier comparison ($CMPR_{xk} = V_x^{**}$). The label of each of the VSCs has been updated at specific intervals to realize the desired operation. For example, during the steady-state operation in band 3, the label of each of the VSC leg is incremented in the Interrupt Service Routine (ISR) occurring at the top update, whereas labels are kept as it is during the ISR occurring at the bottom update. This VSC label information is then used to determine the values for the carrier comparison for the modulation of the corresponding VSC legs, as shown in Fig. 16.

The flow chart, explaining the flux balancing scheme during the band transition is shown in Fig. 17. Only the case in which the transition happens from band 2 to band 3 is shown.

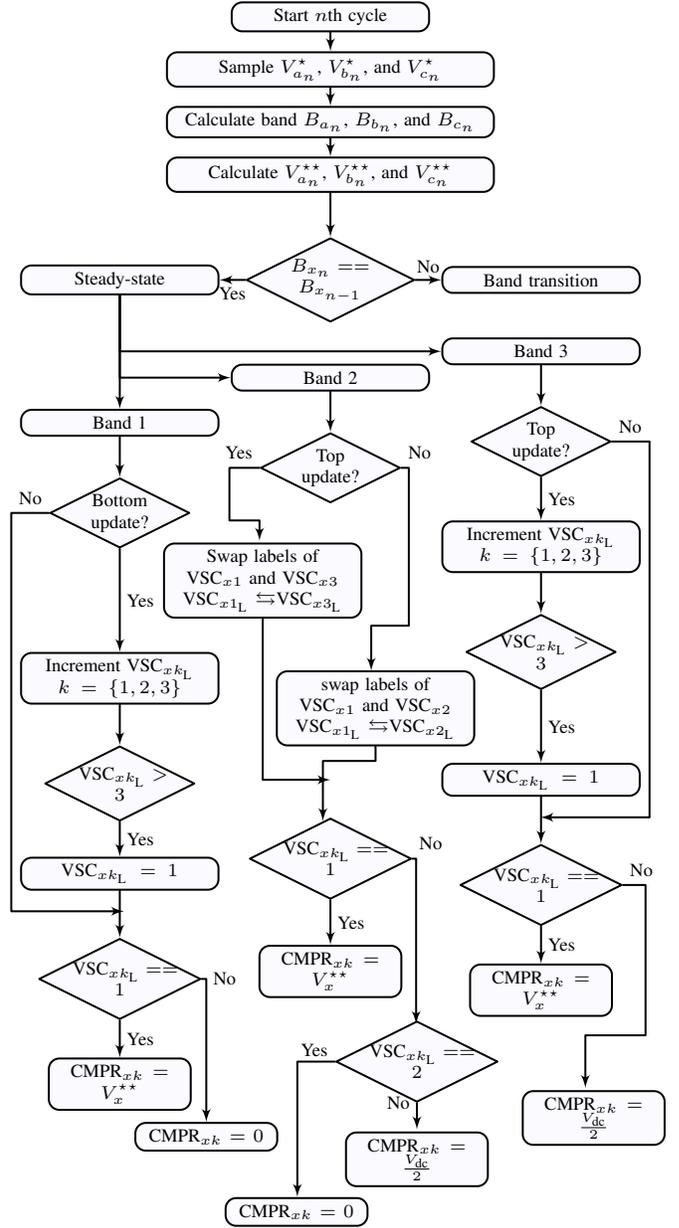


Fig. 16. Flow chart of the proposed modulation scheme. The operation under steady-state is described. Subscript k represents the voltage source converter number ($k = \{1, 2, 3\}$). Subscript x represents the phases $a, b,$ and c ($x = \{a, b, c\}$). The sequence in which the legs are switched is represented by label VSC_{xk_L} , where VSC_{xk_L} is the label of the k th leg of the phase x . VSC leg with label 1 ($VSC_{xk_L} = 1$) is switched, whereas VSC legs with label two and label three are clamped to either positive dc bus or negative dc bus. $CMPR_{xk}$ represents the value that is used for the carrier comparison for the k th leg of the phase x .

However, the same procedure is followed in other cases as well. The switching logic and the values for the carrier comparison in the $(n+1)$ th sampling interval is determined based on the following:

- 1) Whether the transition happens at the top update or at the bottom update.
- 2) Label of the VSC before the start of the n th sampling interval.

The carrier comparison logic, which is reversed for some of

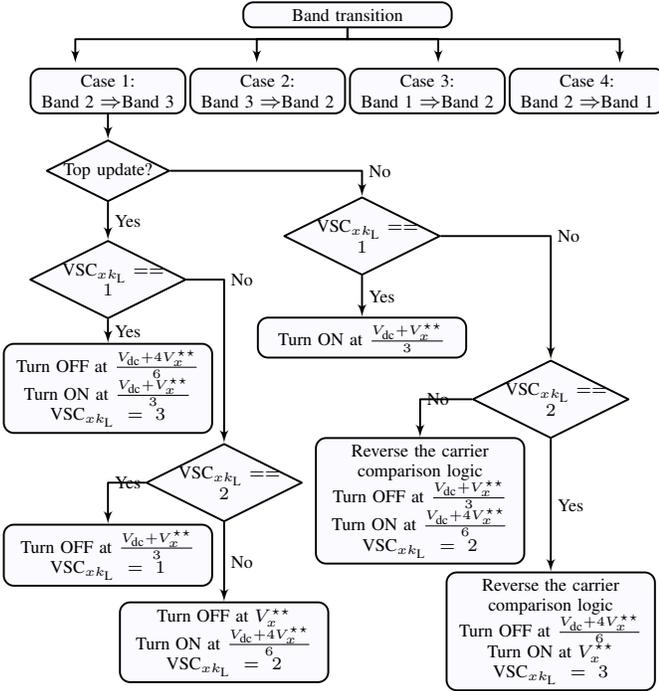


Fig. 17. Flow chart for the proposed flux balancing scheme during the band transition. The scheme for the transition from band 2 to band 3 is only discussed. Refer Fig. 14 and Fig. 15 for the graphical explanation.

the VSCs during the n th sampling interval, is restored back to the original during the $(n + 1)$ st sampling interval. The label information of each of the VSCs is used to ensure a proper transition from one band to the another, as shown in Fig. 17 (refer Fig. 14 and Fig. 15 for the graphical explanation).

V. COMPARATIVE EVALUATION AND RESULTS

The proposed scheme implements PD PWM of the parallel VSCs. The use of the PD PWM results in a superior harmonic performance compared to the PS PWM. However, additional commutations are introduced in the proposed implementation to ensure the flux balancing during the band transition. As a result, for the same carrier frequency, the switching losses in the proposed implementation would be slightly more compared to that in the case of the PS PWM. Therefore, the harmonic performances of both the proposed scheme and the PS PWM are evaluated under a constant switching loss condition.

A. Semiconductor Losses

Time domain simulations have been carried out using PLECS to calculate the semiconductor losses. A 3.45 MW, 690 V converter system with three parallel VSCs is considered as an example system. The 1700 V, 1000 A IGBT with anti-parallel diode from Infineon (FF1000R17IE4) is considered. The conduction losses of the IGBT and the diodes, the turn-on and turn-off losses of the IGBTs and the recovery losses of the diodes are calculated using the parameters given in the datasheet. The dc-link voltage is set to be 1100 V. The effects of the junction temperature on the losses is also considered,

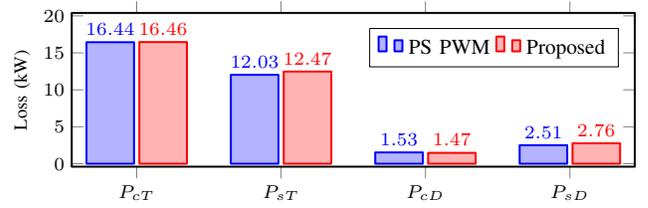


Fig. 18. Total semiconductor losses in the case of the PS PWM and the proposed scheme evaluated at the full load condition with the power factor of one. Switching frequency is 1.65 kHz in both cases. P_{cT} , P_{sT} , P_{cD} , and P_{sD} are the IGBT conduction losses, IGBT switching losses, diode conduction losses, and diode switching losses, respectively.

where the junction-to-case thermal behavior of the IGBTs and the diodes are modeled using the Foster network representation of the thermal equivalent circuit. The case temperature is assumed to be constant at 60°C.

The semiconductor losses are evaluated at full load conditions with a displacement power factor of one. The modulation index is also set to be one. The carrier frequency is taken to be $f_c = 3 \times 1650$ Hz for the proposed scheme. Three 120° phase-shifted carrier signals with the carrier frequency of 1650 Hz are used for the PS PWM. The total semiconductor losses (of all three VSCs) in both the cases are shown in Fig. 18. The conduction losses in both the cases are almost the same, whereas the switching losses in the case of the proposed scheme are slightly higher than that of the PS PWM, as expected due to the additional commutations during the band transition. The switching losses in the IGBTs are higher by 0.47 kW, whereas the switching losses in the diodes are higher by 0.25 kW.

The switching losses in the proposed modulation scheme varies with the displacement power factor angle. The ratio of the switching losses in the proposed PWM scheme to the switching losses in the PS PWM is denoted as α_{sw} and it is evaluated for a modulation index of one. The variation of α_{sw} with displacement power factor angle is shown in Fig. 19. For the application in which the power factor is close to unity, the increase in the switching losses due to the use of the proposed PWM scheme is minimal. However, the switching losses in the proposed PWM scheme increases as the displacement power factor angle approaches $\pm 90^\circ$. It is also important to note that the α_{sw} decreases with the increase in the carrier frequency and in the medium/high switching frequency applications it becomes negligible as shown for $f_c = 3 \times 10$ kHz in Fig. 19.

For N parallel VSCs, maximum number of band transition instances in a fundamental cycle are $2(N - 1)$. Additional commutations are introduced to avoid CI saturation during every band transition. Therefore, α_{sw} increase with increase in the number of parallel VSCs.

B. Harmonic Performance

In order to evaluate the harmonic performance under the constant loss conditions for the applications in which the power factor varies in vicinity of one, the carrier frequency in the case of the PS PWM is increased to 1700 Hz. The command reference signals for the phase voltages (V_x^*) are

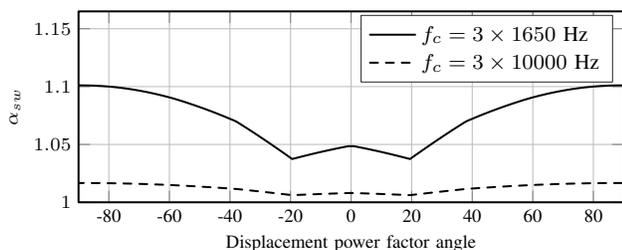


Fig. 19. Switching loss comparison with the rated load and modulation index of one. α_{sw} is the ratio of the switching losses in the proposed PWM scheme to the switching losses in the PS PWM.

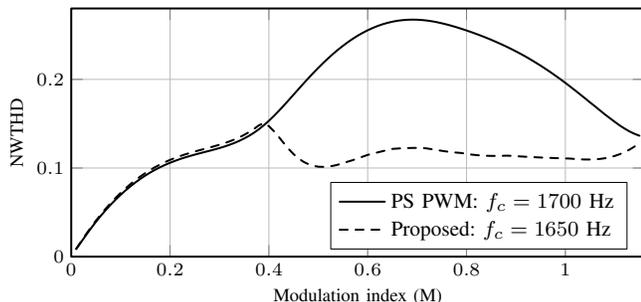


Fig. 20. Harmonic performance of the PS PWM and the proposed scheme, evaluated under the constant loss condition for the full load unity power factor application.

obtained by adding common mode offset in the sinusoidal phase voltages (V_a , V_b , and V_c) and it is given as

$$V_x^* = V_x - 0.5[\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)] \quad (9)$$

The harmonic performances of both schemes are compared by evaluating the Normalized Weighted Total Harmonic Distortion (NWTHTD) of the line-to-line voltage, which is defined as

$$\text{NWTHTD} = \frac{M}{V_f} \sqrt{\sum_{h=2}^{1000} (V_h/h)^2} \quad (10)$$

where M is the modulation index and it is defined as the ratio of the amplitude of the reference phase voltage (V_x) to the half of the dc-link voltage. V_f is the fundamental component of the line-to-line voltage, whereas V_h is the magnitude of the h th harmonic component of the line-to-line voltage.

The NWTHTD over the full modulation range is shown in Fig. 20. As the proposed scheme realizes the PD PWM, it demonstrates a better harmonic performance over a wide modulation indices region ($0.4 \leq M \leq 2/\sqrt{3}$). For the grid connected applications, where the converters typically operates with a modulation index in vicinity of one, the use of the proposed scheme results in 44% reduction in the NWTHTD compared to the PS PWM (at $M = 1$). The PS PWM is marginally better than the proposed scheme at lower modulation index due to the higher carrier frequency (constant loss condition).

C. Core Losses in Coupled Inductor

Core losses in the CI are evaluated for both the schemes. The CI is designed for 3.45 MW, 690 V converter system with

TABLE VI
DESIGN PARAMETERS OF THE COUPLED INDUCTOR

Parameters	Values
Effective cross-section area of core A_c	$4.6 \times 10^{-3} \text{ m}^2$
Number of turns N_{CI}	16
Cross section area of conductor A_{cu}	$292 \times 10^{-6} \text{ m}^2$
Core volume v_c	$7.36 \times 10^{-3} \text{ m}^3$

TABLE VII
SYSTEM PARAMETERS.

Parameters	Values
Power	15 kW
No. of parallel VSCs	Three (5 kW each)
DC link voltage	700 V
Line filter inductor L_f	0.6 mH
Circulating current inductance L_c	30 mH

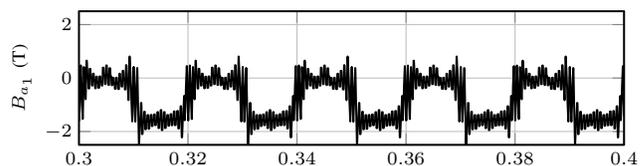


Fig. 21. Simulation results. The parallel VSCs are switched sequentially without flux balancing control. DC voltage is injected during band transition, which introduces dc flux and leads to CI saturation.

three parallel VSCs. Using (5), the maximum value of the flux linkage can be obtained as [12]

$$N_{CI} \phi_{a_{k,max}} = \frac{V_{dc}}{9f_c} \quad (11)$$

Using (11), the product of the number of turns N_{CI} and the core cross-section area is obtained and the information is used to choose a suitable core. Parameters of the designed CI are given in Table VI. Amorphous alloys 2605SA1 is considered as a magnetic material for the CI.

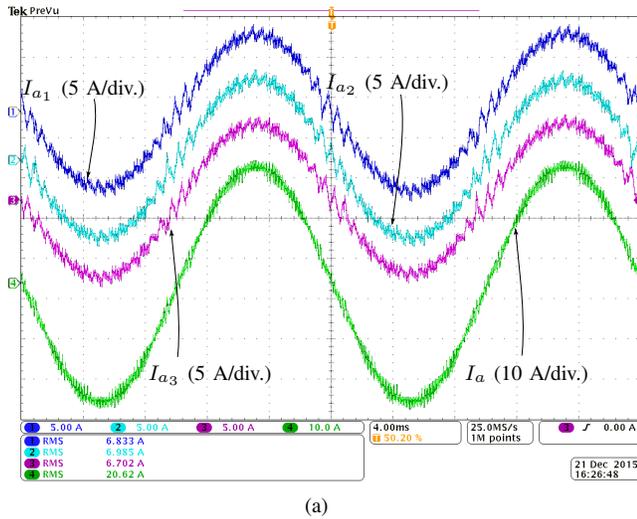
The Improved Generalized Steinmetz Equation (IGSE) [33], [34] is used to calculate the core losses of the CI and the core losses per unit volume are given as

$$P_{fe,v} = \frac{1}{T} \int_0^T k_i \left| \frac{dB(t)}{dt} \right|^\alpha (\Delta B)^\beta dt \quad (12)$$

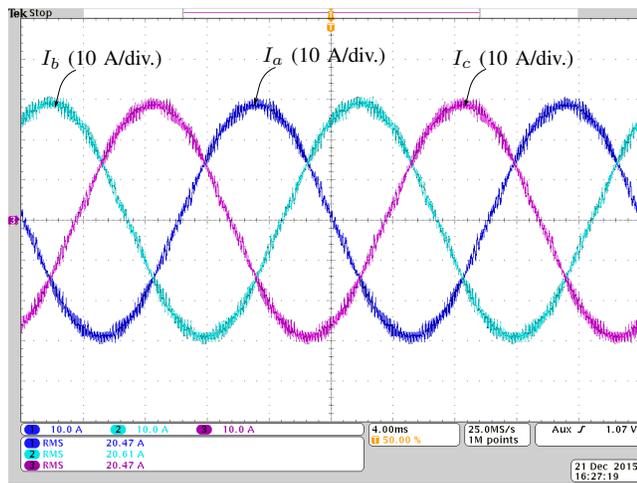
where ΔB is the Peak-to-peak value of the flux density. α , β and k_i are the constants (Steinmetz parameters) determined by the material characteristics. The values of the Steinmetz parameters α , β and k_i are 1.51, 1.74, and 0.62, respectively. The evaluated core losses for the proposed PWM scheme and the PS PWM are 498 W and 409 W, respectively. Since there are three CIs required for the three-phase system, the total core losses in the case of the proposed PWM are 1.49 kW against 1.22 kW in the case of the PS PWM.

D. Hardware Results

To verify the proposed modulation scheme, a small scale prototype was developed. The specifications of this prototype are given in Table VII. The CI was build using the three-phase E-core, made from the amorphous alloy 2605SA1. The



(a)

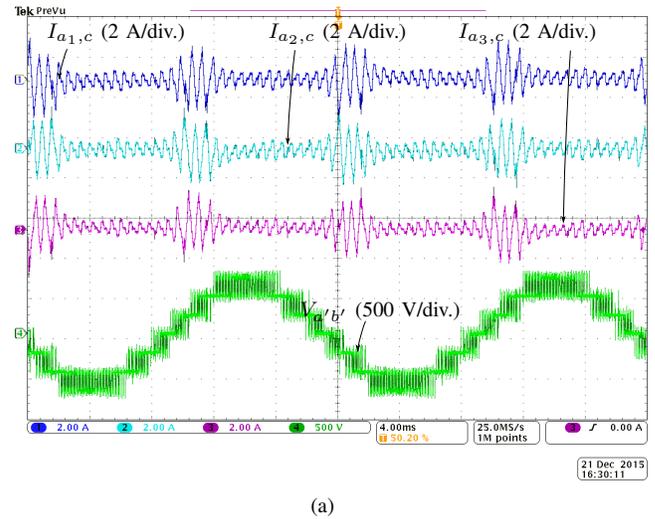


(b)

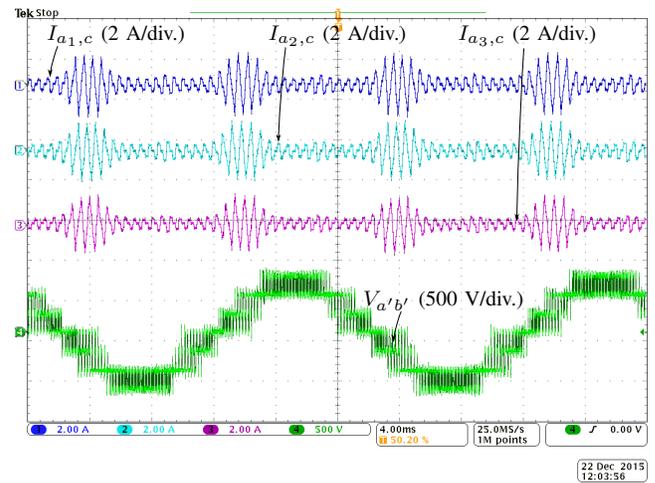
Fig. 22. The experimental current waveforms for the proposed modulation scheme. The carrier frequency is 3×1650 Hz. (a) Ch1: VSC1 phase a current (I_{a1}), Ch2: VSC2 phase a current (I_{a2}), Ch3: VSC3 phase a current (I_{a3}), Ch4: Resultant current of phase a (I_a), (b) Ch1: Resultant current of phase a (I_a), Ch2: Resultant current of phase b (I_b), Ch3: Resultant current of phase c (I_c).

maximum value of the flux density in the core is taken to be 1 T. The effective cross-section area of each of the limbs is 5.78×10^{-4} m² and the number of turns in each of the coils is 78. The photograph of the CI is shown in Fig. 5(b). The proposed modulation scheme has been implemented using the TMS320F28377D Micro-controller. The system was connected to the resistive load of 11.5Ω . The carrier frequency is taken to be 3×1650 Hz.

The simulation study was first carried out to demonstrate the effect of the dc volt-sec injection during the band transition. The simulation parameters were taken to be the same as that of the actual hardware setup. The simulation was carried out using PLECS, where the magnetic toolbox was used to model the CI and the line filter inductor L_f . Magnetic core was modeled using the linear core. The parallel VSCs were switched sequentially. However, the flux balancing control during the band transition was not employed. In this case, the simulated flux density in the CI is shown in Fig. 21. DC volt-



(a)



(b)

Fig. 23. Circulating currents of phase a of all three VSCs and the resultant line-to-line voltage $V_{a'b'}$. (a) Proposed modulation scheme with the carrier frequency of 3×1650 Hz, (b) Phase-shifted PWM with three 120° phase-shifted carrier with the frequency of 1700 Hz.

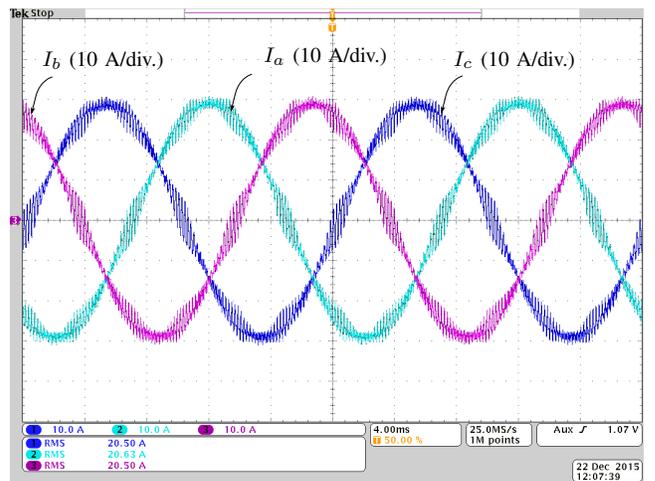
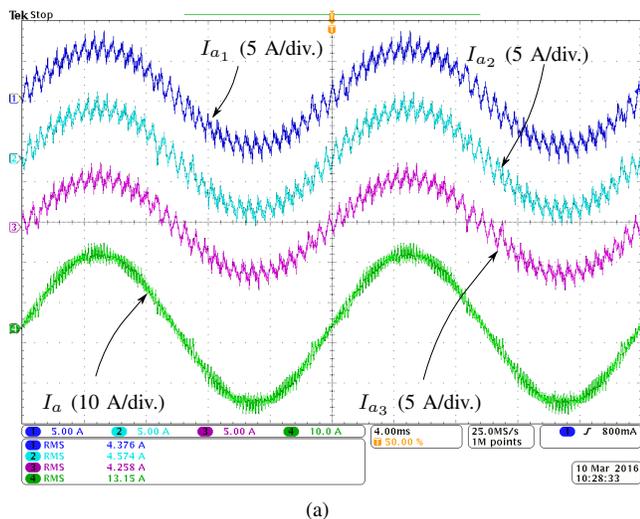
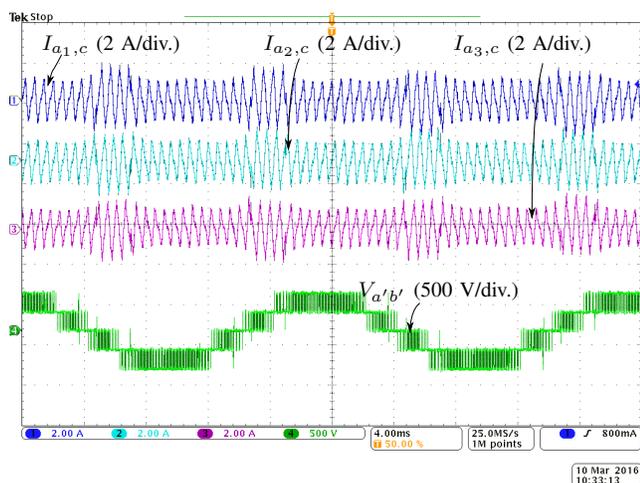


Fig. 24. Resultant line currents for the phase-shifted PWM with three 120° phase-shifted carrier with the frequency of 1700 Hz.



(a)

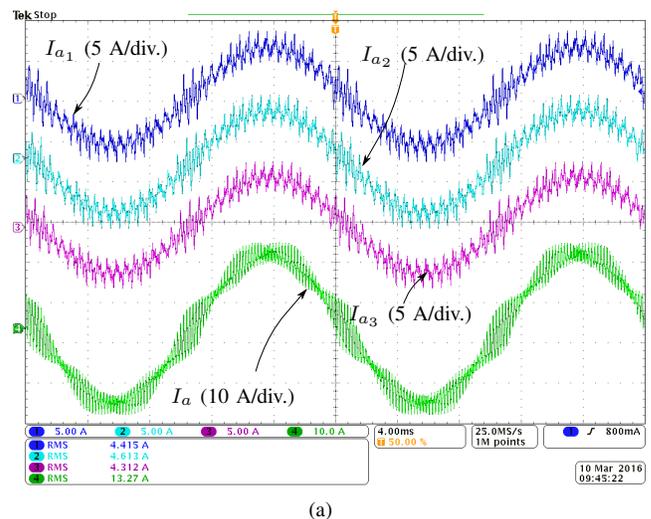


(b)

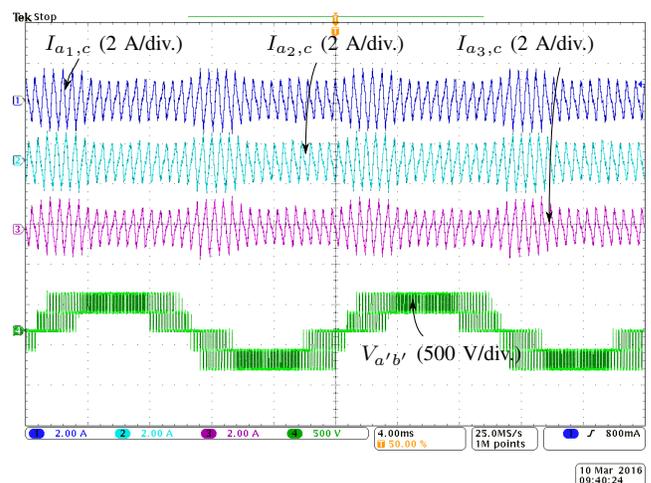
Fig. 25. Proposed PWM scheme: Experimental waveforms for modulation index $M = 2/3$. The carrier frequency is taken to be 3×1650 Hz. (a) Leg currents of the individual VSCs and the resultant line current, (b) Circulating currents of phase a of all three VSCs and the resultant line-to-line voltage $V_{a'b'}$.

sec is injected during the band transition, which introduces dc flux in the CI. This drives CI into saturation region, as shown in Fig. 21. As a result, the inductance offered to the circulating current decreases substantially and large circulating current flows which may activate over-current protection. Therefore, conventional PD PWM without flux balancing scheme can not be applied to parallel interleaved VSCs without oversizing the CI.

The leg currents of phase a of all the VSCs along with the resultant current for the modulation index of $M = 1$ are shown in Fig. 22(a). The rms values of the leg currents of the parallel VSCs are measured and they are shown in Fig. 22(a), which demonstrates that the equal current sharing among the parallel VSCs has been achieved. The resultant line currents of all the phases are shown in Fig. 22(b). The resultant currents are sinusoidal, which show that the disturbance in the line-to-line voltage during the band transition due to the extra commutations is avoided in the proposed modulation scheme. The circulating current components of the phase a



(a)



(b)

Fig. 26. PS PWM: Experimental waveforms for modulation index $M = 2/3$. The carrier frequency is taken to be 1700 Hz. (a) Leg currents of the individual VSCs and the resultant line current, (b) Circulating currents of phase a of all three VSCs and the resultant line-to-line voltage $V_{a'b'}$.

of all three VSCs along with the resultant switched line-to-line voltage $V_{a'b'}$ are shown in Fig. 23(a). These circulating current component is proportional to the flux in the CI and it is evident that the flux balancing is achieved by the proposed modulation scheme (as against the dc flux injection shown in Fig. 21 for the PD PWM implementation). The switched line-to-line voltage has a transition between the two nearest voltage levels during each commutation, as shown in Fig. 23(a). However, this is not the case when PS PWM is used, as shown in Fig. 23(b). As a result, substantial improvement in the harmonic performance can be achieved by the proposed modulation scheme, which is evident from Fig. 22(b) and Fig. 24, where the resultant line currents for both cases are shown for the comparison. The experimental waveforms for the proposed modulation scheme and the PS PWM for the modulation index $M = 2/3$ are shown in Fig. 25 and Fig. 26, respectively. The improvement in the line current quality, achieved by the proposed PWM scheme is more pronounced at the middle of the modulation depth.

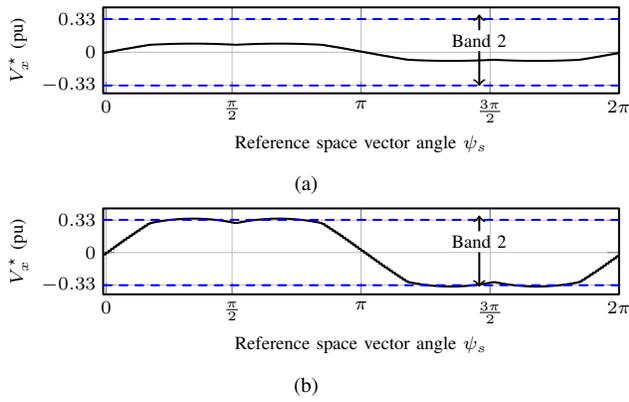


Fig. 27. Sampled command reference signal. (a) $M = 0.1$, the command reference signal is confined within band 2, (b) $M = 0.4$, eight band transitions occur in the fundamental frequency cycle.

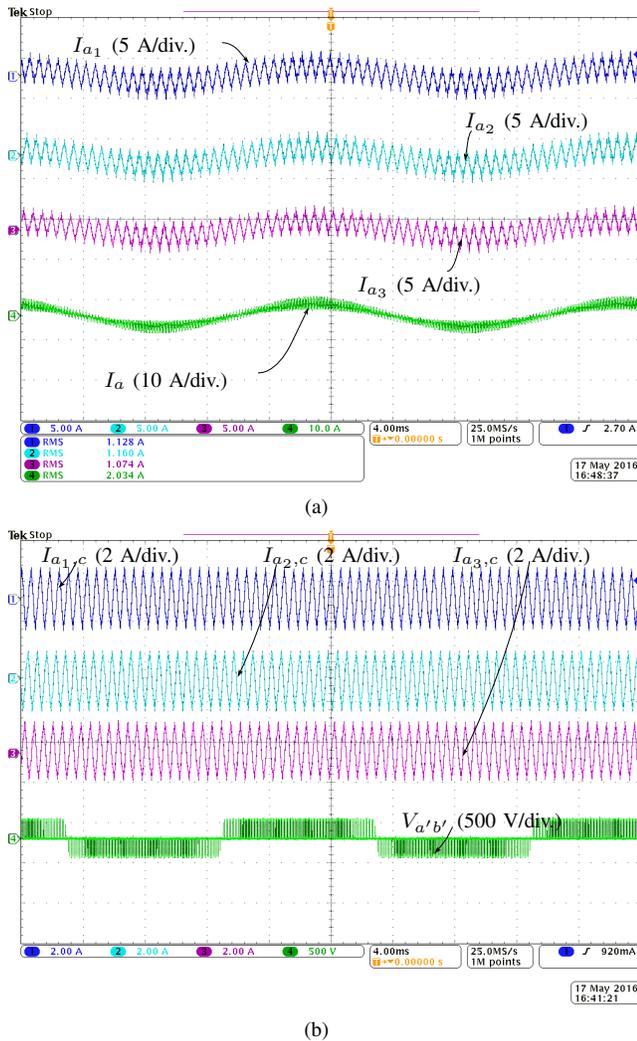


Fig. 28. Proposed PWM scheme: Experimental waveforms for modulation index $M = 0.1$. The carrier frequency is taken to be 3×1650 Hz. (a) Leg currents of the individual VSCs and the resultant line current, (b) Circulating currents of phase a of all three VSCs and the resultant line-to-line voltage $V_{a'b'}$.

For low modulation indices, the command reference signal V_x^* is confined in band 2 and therefore the band transition does

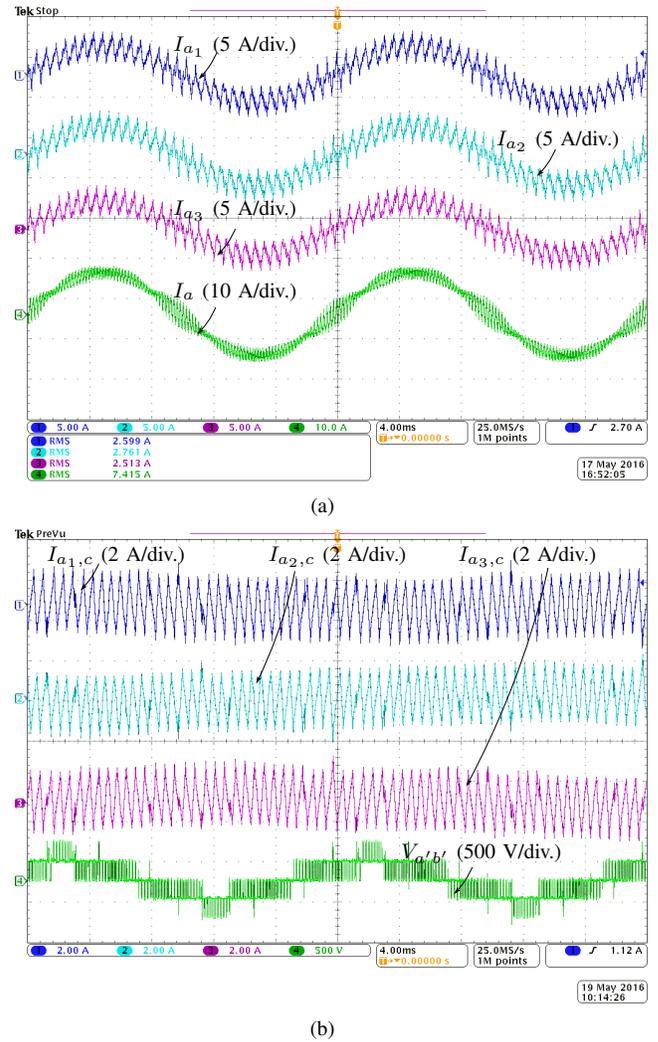


Fig. 29. Proposed PWM scheme: Experimental waveforms for modulation index $M = 0.4$. The carrier frequency is taken to be 3×1650 Hz. (a) Leg currents of the individual VSCs and the resultant line current, (b) Circulating currents of phase a of all three VSCs and the resultant line-to-line voltage $V_{a'b'}$.

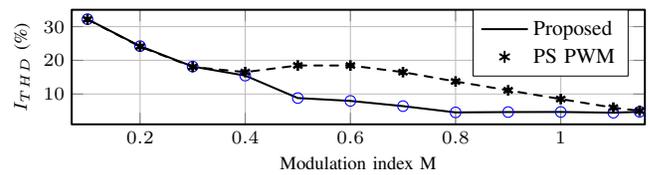


Fig. 30. Measured total harmonic distortion of the resultant line current as a function of the modulation index.

not occur, as it is shown in Fig. 27(a) for the modulation index $M = 0.1$. The experimental waveforms for the proposed PWM for the modulation index $M = 0.1$ are shown in Fig. 28. The circulating currents of phase a are shown in Fig. 28(b), where it is evident that the natural flux balancing is achieved for low modulation indices when the command reference signal V_x^* is confined in band 2. In this case, additional commutations of the VSC legs are not necessary for the flux balancing, as it is visible from the circulating current waveforms shown in Fig. 28(b). The command reference signal for $M = 0.4$ is

shown in Fig. 27(b). In this case, the command reference signal goes through eight band transitions in a fundamental frequency cycle. The associated experimental results are shown in Fig. 29. The flux balancing is achieved by introducing additional commutations and the effects of these additional commutations are visible in the circulating current waveforms, shown in Fig. 29(b).

Several experimental results with the different values of the modulation index for both cases are obtained. The Total Harmonic Distortion (THD) of the resultant line current is obtained as

$$I_{\text{THD}} = \frac{1}{I_{x,f}} \sqrt{\sum_{h=2}^{1000} (I_{x,h})^2} \quad (13)$$

The variation of the total harmonic distortion of the resultant line current as a function of the modulation index is shown in Fig. 30. The proposed modulation scheme demonstrates superior harmonic performance over wide modulation index range.

VI. CONCLUSION

A modulation scheme using the single carrier to realize PD PWM for the parallel 2L-VSCs is presented. The proposed scheme can be easily implemented using a DSP and the complexity is substantially reduced compared to other implementations, which require several trapezoidal carriers. The operation of the parallel VSCs with the coupled inductor is discussed and the dc flux injection issue in the case of the PD PWM is investigated. During the steady-state (without band transition), the proposed scheme ensures volt-sec balance in a switching cycle by sequential switching of the parallel VSC legs.

A dc flux is injected during the very first sampling interval that follows the band transition and it may lead to CI saturation. The proposed scheme also ensures volt-sec balance in the first sampling interval that follows the band transition. This is achieved by introducing additional commutations of the parallel VSCs. The band transition scheme also ensures the volt-sec balance to synthesize the reference space voltage vector even during a band transition. As a result, any disturbance in the line-to-line voltage is avoided. The harmonic performance of the proposed scheme is compared with the PS PWM by evaluating the NWTHTD under constant switching loss condition. The carrier frequency in the proposed scheme is reduced to account for the effect of the additional commutations introduced during the band transition. As a result, the harmonic performance of the proposed implementation is slightly inferior compared to the PS PWM for the low modulation indices ($M < 0.4$), whereas it is harmonically superior in the remaining modulation range. For the grid connected applications, where the converter operates with the modulation index in the vicinity of one, the proposed implementation results in 44% reduction in the NWTHTD.

APPENDIX

The magnetic structure of the N limb CI is shown in Fig. 5(a). By neglecting the resistance of the coils, the induced

voltage across the k th coil can be obtained as (refer Fig. 1)

$$V_{x_k o} - V_{x' o} = L_{x_k x_k} \frac{dI_{x_k}}{dt} - \sum_{\substack{j=1 \\ j \neq k}}^N L_{x_k x_j} \frac{dI_{x_j}}{dt} \quad (14)$$

where $L_{x_k x_k}$ is the self inductance and $L_{x_k x_j}$ is the mutual inductance between the k th and j th coils. By assuming the leakage flux to be zero, the flux induced by one of the coils completes its path through the remaining limbs and the relationship between the self and mutual inductances can be given as

$$L_{x_k x_k} = \sum_{\substack{j=1 \\ j \neq k}}^N L_{x_k x_j} \quad (15)$$

By adding the induced voltages across all coils and taking average gives

$$\frac{1}{N} \sum_{k=1}^N V_{x_k o} - V_{x' o} = \frac{1}{N} \sum_{k=1}^N \left(L_{x_k x_k} - \sum_{\substack{j=1 \\ j \neq k}}^N L_{x_k x_j} \right) \frac{dI_{x_k}}{dt} \quad (16)$$

By using (15) and (16), the resultant switched output voltage can be obtained as

$$V_{x' o} = \frac{1}{3} \sum_{k=1}^3 V_{x_k o} \quad (17)$$

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