A Gate Driver Design for Medium Voltage Silicon Carbide Power Devices with High dv/dt

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***Abstract*—The use of silicon carbide (SiC) devices in medium voltage (MV) applications has become a possibility due to the development of reliable MV SiC power devices. However, when SiC devices are used in these MV applications, they are exposed to a high voltage peak stress (of up to 15 kV across the primary and secondary side of the gate driver) and a very high dv/dt (of up to 100 kV/µs across the isolation transformer). The gate driver design is very critical for proper functioning of the MV devices under the presence of such high dv/dt. This paper presents a design of an improved gate driver power isolation method, with a low coupling capacitance between the primary and the secondary side. The footprint of the isolation transformer is minimized to meet the clearance and insulation requirements. Comparisons have been drawn with an existing gate driver topology, on the basis of size of the gate driver, and common mode performances for different dv/dt. Experimental results are provided to validate both the gate driver designs. The testing and analysis is carried out on a 10 kV SiC MOSFET developed and packaged by Wolfspeed. In addition, a brief discussion on the insulation standards for these kinds of applications is provided. The gate driver concept is aimed at providing a benchmark for building an efficient and reliable method to drive MV SiC devices.**

***Index Terms*—coupling capacitance, double pulse tests, dv/dt immunity, gate driver, medium voltage, silicon carbide devices**

I. Introduction

With the advancement in the semiconductor device industry, power devices such as silicon carbide metal-oxide-field-effect transistors (SiC-MOSFETs) and silicon carbide insulated-gate-bipolar transistors (SiC-IGBTs) are now available with blocking voltages up to 15 kV [1]. From the perspective of power converter applications, these devices have facilitated the use of power converters at distribution voltage level without the use of higher order multilevel converter technologies [2].

The efficient and reliable use of these MV devices can be realized not only by improving the performance of the device itself, but also by maintaining a reliable auxiliary system. There are a lot of challenges involved in using a MV SiC device in a power converter system (due to the high dv/dt across the SiC MOSFETs), which mainly includes the design of the passive elements and the design of the gate drivers [3], [4]. The design of the gate drivers, is however, more critical since improper designs of gate drivers can lead to instantaneous device failures and unreliable converter operation. If the insulation between the MV and the signal side of the gate driver is not designed carefully, it might lead to damage of the control equipments and might create safety issues. In addition, the amount of common mode noise injected by the gate driver is of high importance, since, it affects the operation of the control and other auxiliary circuitry since they share a common ground with the gate driver. The high dv/dt experienced by the devices and consequently, other elements of the power converter system, leads to the reduction in signal integrity of the control signals due to the common mode noise that flows through the inter-winding capacitance of the isolation transformer. The magnitude of the common mode (CM) current (I_{cm}) is directly affected by the dv/dt and isolation capacitance (C_{iso})

$$i_{cm} = C_{iso}\frac{dv}{dt} \tag{1}$$

Designing the power transmission stage of the gate driver is a challenge basically due to three main reasons:

- High isolation requirements
- Low coupling capacitance
- Optimized gate driver footprint

It becomes necessary to satisfy all these requirements simultaneously, and since the requirements counter one another, it becomes imperative to have an optimum trade-off.

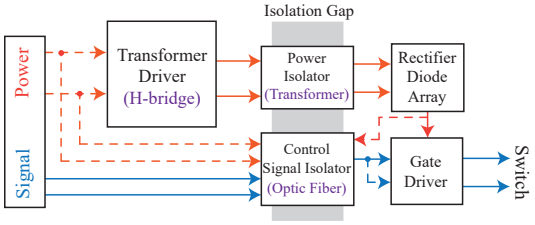


Fig. 1: General schematic of the architecture of a gate driver circuit.

For a reliable operation of the MV devices, the gate drivers are aimed towards satisfying the above requirements. A number of gate driver concepts have been introduced in the literature [5]–[12]. In [5], a gate driver based for a 15 kV SiC MOSFET is designed and evaluated. The isolation in the gate driver power supply is based on a power over fiber (PoF) concept. This provides very high immunity for common mode noise. However, due to its very low efficiency (24%), and its maximum power output being limited to 0.5 W, realization of the gate driver for driving parallel dies leads to an increase in the gate driver footprint. In [6], a gate driver is designed to drive 15 kV SiC IGBTs and is based on the

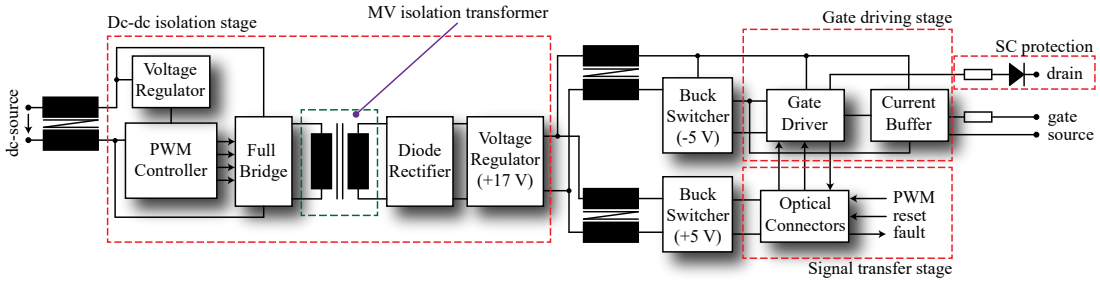


Fig. 2: Overall architecture of the designed gate driver. It includes four main parts: dc-dc isolation stage, signal transfer stage, gate driving stage and short circuit protection stage.

conventional transformer method. A coupling capacitance of less than 1 pF is claimed. However, no information on the common mode currents is provided. A gate driver with high common mode rejection and a miller clamp is provided in [7]. A flyback based topology is used for the isolation stage and a coupling capacitance of 2.6 pF has been achieved. Gate drivers using wireless power transfer have also been studied [9], [10]. These are however, sensitive to electromagnetic interference (EMI) and requires larger size for isolation and shielding. A current-loop based gate driver is proposed in [11]. No experimental results are however provided regarding the insulation capabilities of the gate driver.

This paper provides a design and development of a MV gate driver to minimize the common mode noise through the source (by minimizing the parasitic capacitance of the isolation transformer). A dc isolation which is multiple time the working voltage is provided for reliable operation of the gate driver over an extended period of time. The performance of the gate driver is evaluated experimentally by conducting double pulse tests on a 10 kV SiC MOSFET from Wolfspeed. The coupling capacitance and the associated common mode currents of the gate driver is also measured. Comparison between the designed gate driver and the gate driver designed in [6] in terms of gate driver footprint and common mode performance is also carried out.

II. State-of-the art Gate Driver Power Supply

The design of the existing state-of-the art gate driver is based on the requirements necessary to drive a MV device with high dv/dt. The gate driver is tested in double pulse test and continuous operation using a 15 kV SiC N-IGBT [6]. Fig. 3 shows the photograph of a state-of the art gate driver.

A. Power Supply Topology

The power supply topology of is based on a Single Active Bridge (SAB) converter where, a full bridge converter (on the primary side) is used to transfer power through the isolation transformer [13]. A switching frequency of the SAB is chosen as 50 kHz. A rectifier diode bridge is used to convert the high frequency ac signal to unregulated dc values. Voltage regulators are not provided on the secondary side and the voltage regulation is done by the input dc power supply. The transformer consists of two windings, which generates +20 V and -5 V to drive the 15 kV SiC IGBT (recommended values). The +5 V, which is required to drive the optical receivers and transmitters is derived from the -5 V supply.

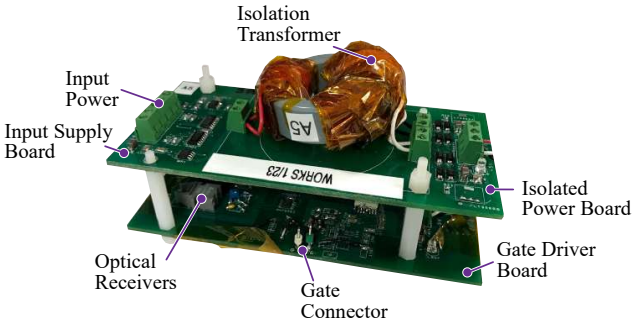


Fig. 3: Photograph of a state-of the art gate driver.

B. Transformer Design

The transformer provides the high voltage insulation between the primary and the secondary side of the gate driver and hence, termed as isolation transformer. This transformer is realized with a toriodal ferrite core based transformer. A ferrite based material is chosen since it has a high permeability, and also, due to its low costs. The inner diameter of the toroidal core is chosen to be 35 mm and an outer diameter of 50 mm is used as the core for the isolation transformer. Since the power transferred from the primary to secondary is a few watts, the effect of leakage inductance is ignored. The medium voltage insulation is provided by the use of several layers of Kapton tape [14]. Fig. 5(a) shows the representation of the transformer used for the gate drive circuit.

III. Proposed Gate Driver Isolated Power Supply

The high voltage isolation and high dv/dt requirements on the gate driver imposes several restrictions on the design of the dc-dc isolation stage. In addition, the selection of components having high immunity to noise and having reliable signal transfer capability, while maintaining a small footprint, is imperative. The overall architecture of the proposed gate driver is shown in Fig. 2 [15]. The design of the dc-dc isolation stage is the most important aspect while building a MV gate driver for driving MV SiC devices dud to the stringent requirements

imposed on it on account of the high dv/dt it experiences. A photograph of the proposed gate driver is shown in Fig. 4.

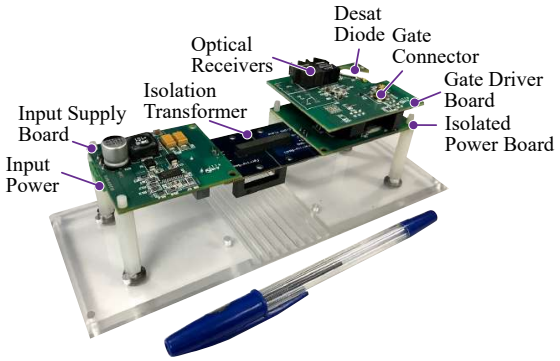


Fig. 4: Proposed gate driver solution. The existing gate driver is three times larger than the proposed gate driver in terms of volume.

A. Power Supply Topology

The designed power supply utilizes the SAB topology to deliver power across the isolation stage. The full-bridge is switched at a switching frequency of 100 kHz which ensures a reasonable temperature rise in the transformer (on account of core losses) while maintaining a minimum size of the transformer. The secondary side of the SAB consists of a diode rectifier for converting the high frequency ac signal to an unregulated dc-stage. The output of the unregulated dc-stage is kept between 17 V and 18 V. A linear regulator of 17 V is used thereafter to convert the unregulated dc-voltage to a regulated dc voltage. A -5 V stage for turning off the SiC-MOSFET is derived from the regulated +17 V power supply. The power supply for the signal stage (optical fiber) is also generated from the regulated +17 V supply. The +17 V/ -5 V gate drive is based on the recommended driving voltages for the Gen3 10 kV SiC MOSFET.

B. Transformer Design

A PCB based planar winding is used in the new design. This leads to an increase in the leakage inductance of the transformer as compared to wire based winding on similar cores, but it greatly helps in the reduction in coupling capacitance owing to the smaller area of cross section between the winding structure and the core. Also, in order to meet the insulation requirements, each of the primary and the secondary windings are inserted on the middle layers of the PCB which ensures that the windings have proper insulation both from the top and the bottom sides. In order to maintain the insulation standards, the designed transformer PCB is manufactured using a polyamide material, Arlon 85S whose dielectric strength is 1.5 times that of FR4 with 1200 V/mil (when new) and around 700 V/mil with aging [16]. The dielectric strength of FR4 is around 800 V/mil which reduces down to 300 V/mil with aging [17]. Fig. 5(b) shows the representation of the transformer used for the gate drive circuit.

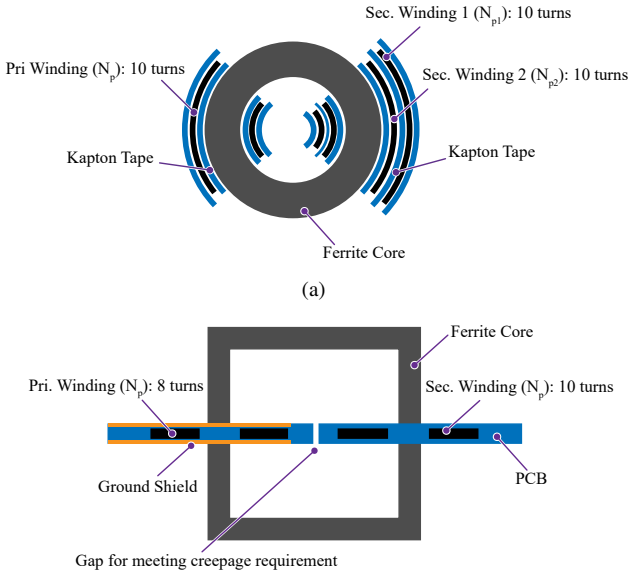


Fig. 5: (a) Schematic representation of the transformer core and the windings of (a) Existing gate driver transformer (b) Proposed gate driver transformer.

IV. Comparative Study between the Gate Drivers

A comparison between both the gate drivers is drawn based mainly on three factors: the transformer design, overall footprint, and the common mode performance. The effect of the transformer design on the common mode performance of the gate drivers is also studied. A brief idea about the power supply stage is also provided. Comparisons between the gate driving stage is not considered here. This is due to the fact that the gate driver stage of the MV gate driver is similar to that of the LV gate drivers, and it is widely studied in the literature, apart from the fact that the MV gate driver requires a fast MV Schottky/pin diode for desat protection.

A. Power Supply Stage

Both the gate drivers are designed with the same SAB topology for the input power stage. While the existing gate driver uses four different switches to realize the full bridge circuit, an integrated switch is used in the new gate driver design. Similarly, the secondary side contains discrete diodes in the existing gate driver design (two sets of diode bridges are provided for each of the two secondary windings), while an integrated diode array is used in the proposed gate driver.

B. Transformer Design

The difference in the transformer design in both the gate drivers is the major reason for the difference in performance. While the existing gate driver uses a toroidal based ferrite core, the proposed gate driver uses two C cores glued together. Fig. 6 shows the transformer cores and their relative sizes. The sizes vary from each other due to two major reasons, one being the operating switching frequency, and the other being the winding structure. It should be noted that the flux

density of the transformer cores are not the same in both the cases. Since the designed gate driver uses a pcb based winding structure, and has just two windings, it takes up considerably lesser space as compared to the toroidal based structure which has three windings. In addition, the insulation of the designed transformer is realized by the pcb based structure (pcb is constructed with a material with high voltage breakdown strength) and hence the size of the transformer becomes smaller. Since the toroid based transformer uses kapton as an insulating material, additional safety measures have to be taken while determining the size of the transformer, since kapton tape is porous in nature.

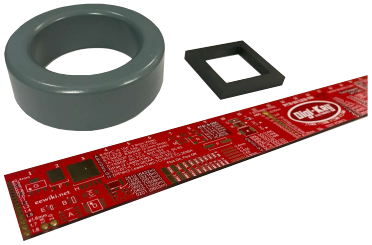


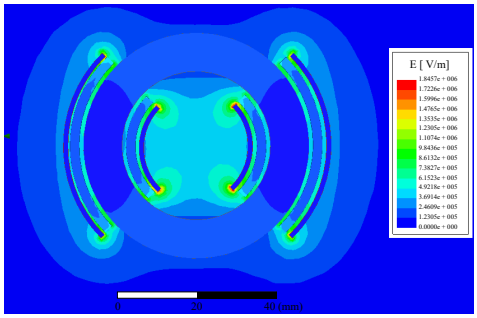
Fig. 6: Transformer isolation cores used for both the gate drivers. The ruler is placed to show the relative size of the magnetic cores. The toroid has an outer diameter of 50 mm, with a height of 15 mm. The C-cores have a outer dimension of 28 mm $\times$ 28 mm $\times$ 4 mm.

C. Isolation Capacitance

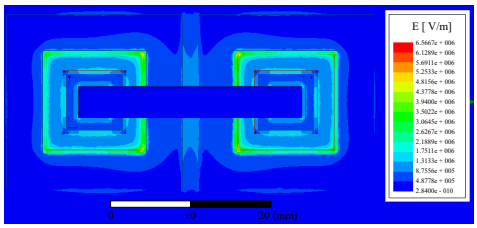
The major difference between the isolation capacitance of the gate drivers come from the fact that the existing gate driver uses two secondary windings to generate the driving stage voltages (and the voltage for the optocouplers), where as the new gate driver design uses one winding in the secondary and derives all the voltages from the same. This serves as an advantage due to the fact that it results in a lower isolation capacitance (in conjunction with other factors). The coupling capacitance between the primary and the secondary winding of the transformer is mainly dependent on the distance between the primary and the secondary windings, and the area enclosed by the transformer windings and the core. The dominant part of the capacitive coupling is present through the transformer core [7]. The proposed gate driver uses a pcb based winding as opposed to wire based winding in the existing gate driver which helps in reducing the area enclosed by the transformer winding and the core and consequently the coupling capacitance. Finite Element Analysis (FEA) of both the designs reveal a coupling capacitance of nearly 1 pF and 4 pF respectively. The analysis is done assuming an ideal environment to provide a rough idea of the relative isolation capacitance. The FEA showing the relative electric fields is shown in Fig. 7

D. Clearance and Creepage Requirements

The transformer provides the high voltage isolation between the two sides of the gate driver. The design of the transformer is based in two major factors which includes achieving a low coupling capacitance between the primary and secondary and



(a)



(b)

Fig. 7: Finite Element Analysis of the transformer cores for (a) toroid based ferrite core, and (b) C-cores glued together.

being able to meet the high isolation requirements, apart from having a small footprint. In addition to these requirements, it is necessary for the transformer design to meet the clearance and creepage standards as provided in IEC 61800-5-1 [18]. For a working voltage of 7.2 kV - 7.6 kV, which is ideally the operating voltage for 10 kV SiC MOSFETs, the clearance requirement is 25 mm for all the pollution levels. The creepage requirement comes to be around 32.5 mm [18], [19].

The proposed gate driver adheres to the standards and is tested up to a dc voltage of 20 kV. The adherence to the standards is based on the fact that the minimum distance between the open terminals of the primary and secondary side of the transformer is maintained below 25 mm. The creepage distance is maintained through the support structure. In the existing gate driver, the creepage distance is maintained directly on the pcb structure. The clearance between the open terminals is also at 80 mm (which is way more than the required clearance). However, the insulation is based on the layers of kapton which is a porus material. It might not be a reliable option for a continuous operation in the field.

E. Relative Size

The relative size of both the gate drivers are compared. Even having a similar operational capability (even though the common mode performance is better in the proposed gate driver), the sizes of the gate drivers vary a lot. While the proposed gate driver has dimensions of 6 inches $\times$ 2 inches $\times$ 1.5 inches, the existing gate driver is three times more in volume with dimensions of 6 inches $\times$ 3 inches $\times$ 3 inches. The sizes of the gate drivers vary due to the way each of these are designed. As it can be seen, in the existing gate driver, the gate driver board is of similar size as that of the power board.

This necessitates a clearance between the top and the bottom boards. In case of the designed system, the gate driver board is limited to the isolated power board in size and hence can be placed very close to each other.

V. Experimental Validation

The gate drivers are tested for its common mode performance on a 10 kV SIC MOSFET designed and packaged by Wolfspeed. The devices used and the experimental setup is shown in Fig. 8. The common mode current is measured on the connection from the dc power supply to the gate drivers. A dc power supply by Keysight (E3631A) is used to supply power to each of these gate drivers. It should be noted that the designed gate driver uses an input voltage of +16 V, where as the existing gate driver uses an input voltage of +10 V. A gate

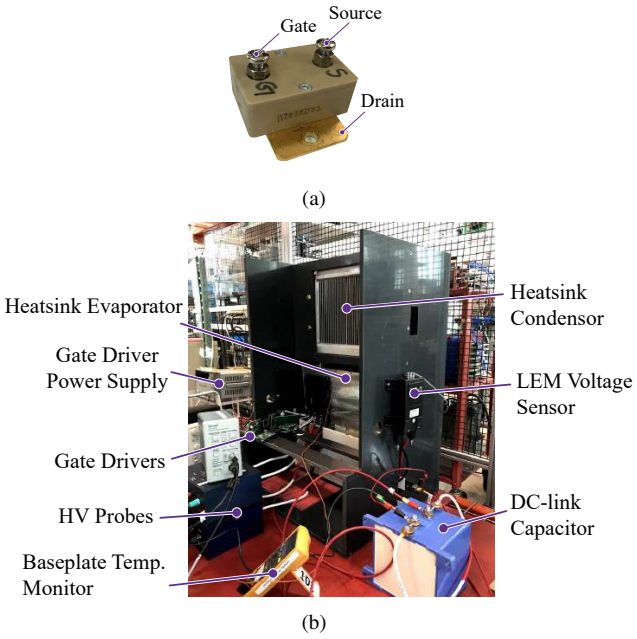


Fig. 8: (a) 10 kV SiC MOSFET used for testing and validating the operation of the gate drivers (b) Experimental test setup used. The experimental test setup is built to test the devices in continuous mode of operation.

resistance of 20 Ω is used for both the gate drivers and the common mode performance for various dc-link voltages (and various dv/dt) is measured.

The experimental results showing the common mode currents for different values of dc-link voltages is shown in Fig. 10, for the existing gate driver and Fig. 11, for the designed gate driver. It should be noted that the scales for the common mode currents are different in both the cases. Fig. 9 shows comparative results for both the gate drivers at exactly similar conditions at a dc-link voltage of 7.5 kV. A maximum common mode current of 275 mA flows through the existing gate driver for a dv/dt of 39 kV/µs. For the same dv/dt, a maximum common mode current of 83 mA is observed. An isolation capacitance of nearly 6 pF is noted for the existing gate driver from the measured dv/dt and the common mode currents. For the designed gate driver, an isolation capacitance of around

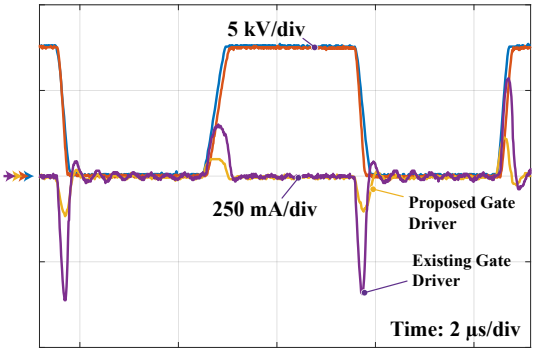


Fig. 9: Comparative experimental results for demonstrating the performance of the designed gate driver over the existing gate driver. A maximum common mode current of 275 mA flows through the existing gate driver for a dv/dt of 39 kV/µs. For the same dv/dt, a maximum common mode current of 83 mA is observed.

2.5 pF is found. The results are in agreement to the fact that the isolation capacitance, which determines the common mode currents for the designed gate driver is much lesser than the existing gate driver. This ensures superior performance of the designed gate driver over the existing gate driver.

VI. Conclusions

This paper presents a new gate driver for driving medium voltage silicon carbide devices. Comparisons have been drawn with an existing gate driver on basis of the common mode performance, transformer design and relative sizes of the gate driver. A superior common mode performance of the designed gate driver is observed, with its isolation capacitance being 6 pF as compared to an isolation capacitance of 2.5 pF, for the existing gate driver design. The design of the isolation transformer, and its windings serve as a major difference between the two gate drivers, which consequently affects their size and performance. In addition, a brief discussion on the insulation standards required to be satisfied for safe an reliable operation is also provided. This gate driver design is aimed to serve as a building block for safe an reliable operation of medium voltage devices. It also aims at providing an impetus for the use of medium voltage silicon carbide devices.

References

[1] B. Sarrazin, R. Hanna, P. Lefranc, S. Am, F. Dumas, and J. P. Lavieville, "Insulated power supply for gate drivers up to 40 kV for medium-voltage direct current applications," *IET Power Electronics*, vol. 10, no. 15, pp. 2143–2148, 2017.

[2] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Solid-state transformer and mv grid tie applications enabled by 15 kv sic igbts and 10 kv sic mosfets based multilevel converters," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3343–3360, July 2015.

[3] A. Anurag, S. Acharya, Y. Prabowo, V. Jakka, and S. Bhattacharya, "Design of a Medium Voltage Mobile Utilities Support Equipment based Solid State Transformer (MUSE-SST) with 10 kV SiC MOSFETs for Grid Interconnection," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2018, pp. 1–8.

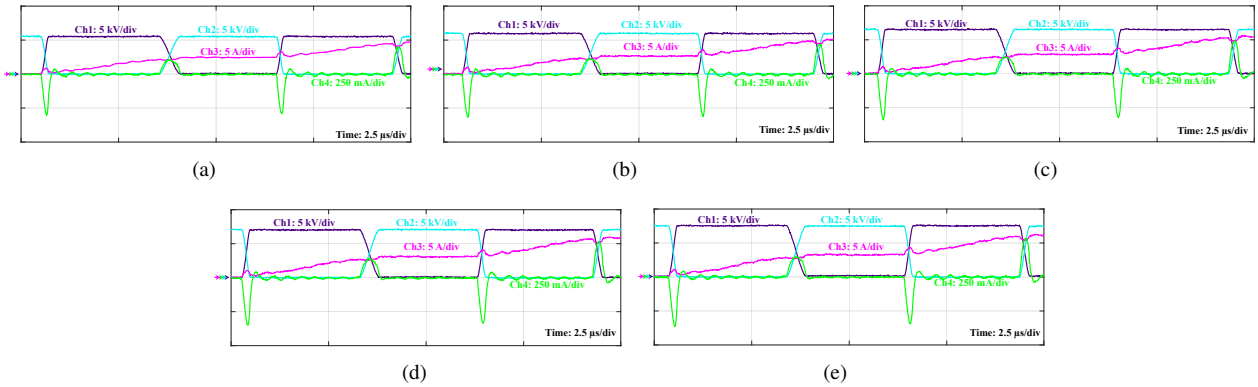


Fig. 10: Experimental results showing the variation in the common mode current in the existing gate driver with increasing voltage for a dc-link voltage of (a) 5.5 kV (b) 6 kV (c) 6.5 kV (d) 7 kV, and (e) 7.5 kV. The maximum common mode current occurs at a dv/dt of 36 kV/µs. (Ch1: Voltage across bottom device; Ch2: Voltage across top device; Ch3: Current through the inductor; Ch4: Common mode currents through the gate driver circuit).

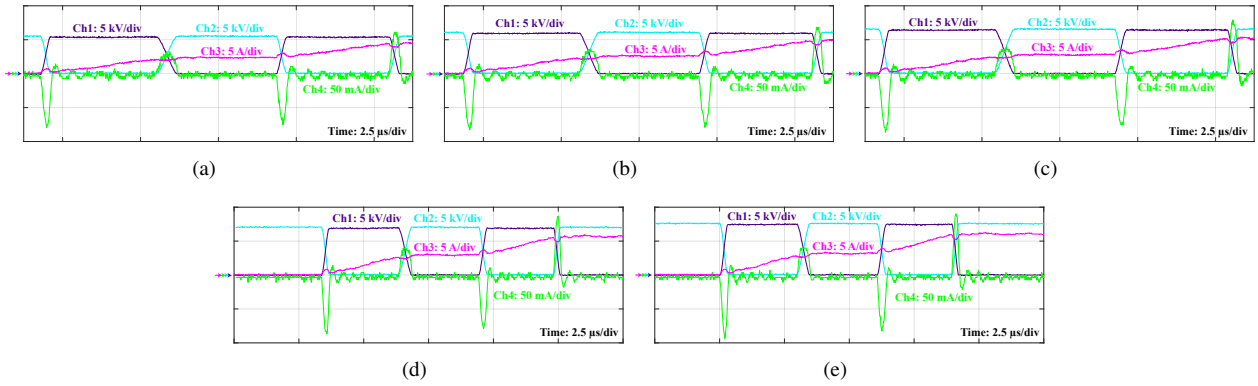


Fig. 11: Experimental results showing the variation in the common mode current in the proposed gate driver with increasing voltage for a dc-link voltage of (a) 5.5 kV (b) 6 kV (c) 6.5 kV (d) 7 kV, and (e) 7.5 kV. The maximum common mode current occurs at a dv/dt of 36 kV/µs. (Ch1: Voltage across bottom device; Ch2: Voltage across top device; Ch3: Current through the inductor; Ch4: Common mode currents through the gate driver circuit).

[4] S. Acharya, A. Anurag, Y. Prabowo, and S. Bhattacharya, "Practical Design Considerations for MV LCL Filter Under High dv/dt Conditions Considering the Effects of Parasitic Elements," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2018, pp. 1–7.

[5] X. Zhang, H. Li, J. A. Brothers, J. Wang, L. Fu, M. Perales, and J. Wu, "A 15 kV SiC MOSFET gate drive with power over fiber based isolated power supply and comprehensive protection functions," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 1967–1973.

[6] A. Kadavelugu and S. Bhattacharya, "Design considerations and development of gate driver for 15 kV SiC IGBT," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, March 2014, pp. 1494–1501.

[7] D. N. Dalal, N. Christensen, A. B. Jrgensen, S. D. Snderskov, S. Bczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter," in *2017 19th European Conference on Power Electronics and Applications*, Sept 2017, pp. P.1–P.10.

[8] B. Hu, Z. Wei, H. Li, D. Xing, R. Na, J. A. Brothers, and J. Wang, "A gate drive with active voltage divider based auxiliary power supply for medium voltage SiC device in high voltage applications," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 2979–2985.

[9] K. Kusaka, M. Kato, K. Orikawa, J. i. Itoh, I. Hasegawa, K. Morita, and T. Kondo, "Galvanic isolation system for multiple gate drivers with inductive power transfer - Drive of three-phase inverter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 4525–4532.

[10] R. Steiner, P. K. Steimer, F. Krismer, and J. W. Kolar, "Contactless energy transmission for an isolated 100W gate driver supply of a medium voltage converter," in *2009 35th Annual Conference of IEEE Industrial Electronics*, Nov 2009, pp. 302–307.

[11] J. Gottschlich, M. Schfer, M. Neubert, and R. W. D. Doncker, "A galvanically isolated gate driver with low coupling capacitance for medium voltage SiC MOSFETs," in *2016 18th European Conference on Power Electronics and Applications*, Sept 2016, pp. 1–8.

[12] S. Am, P. Lefranc, D. Frey, R. Hanna, and B. Sarrazin, "Gate Drivers for Medium Voltage Applications," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2017, pp. 1–8.

[13] Y. Ting, S. de Haan, and B. Ferreira, "Modular Single-Active Bridge DC-DC Converters: Efficiency Optimization over a Wide Load Range," *IEEE Industry Applications Magazine*, vol. 22, no. 5, pp. 43–52, Sept 2016.

[14] "kapton Tape," www.kaptontape.com, accessed: 2018-04-30.

[15] A. Anurag, S. Acharya, Y. Prabowo, G. Gohil, and S. Bhattacharya, "Design Considerations and Development of an Innovative Gate Driver for Medium Voltage Power Devices with High dv/dt," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[16] "High Voltage Printed Circuit Design and Manufacturing Notebook," www.magazines007.com, accessed: 2018-04-23.

[17] "Arlon," www.cirexx.com, accessed: 2018-04-23.

[18] "Insulation coordination for equipment within low-voltage systems - Part 1: Principles, requirements and tests," International Electrotechnical Commission, Standard, 2007.

[19] T. Batra, G. Gohil, A. K. Sesham, N. Rodriguez, and S. Bhattacharya, "Isolation design considerations for power supply of medium voltage silicon carbide gate drivers," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 2552–2559.