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R. Maheshwari, G. Gohil, L. Bede and S. Munk-Nielsen

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Effect of Dead-Time in Interleaved PWM for Two Parallel-Connected Inverters

Ramkrishan Maheshwari*, Ghanshyam Gohil†, Lorand Bede†, Stig Munk-Nielsen†
*Dept. of Electrical Engineering
Indian Institute of Technology, Delhi
New Delhi, India

†Dept. of Energy Technology
Aalborg University
Aalborg, Denmark

Tel.: +91 11 2659 7951
E-Mail: rkmahesh@ee.iitd.ac.in
URL: http://ee.iitd.ac.in

Keywords

Parallel-connected inverter, Dead-time, Circulating current, Pulsewidth modulation.

Abstract

Parallel-connected inverters are used for high power application. Due to the parallel-connection, there exists a circulating current which does not contribute to the ac side current. The analysis presented in the paper shows that the circulating current is affected by the dead-time. The effect of the dead time on the circulating current for the space vector pulse width modulation (PWM) and a discontinuous PWM is analyzed. The dead-time causes a dc value of the circulating current for the discontinuous PWM. A dead-time compensation technique is used for eliminating the dc component of the circulating current. Experimental results are presented to verify that.

Introduction

Parallel-connected voltage source inverters (VSI) have several advantages, such as reduced current ripple, modularity, improved thermal management, increased power capability, redundancy, easy maintenance, increased efficiency etc. [1]-[8]. The parallel-connected inverters have a common dc-link, and the ac sides of the inverters are connected through single-phase chokes as shown in Fig. 1. The parallel-connected inverters are widely used as a front-end ac-dc converter for high-power applications [1], [4]. Several literatures are available on the operation, control, and design of the parallel-connected inverters used for rectifiers [6], renewable energy systems, active filters [2], and power systems. The parallel-connected VSI are operated with interleaved pulsewidth modulation (PWM). This causes a circulating current between the inverters. The circulating current does not contribute to the grid current and causes additional losses in the system.

An interleaved discontinuous PWM (DPWM) is used in [7] for the parallel-connected inverters. The implementation is done by calculating the dwell time of the voltage vectors which are needed to be applied. The duty cycles are calculated using the dwell time and then phase shifted by the switching period. This results in different duty cycles for a phase of different inverters and causes a low frequency component in the circulating current. Similar implementation was used in [8] for DPWM, and a low frequency circulating current is observed due to difference between the duty cycles of the two inverters in a phase during a switching period.

In this paper, it is shown that the low frequency oscillation in the interleaved DPWM can be eliminated. However, in this process, a dc component is introduced in the circulating current. It is shown in the paper that the dc component is due to the dead-time. A deadtime compensation can be used to eliminate the dc component. In this way, the circulating current contains only switching frequency component. Therefore, the circulating current filter size can be optimized. Section II describes the cause of the circulating current. The effect of the dead-time on the circulating current is

analyzed in Section III. The experimental results verifying the analysis are shown in Section IV. Conclusions are presented in Section V.

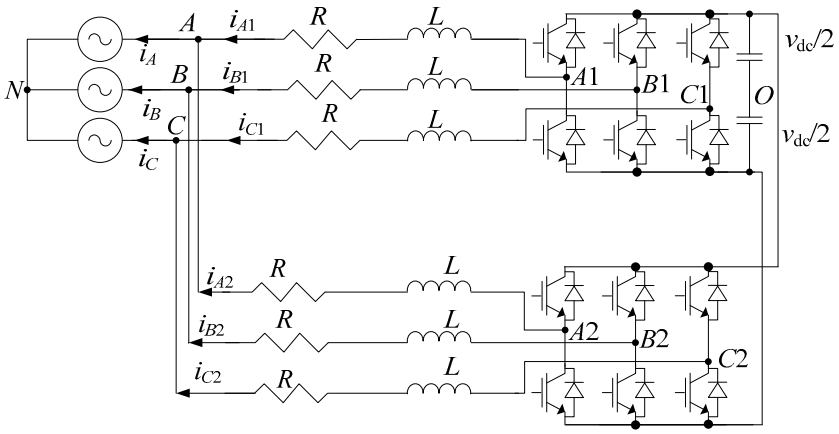


Fig. 1. Parallel-connected inverters.

Circulating Current

The block schematics of the system under consideration is shown in Fig. 1. The dynamics of the circulating current (i_o), which is the average of inverter 1 inductor currents, can be given by

$$Ri_o + L\frac{d}{dt}i_o = \frac{1}{2}\left(v_{cm1} - v_{cm2}\right) \tag{1}$$

where R and L represent the resistance and inductance of the inverter output choke. v_{cm1} and v_{cm2} are the common-mode (CM) voltages of the inverter 1 and inverter 2, respectively. The CM voltage is given by

$$v_{cmx} = \frac{1}{3}\left(v_{AxO} + v_{BxO} + v_{BxO}\right) \qquad x = 1,2 \tag{2}$$

The circulating current depends on the difference of the CM voltages. The CM voltage depends on the PWM strategy used for the converter. In addition, the difference of the CM voltage depends on the interleaving angle between the carrier signals for the inverters. The interleaving angle affects the total harmonic distortion (THD) of the inverter output current also. It is shown in [4] that the minimum THD for the output current is obtained when the interleaving angle is 180° for the two parallel-connected inverters. Therefore, this paper considers the case of 180° interleaving angle.

Different PWM strategies generate different CM voltage. However, in a switching period, if the reference signal for the PWM is the same for both inverters, the CM voltage averaged over a switching period will be the same for both inverters and the difference of the averaged CM voltages will be zero. This results in zero circulating current averaged in a switching period according to (1). However, in a practical case when dead time is not neglected there are some cases which result in nonzero circulating current. The analysis for the CM voltage when the dead time is not neglected is presented in the following section.

Effect of Dead-Time on Circulating Current

In a leg of a two-level inverter shown in Fig. 2, there is a time delay between the turn-off of the one device in a leg and the turn-on of the other device in the same leg. This delay is referred to as the dead-time, and both devices are off during this time. In the previous section, it is assumed that the dead-time is zero. The effect of the dead-time is analyzed in this section for space vector PWM (SVPWM) and DPWM3. The assumptions made for the analysis are that the current is in-phase with the reference voltage and the phase currents do not change sign in a switching period. Since the

current is in-phase with the reference voltage, the current direction is positive for positive reference voltage, and the current direction is negative for negative reference voltage. If the current direction is positive, the bottom diode of the inverter leg will conduct during the dead-time, and the ac terminal voltage will be $-v_{dc}/2$. Similarly, if the current direction is negative, the top diode of the inverter leg will conduct during the dead-time, and the ac terminal voltage will be $+v_{dc}/2$.

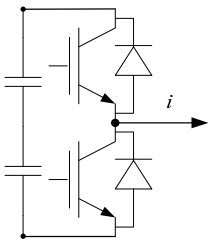


Fig. 2. A leg of a two-level inverter.

The ac terminal voltages and the difference between the terminal voltages of the phases for SVPWM are plotted in Fig. 3. The dotted curves show the ideal condition without the dead-time, while the solid lines show the different plots with the dead-time. The point to be noted here is that the reference signals for both inverters are the same and updated at the same time. If there is no dead-time, it can be shown that the average value of the CM voltage for both inverters is the same and the difference between the CM voltages is zero. Therefore, there is no low frequency component in the circulating current.

During the dead-time, the ac terminal voltage is $-v_{dc}/2$ for phase *A* and *B* because of positive current, and the rising edge of the ac terminal voltages are delayed by the dead-time (t_d). The opposite is true for phase *C*, and the falling edge of the ac terminal voltage is delayed by the dead-time. Due to this, the difference between the ac terminal voltages of a phase has different waveform compared to the ideal condition. It can be shown that the time for which the difference between phase A terminal voltages is $-v_{dc}$ is equal to the time for which it is $+v_{dc}$, and it is equal to $2t_a + t_d$ which is shown in Fig. 3. This means that the average value of the difference of phase *A* terminal voltages is zero. Similarly, it can be shown that the average values of phase *B* and phase *C* ac terminal voltages difference are zero. This implies that

$$v_{cm1} - v_{cm2} = 0 \tag{3}$$

Similar analysis can be done for a DPWM. The DPMW3 given in [5] is chosen for the analysis. The ac terminal voltages, the difference between the ac terminal voltages of the phases, and the circulating current for the DPWM3 are plotted in Fig. 4. The figure is plotted for a condition when phase *A* discontinues switching and is clamped to the positive dc-link terminal, and phase *C* (which was clamped to the negative dc-link terminal) continues switching. The reference voltage value of phase *B* changes its sign from negative to positive as shown in Fig. 4. Dotted curves in Fig. 4 show the waveform under ideal conditions without the dead-time, while the solid curves show the waveform with the dead-time. As described in the previous analysis of the SVPWM with the dead-time, it can be shown that the time, for which the difference between phase *B* terminal voltages is $-v_{dc}$, is equal to the time for which it is $+v_{dc}$. This means that the average value of the difference between phase *B* terminal voltages is zero, and the average circulating current component due to phase *B* is zero. The same is true for phase *C*. However, phase *A* which has positive reference voltage and positive current and when it clamps to positive dc-link terminal, phase *A* top switch of inverter 1 is switched off at the end of switching period. Due to positive current in the phase, the rising edge of the ac terminal voltage is delayed because of the dead-time which is marked

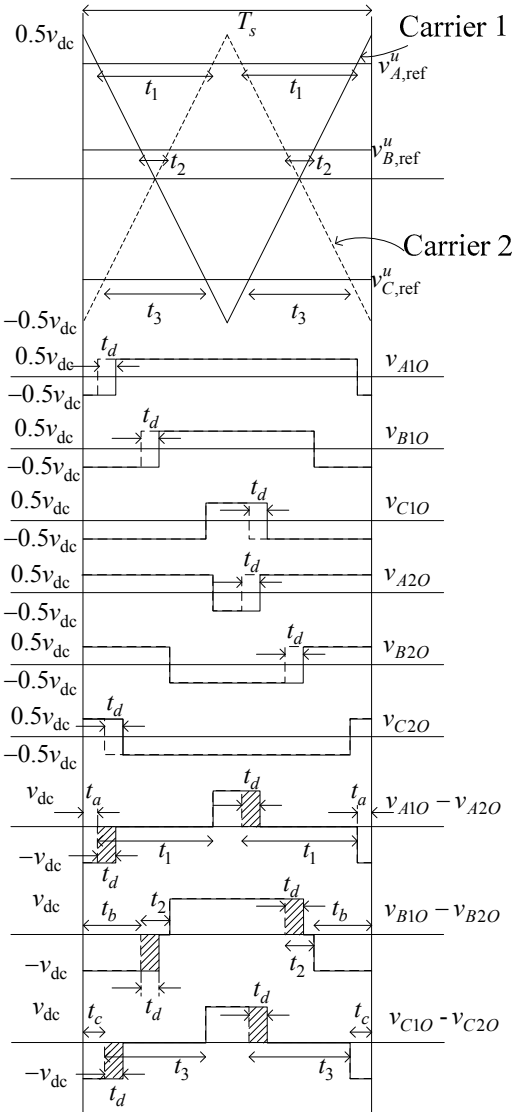


Fig. 3. Difference between the ac terminal voltages of the inverters for SPWM or SVPWM.

in Fig. 4 by a red circle. Therefore, the average value of the difference between phase *A* terminal voltages is not zero and is given by

$$\left\langle v_{A1O} - v_{A2O} \right\rangle_{T_s}\Big|_{\omega t=30^\circ,300^\circ} = -\frac{v_{dc}}{T_s} t_d \tag{4}$$

where T_s is the switching period.

Similar condition will occur for phase *B* at ωt = 180° and 270° and for phase *C* at ωt = 60° and 150°. Due to this, there exists a dc component of the circulating current.

Similarly, when a phase clamps to a negative dc-link voltage, that phase bottom IGBT of inverter 2 is switched off at the end of the switching period, and due to the dead-time there is a delay in the falling edge of the ac terminal voltage for the inverter 2. This in turn causes a nonzero average difference between the ac terminal voltages. The conditions when it occurs for inverter 2 are for phase *A* at ωt = 120° and 210°, phase *B* at ωt = 240° and 330°, and phase *C* at ωt = 90° and 360°. There are 12 switching periods in a fundamental period (T_f) where the average value of the difference between a phase voltages has the value of $-v_{dc}t_d/T_s$. So the

average value of the difference between the common-mode voltages of the two inverters over a fundamental cycle is given by

$$\left\langle v_{cm1} - v_{cm2} \right\rangle_{T_s} \Big|_{\omega t = 30^\circ, 300^\circ} = -\frac{4v_{\mathrm{dc}}}{T_s} t_d$$

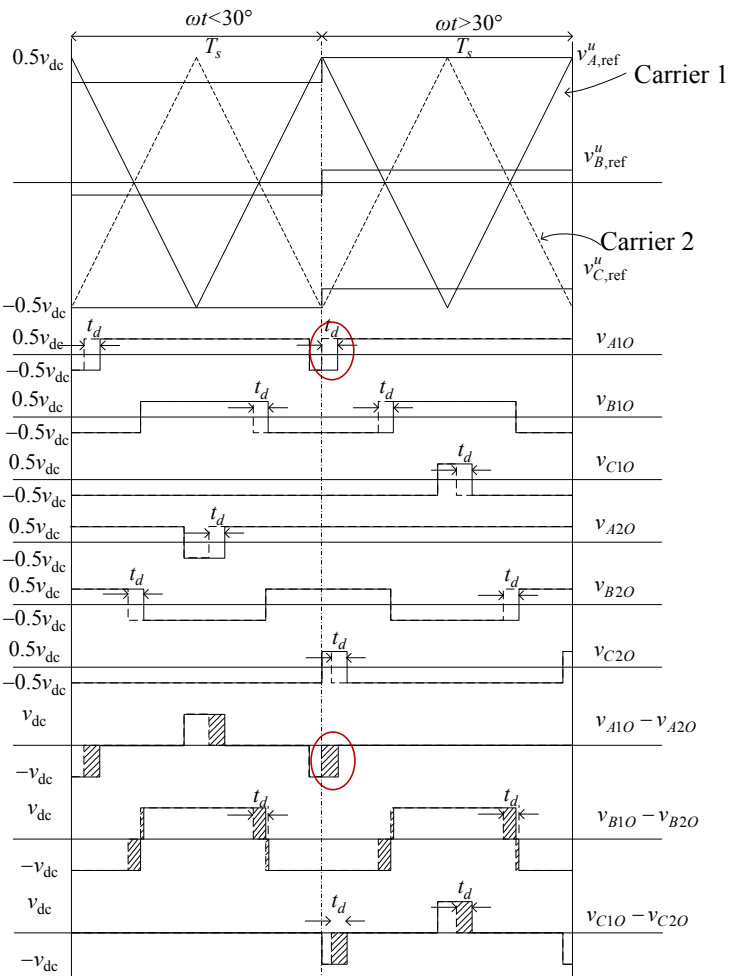


Fig. 4. Difference between the ac terminal voltages of the inverters for DPWM3.

Therefore, a dead time compensation is required to eliminate the dc component. A dead-time compensation technique discussed in [9] is used to remove the dc component of the circulating current

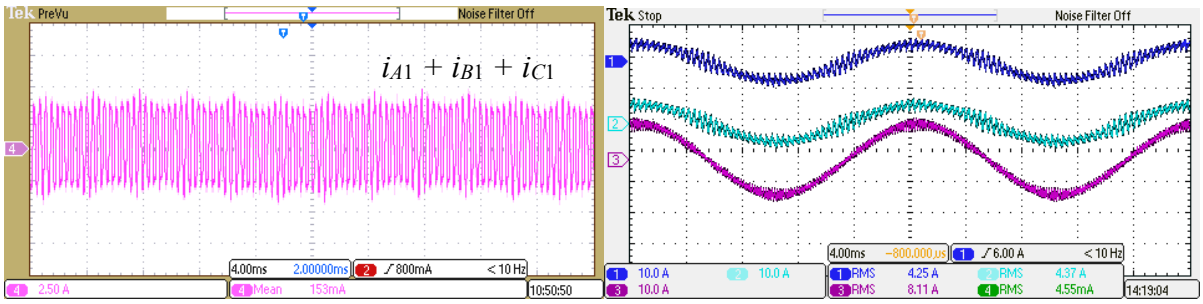
Experimental Results

A two parallel-connected inverters with inductance of the choke in each phase equal to 6.8 mH (L = 6.8 mH) are supplying a three-phase load of 20 Ω. Since the circulating current depends only on the CM voltage, the choice of load does not influence the circulating current. The inverters are operated with dc-link voltage equal to 500 V. The carrier frequency used for modulation is equal to 2.5 kHz. The carrier waveforms of the two inverters are 180° phase shifted. The modulation index used for the experiment is equal to 1.

The sum of the phase currents of inverter 1, when SVPWM is used, is shown in Fig. 5(a). The dead-time used for the experiments is 2 µs. The average value of the sum of the currents, i.e., three times the

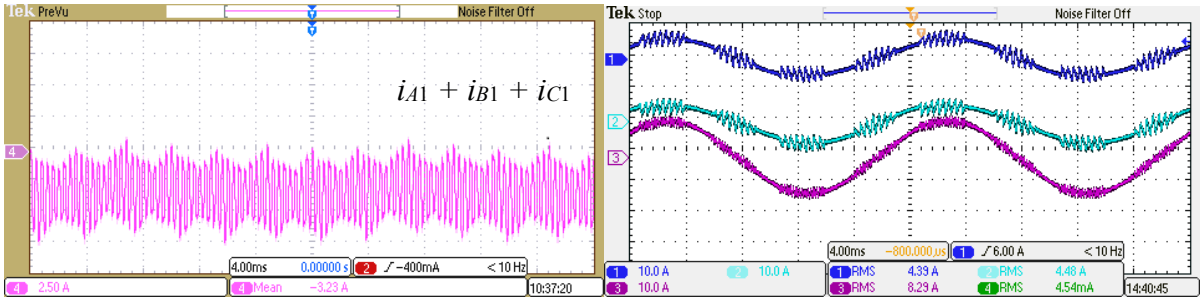
circulating current is zero. The rms value of the circulating current is 0.88 A. Phase A current of inverter 1, inverter 2, and the load current are shown in Fig. 5(b).

The sum of the phase currents of inverter 1 for DPWM3 is shown in Fig. 6(a). Since the dead-time of 2 μs is used, the average value of the sum of the currents, i.e., three times the circulating current is equal to − 3.23 A. Phase A current of inverter 1, inverter 2, and the load are shown in Fig. 6(b). A standard dead-time compensation technique is used with DPWM3 and the results are shown in Fig. 7. It can be seen that the average value of the circulating current is zero. The rms value of the circulating current is 0.77 A. There is a reduction of 12.5% in the rms value of the circulating current, and the dc offset is eliminated.



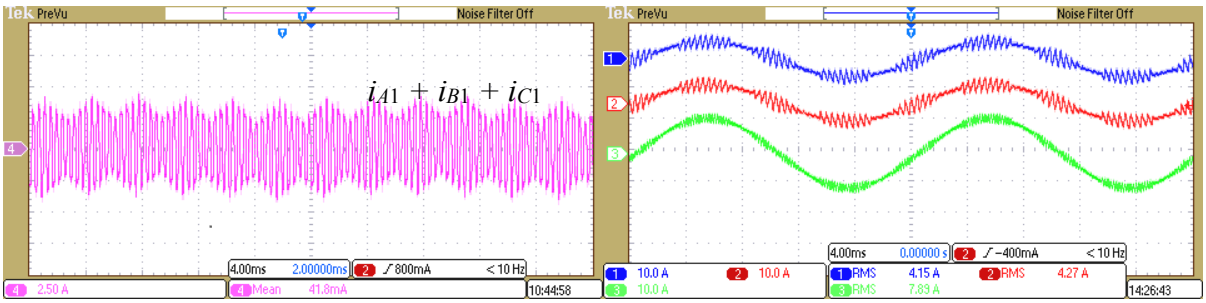
(a) (b)

Fig. 5. (a) Sum of the phase currents of inverter 1, (b) phase *A* current of inverter 1, inverter2, and the load for SVPWM (m = 1).



(a) (b)

Fig. 6. (a) Sum of the phase currents of inverter 1, (b) phase *A* current of inverter 1, inverter2, and the load for DPWM3 (m = 1).



(a) (b)

Fig. 7. (a) Sum of the phase currents of inverter 1, (b) phase *A* current of inverter 1, inverter2, and the load for DPWM3 with the dead-time compensation.

Conclusion

This paper presents an analysis of the CM voltage for two parallel-connected inverters which causes the circulating current. The analysis shows that the average value of the circulating current over a switching period will be zero if the reference voltage signals for both converters are the same. It means

that there will not be any low order harmonics in the circulating current in this condition. It is shown that the DPWM with the dead-time causes a dc component in the circulating current, and it can be made zero if the dead-time compensation is provided. The experimental results are presented to verify the analysis.

References

[1] Fukuda S., Matsushita K.: Control method for parallel-connected multiple inverter systems, in Proc. 7th Int. Conf. Power Electron. Variable Speed Drives, London, U.K.1998, pp. 175- 180

[2] Asiminoaei L., Aeloiza E., Enjeti P. N., and Blaabjerg F.: Shunt active-power-filter topology based on parallel the interleaved inverters, IEEE Trans. Ind. Electron. vol. 55 no. 3 pp. 1175–1189 Mar. 2008

[3] Abusara M. A. and Sharkh S. M.: Design and control of a grid-connected the interleaved inverter, IEEE Trans. Power Electron. vol. 28 no. 2 pp. 748–764 Feb. 2013

[4] Xiaolin Mao, Jain A. K., and Ayyanar R.: Hybrid the interleaved space vector PWM for ripple reduction in modular converters, IEEE Trans. Power Electron. vol.26 no.7 pp.1954–1967 July 2011

[5] Hava A.M., Kerkman R. J., and Lipo T. A.: Simple analytical and graphical methods for carrier-based PWM-VSI drives, IEEE Trans. Power Electron. vol. 14 no. 1 pp. 49–61 Jan. 1999

[6] Zhihong Ye, Boroyevich D., Jae-Young Choi, and Lee F. C.: Control of circulating current in two parallel three-phase boost rectifiers, IEEE Trans. Power Electron. vol.17 no.5 pp.609–615 Sep 2002

[7] Kun Xing; Lee F. C., Borojevic D., Zhihong Ye, and Mazumder S.: The interleaved PWM with discontinuous space-vector modulation, IEEE Trans. Power Electron. vol.14 no.5 pp.906–917 Sep 1999

[8] Chen T. P.: Circulating zero-sequence current control of parallel three-phase inverters, IEE Proc. Electric Power Applications vol. 153 no. 2 pp.282–288 March 2006

[9] Holmes G. and Lipo T.: Pulse Width Modulation for Power Converters, Principles and Practice, ser. IEEE Press Series on Power Engineering. New York: Wiley-Interscience 2003