An Open-Loop 28GHz 16-Phase Clock Generator in 28nm CMOS

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***Abstract*—This paper presents an open-loop 28GHz 16-phase clock generator in 28nm CMOS technology. The open loop architecture is composed of 22.5° delay units and uses phase compensation to account for delay time variations. The 16-phase 28GHz clock generator consumes 14mW, leading to a power efficiency of 0.032mW/GHz/phase. The maximum phase error is 6° and the RMS phase error is 3° when the input frequency varies from 27GHz to 29GHz.**

Keywords—multiphase clock generator, open-loop.

I. INTRODUCTION

Multi-phase clocks are desired in many high-speed applications such as wireless communication systems and time-interleaved ADCs. Recently, the 28GHz frequency band has become an attractive candidate for 5G networks [1]. This is due to the favorable channel characteristics in this frequency band and the feasibility to realize highly integrated high-performance hardware in silicon at this frequency range [2]. Due to a larger propagation loss around 28GHz compared with the frequency band used in existing wireless systems, beamforming techniques are essential in establishing reliable wireless communication links. It is estimated that the required number of antennas could be orders of magnitude larger than current wireless systems [3]. A generally agreed approach in the receiver design is to first phase-shift each antenna signal with a proper amount of delay in the carrier frequency band, and then to combine the phased-shifted signals before demodulation. This reduces the hardware complexity by using much less demodulation hardware, compared with the approach of demodulating each antenna signal. It does require phase-shifters to provide controllable phase shifts operating around the carrier frequency. Phase shifters [2, 4] operating in the 28GHz range have been reported. However, these phase shifters generally require inductors and can consume prohibitively large die areas for large antenna arrays desired in 5G systems. An alternative approach is to sample each antenna signal at the appropriate phase and later combine the samples to realize beamforming. In this approach, there is no need to delay the antenna signals using phase shifters and the required die area is considerably smaller. To sample the antenna signals at different phases, multi-phase clocks are needed to provide the timing for sampling. Conventionally, multi-phase clocks are generated using closed-loop architectures, such as DLLs or PLLs. However, closed-loop architectures require certain lock-in time for the loop to converge. In addition, PLLs accumulate jitter over time. DLLs contribute less jitter but suffer from narrow frequency range and false locking. Open-loop structures [5-8] have been investigated to avoid issues associated with locked loops and they intrinsically have low jitter. However, the demonstrated frequency of existing open-loop designs is limited to around 1-10GHz. Additionally, the accuracy of the beamforming technique will benefit from more clock phases. Typically, 16 phases (4-bit) have been adopted in most beamforming designs using phase shifters and have been demonstrated with satisfying results.

This paper presents an open-loop 28GHz 16-phase clock generator in 28nm CMOS. A 22.5° phase delay unit design is presented to provide 16 phases. The phase error compensation scheme adopts the same principle as that in [7, 8]. The circuit can generate evenly-spaced 16-phase clocks with a low power of 14mW.

II. CIRCUIT DESIGN

A. Architecture

Fig. 1 shows the architecture of the proposed open-loop 16-phase differential clock generator. It consists of a clock buffer, a delay line of 16 delay units (DUs) and 8 phase interpolators (PIs). The clock buffer is same as the delay unit. Each PI has two differential inputs and one differential output. The solid line represents positive input/output, while the dotted line represents negative input/output. Each DU offers a phase delay of θ, which should be ideally 22.5° for a 16-phase clock generator. In reality, this target phase delay cannot be guaranteed due to PVT variations and θ will deviate from the ideal value. However, taking appropriate phases from the delay line and interpolating them with appropriate weights can compensate for DU delay time variation and generate evenly spaced multi-phase clock. Using the delay compensation technique in [8], the differential outputs of the eight PIs are 8θ+0°, 8θ+22.5°, 8θ+45°, 8θ+67.5°, 8θ+90°, 8θ+112.5°, 8θ+135° and 8θ+157.5°, as derived in Fig. 1. The opposite polarities of the differential outputs provide the other eight phases to obtain a total of 16 phases. Although the absolute phase position for the clock in each PI is a function of θ, the relative phase spacing remains 22.5°, independent of θ. Therefore, when θ deviates from the ideal 22.5° phase delay, the design can still generate 16-phase evenly spaced clocks.

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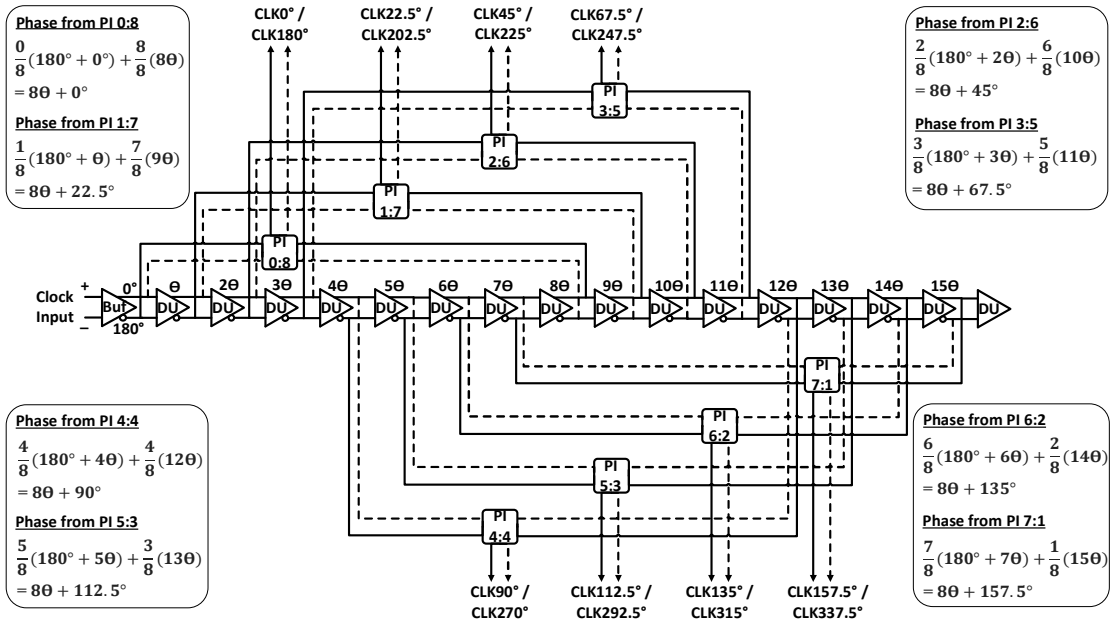

Fig. 1. The architecture of the open-loop 16-phase differential clock generator

However, there is a limitation on how much θ can deviate from the ideal 22.5° shift. The limitation is set by the interpolation capability of the PI.

B. Delay Unit

The delay unit is used in a 16-phase clock generator, thus it is required that the phase delay of each delay cell is 22.5° at the input frequency. In order to achieve good accuracy, the output clock for each DU along the delay chain should have similar amplitude. Fig. 2 shows the schematic of the proposed delay unit design. Fully-differential structure is used to improve noise rejection, increase output swing range and limit the power consumption. PMOS-based level-shifted active inductor loads are used to provide wider bandwidth. The level-shifted active inductor load and its small signal model are circled by dashed box in Fig. 2. In its small signal model, g_{m3} and g_{m5} are the transconductance of transistors M3 and M5, respectively. C is the capacitor introduced by transistor M9, which is used as MOS capacitor here. Transistors M5 and M7 comprise the source follower. The source follower provides a voltage level shift between the gate and drain of M3, which will reduce the headroom consumption across M3 [7]. From the small signal model, we can calculate the equivalent impedance Z_{eq} of the level shifted active load as expressed in Fig. 2. The equivalent impedance is comprised of an effective resistance R_{eff} in series with an effective inductor L_{eff}, whose values are $1/g_{m3}$ and $C/g_{m3}g_{m5}$, respectively.

The delay units connect in cascade with the same delay unit as the load, thus the output load can be represented as capacitor C_L. The equivalent circuit for the delay unit is shown in Fig. 3. The load impedance is equivalent to the active load equivalent impedance Z_{eq} in parallel with the load capacitor C_L. Then the transfer function of the delay unit, $A_V(s)$, can be calculated and is expressed in Fig. 3. At low frequency, the DC gain is g_{m1}/g_{m3}. The equation shows that the level-shifted active load introduces a zero at frequency $\omega_Z=g_{m5}/C$ to the transfer function, which helps improve the bandwidth. Further, the RLC based load provides a second order frequency response and introduces two poles. The positions of these two poles depend on the quality factor $Q=\omega_0/\omega_Z$, where ω_0 is the natural frequency.

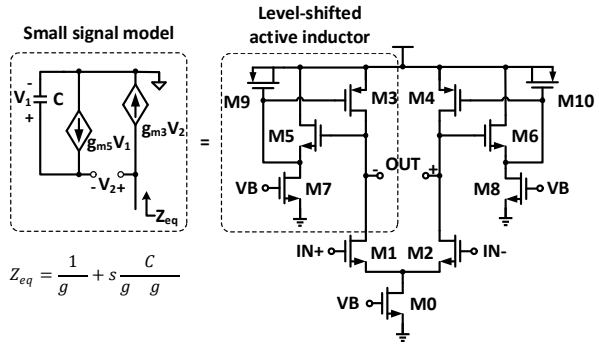

Fig. 2. Delay unit

The delay unit is targeted to have 22.5° phase delay for the input frequency of 28GHz. In order to have relatively constant amplitude gain around the input frequency, it is preferred that the gain peaking occurs at the input frequency. The zero frequency ω_Z is settled smaller than the natural frequency ω_0. Thus, the two poles would be a complex pair, which leads to an amplitude peaking in the frequency response. The zero is placed below the natural frequency ω_0 to obtain the 22.5° phase response at the input frequency. Fig. 4 illustrates the simulated delay unit frequency response. The delay unit has 22.5° phase

shift at 28GHz. The gain at peaking is set close to 0dB. This ensures constant clock amplitude when clock propagates through the delay unit chain.

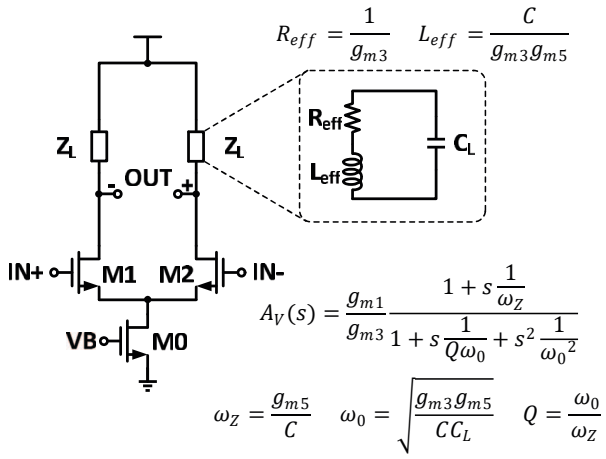

Fig. 3. Delay unit equivalent circuit

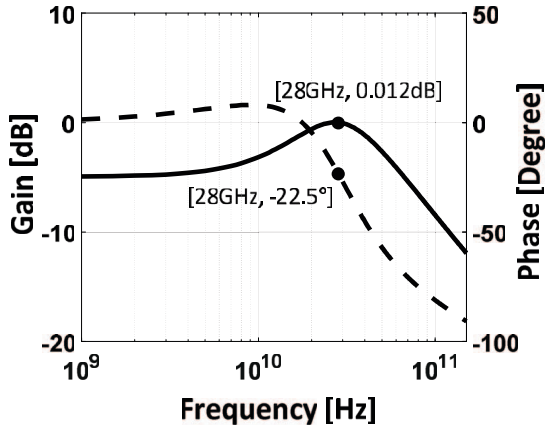

Fig. 4. Simulated delay unit frequency response

C. Phase Interplator

The phase interpolator shown in Fig. 5 is used to obtain wide range of phase interpolation. It has two differential inputs and one differential output. Transistors M1-M4 comprise the two differential input pairs, which are cross-connected to the output nodes. Transistors M5 and M6 are current sources biased by the same biasing voltage. The load is implemented by resistor R. The differential output phase is the sum of the two differential input phases with appropriate weights. The interpolation ratio is realized though the current ratio between transistors M5 and M6. From the architecture in Fig. 1, we can calculate that the phase difference between the two differential inputs for each PI is 180°-8θ. It is ideally 0, when the phase shift θ is 22.5°. As θ deviates from 22.5°, the absolute value of this phase difference will increase. As long as this difference is within the toleration range of the PIs, the outputs will be 22.5° spaced clocks despite the variation of θ. For example, if we assume that the maximum toleration range of the PIs is 90°, the phase shift θ can deviate from the 22.5° by ±11.25°.

III. Simulation Results

The 16-phase clock generator has been designed in STM 28nm CMOS28FDSOI technology and simulated using Cadence Spectre. Fig. 6 shows 8 output clock phases of 0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135°, and 167.5° at 28GHz. From the figure, we can see the clock generator is able to generate evenly spaced multiphase clocks with constant amplitude. Fig. 7 presents the phases of the 8-phase clocks from 27GHz to 29GHz. The deviation from the ideal phase is very small.

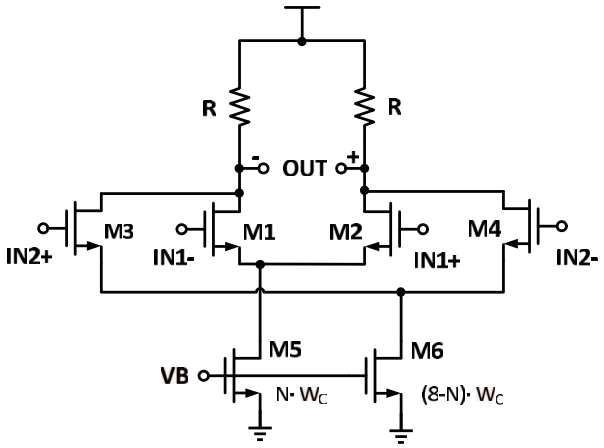

Fig. 5. Phase interpolator

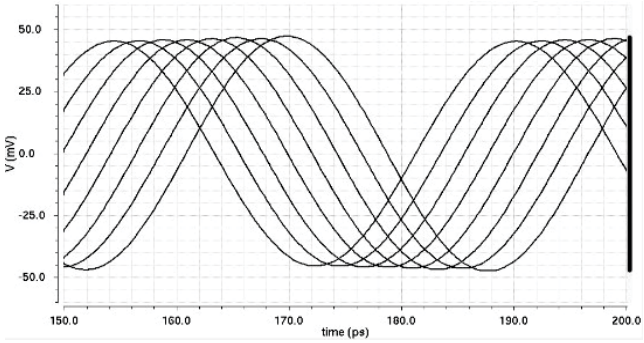

Fig. 6. Multi-phase clock generator outputs.

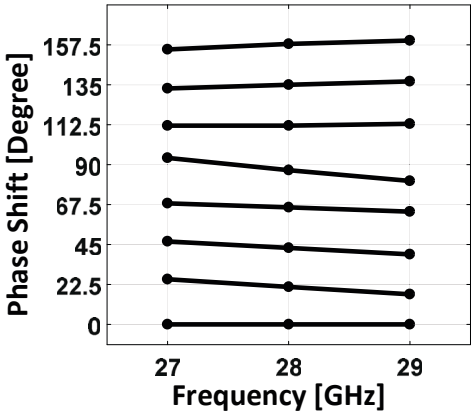

Fig. 7. Phases of the multi-phase clock outputs

Fig. 8 shows the maximum phase error of the output clocks from 27GHz to 29GHz. The phase error here is the difference between measured spacing interval of neighboring clocks and the ideal 22.5° phase interval, which can be expressed as

$$\theta_{error,\mathrm{i}} = \theta_{\Delta i} - 22.5° \quad (1)$$

Where $\theta_{\Delta i}$ means the spacing interval between the $(i+1)^{\text{th}}$ output clock and the i^{th} output clock. The maximum phase error is 2° at 28GHz, and the maximum phase error is less than 6° from 27GHz to 29GHz. This indicates that the open-loop architecture in this design can tolerate the delay variation in delay unit.

Fig. 9 shows the measured RMS phase error among the output clocks. The RMS phase error is defined as

$$\theta_{\Delta,\mathrm{RMS}} = \sqrt{\frac{1}{N-1}\times\sum_{i=1}^{N-1}\left|\theta_{error,i}\right|^2} \quad (2)$$

Where N=8 and $\theta_{error,i}$ is the abovementioned phase error. The RMS phase error is about 0.4° at 28GHz. The multiphase clock generator exhibits less than 3° RMS phase error from 27GHz to 29GHz.

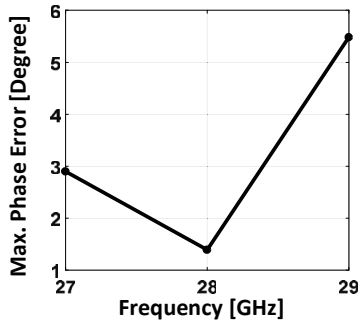

Fig. 8. Maximum phase error among output phases

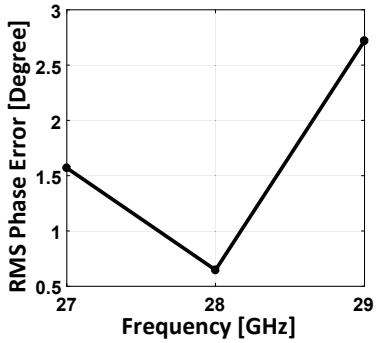

Fig. 9. RMS phase error among output phases

The total DC current consumption is 14mA from a 1V supply voltage at 28GHz, achieving 0.032mW/GHz/phase power efficiency. Table I compares the performance of this design with other open loop multiphase clock generators. It shows that this design reaches higher frequency, generates more clock phases, and achieves better power efficiency.

TABLE I PERFORMANCE COMPARISON

	[5]	[6]	[7]	[9]	**This work**
Architecture	Open Loop	Open Loop	Open Loop	DLL	**Open Loop**
Technology	0.13μm	65nm	65nm	28nm	**28nm**
Phases	4	4	8	16	**16**
Frequency (GHz)	1.2-2.8	0.37-2.5	8-12	0.035-2.26	**27-29**
Power (mW)	30	2.6	14.8	2.7	**14**
Power Efficiency (mW/GHz/Phase)	2.7	0.26	0.19	0.075	**0.032**

IV. CONCLUSION

An open-loop differential 28GHz 16-phase clock generator was presented in this paper. Simulation results show that this design achieved higher operating frequency and more phases, with better power efficiency compared with existing open-loop multi-phase clock generators. The maximum phase errors among the multi-phase clock outputs is below 6° and the RMS phase error among the multi-phase outputs is below 3° from 27GHz to 29GHz. This indicates that the presented design can tolerate delay unit variation.

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