CURRICULUM VITAE

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EDUCATION

1980 Ph.D. University of Illinois, Urbana, Illinois
Department of Electrical Engineering
Thesis “Theoretical Studies of High Field Transport in III-V Semiconductors”

1978 M.S. University of Illinois, Urbana, Illinois
Department of Electrical Engineering
Thesis “ Quantum Size Effects in Single Active Layer LPE
lnGaAsP-lnP Heterostructure Laser Diodes”

1976 B.S.E.E. University of Tokyo, Tokyo, Japan
Department of Electronic Engineering

PROFESSIONAL EXPERIENCE

2010-Present Research Professor , TxACE and Electrical and Computer Engineering
Jonsson School of Engineering & Computer Science
The University of Texas at Dallas

2007-2009 TI Fellow, Low Power CMOS Technology
External Development and Manufacturing
Texas Instruments Inc, Dallas, TX

2004-2007 TI Fellow, Analog/RF Technology CAD (TCAD)
Silicon Technology Development
Texas Instruments Inc, Dallas, TX

2002-2004 TI Fellow, Analog/RF Platform
Silicon Technology Development
Texas Instruments Inc, Dallas, TX

1999-2002 Manager, C05 Embedded Flash and Analog Programs
Silicon Technology Development

	Texas Instruments Inc, Dallas, TX
1998-1999	TI Fellow, C05 Analog CMOS Development Silicon Technology Development Texas Instruments Inc, Dallas, TX
1996-1998	Director, Memory Process Technology Lab Memory R&D Center Texas Instruments Inc, Dallas, TX
1993-1996	Director, Design and Test Technology Lab Semiconductor Process and Device Center Texas Instruments Inc, Dallas, TX
1989-1992	Senior Member of Technical Staff Semiconductor Process and Device Center Texas Instruments Inc, Dallas, TX
1985-1988	Senior Member of Technical Staff Central Research Laboratory Texas Instruments Inc, Dallas, TX
1984-1985	Senior Member of Technical Staff VLSI Design Laboratory Texas Instruments Inc, Dallas, TX
1980-1984	Member of Technical Staff Semiconductor Process Laboratory Texas Instruments Inc, Dallas, TX

PROFESSIONAL AFFLIATIONS

Life Fellow, Institute of Electrical and Electronics Engineers (IEEE)

AWARDS AND HONORS

2008	Technical Program Group member for SRC NRI (Nanoelectronics Research Institute)
2003-2008	Passives Subgroup Chair , ITRS RF and Analog/Mixed-Signal Technologies for Wireless Communications Working Group
2003	Guest Editor, Special Issue on Device Integration Technology for Mixed-Signal SOC, IEEE Transactions on Electron Devices
2002-2003	Subcommittee member, Integrated Circuits and Manufacturing, IEDM
2000	Organizer of 2000 IEDM Short Course “Technology for the Internet Era”
1998-2003	Member of the Advisory Board for the University of Illinois College of

	Engineering
1995-1996	SEMATECH Strategic Technology FTAB Member
1994-1996	SRC Design Sciences PTAB Alternate Member
1994	Elected to TI Fellow Citation: For Technical Expertise and Contributions to the Development of Several Generations of DRAM Technologies.
1992	Elected to IEEE Fellow Citation: For Contribution to the Development of Semiconductor Memories
1992	Conference Chair, 1992 Device Research Conference
1991	Technical Program Chair, 1991 Device Research Conference
1986	Outstanding Paper Award at 1986 IEEE International Solid-State Circuits Conference.
1976	Sankei Newspaper Scholarship

PATENTS

1) 7,250,334 “Metal insulator metal (MIM) capacitor fabrication with sidewall spacers and aluminum cap (ALCAP) top electrode”
2) 6,764,892 “Device and method of low voltage SCR protection for high voltage failsafe ESD applications”
3) 6,753,202 “CMOS photodiode having reduced dark current and improved light sensitivity and responsivity”
4) 6,621,064 “CMOS photodiode having reduced dark current and improved light sensitivity and responsivity”
5) 6,576,959 “Device and method of low voltage SCR protection for high voltage failsafe ESD applications”
6) 6,548,874 “Higher voltage transistors for sub micron CMOS processes”
7) 6,512,280 “Integrated CMOS structure for gate-controlled buried photodiode”
8) 6,392,263 “Integrated structure for reduced leakage and improved fill-factor in CMOS pixel”
9) 6,303,420 “Integrated bipolar junction transistor for mixed signal circuits”
10) 5,959,308 “Epitaxial layer on a heterointerface”
11) 5,894,145 “Multiple substrate bias random access memory device”
12) 5,595,925 “Method for fabricating a multiple well structure for providing multiple substrate bias for DRAM device formed therein”
13) 5,290,719 “Method of making complementary heterostructure field effect transistors”
14) 5,238,869 “Method of forming an epitaxial layer on a heterointerface”
15) 5,214,298 “Complementary heterostructure field effect transistors”
16) 5,164,917 “Vertical one-transistor DRAM with enhanced capacitance and process for fabricating”
17) 5,065,132 “Programmable resistor and an array of the same”
18) 4,914,053 “Heteroepitaxial selective-area growth through insulator windows”
19) 4,910,164 “Method of making planarized heterostructures using selective epitaxial growth”

20)4,713,678 “dRAM cell and method”
21)4,545,034 “Contactless tite RAM”

SEMINARS

1) “DRAM Technology: 1Gbit and Beyond”, MIT MTL VLSI Seminar, October, 1996
2) “Issues in DRAM/Logic Integration”, University of California at Berkeley, April 1996
3) “Overview of DRAM Technology”, UTD Seminar, October 1997
4) “Technology for the Internet Era: Introduction and Overview”, 2000 IEDM Short Course
5) “Integration of Analog/RF Functions into Digital CMOS Process for System-On-a-Chip (SOC)”, TI Internal Engineering Lecture Series, April 2002.

PRESENTATIONS

1) “Band structure dependent impact ionization in Ill-V semiconductors”, H. Shichijo and K. Hess, Industrial Affiliates Program in Physical Electronics, University of Illinois, Urbana, April 1980.
2) “Band structure dependent impact ionization in semiconductors”, K. Hess and H. Shichijo, Physics of Submicron Devices, Colorado State University, Fort Collins, July 1980.
3) “A re-examination of practical scalability limits of n-channel and p-channel MOS devices for VLSI, H. Shichijo”, 1981 IEDM, Washington, D.C., December 1981.
4) “Performance of submicron MOSFET’s fabricated by edge-defined vertical-etch technique”, H. Shichijo, Y.T. Lin, T.C. Holloway, Y.C. Lin and W.R. Hunter, Workshop on the Physics of Submicron Structures, Urbana-Champaign, Illinois, June 28-30, 1982.
5) “Experimental electrical characteristics of submicrometer MOSFETs”, H. Shichijo, Y.T. Lin, T.C. Holloway, Y.C. Lin and W.R. Hunter, Device Research Conference, Ft. Collins, Colorado, June 1982.
6) “Characterization of n-channel and p-channel LPCVD polysilicon MOSFET”, H. Shichijo, S.D.S. Malhi, P.K. Chatterjee, R.R. Shah, M.A. Douglas, and H.W. Lam, 1983 IEDM, Washington D.C., Dec.1983.
7) “N-channel and p-channel LPCVD polysilicon MOSFETs and effects of grain boundary passivation”, H. Shichijo, S.D.S. Malhi, P.K. Chatterjee, R.R. Shah, M.A. Douglas and H.W. Lam, Materials Research Society 1984 Spring Meeting, Albuquerque, Feb.1984.
8) “Small-grain polysilicon MOSFETs on oxide and its applications for VLSI memories”, H. Shichijo, S.D.S. Malhi, P.K. Chatterjee, A.H. Shah, G.P. Pollack, W.F. Richardson, S.K. Banerjee, M. Elahy and R.H. Womack, 17th Industrial Affiliates Program in Physical Electronics, Univ. of Illinois, Urbana, April 1984.
9) “TITE RAM: A new SOI DRAM gain cell for Mbit DRAMs”, H. Shichijo, S.D.S. Malhi, A.H. Shah, G.P. Pollack, W.F. Richardson, M. Elahy, S.K. Banerjee, R.H. Womack and P.K. Chatterjee, 1 6th (1984 International) Conference on Solid State Devices and Materials, Kobe, Japan, August 1984.

10) “The physics of VLSI design: Scaling of MOS devices”, H. Shichijo, IEEE Dallas Student Chapter Meeting, Southern Methodist University, Dallas, Oct. 23,1984.
11) “Polysilicon transistors for VLSI MOS memories (Invited Paper)”, H. Shichijo, S.D.S. Malhi, W.F. Richardson, G.P. Pollack, A.H. Shah, L.R. Hite, S.K. Banerjee, M. Elahy, R. Sundaresan, R.H. Womack, H.W. Lam and P.K. Chatterjee, 1984 IEDM, San Francisco, Dec. 1984.
12) “Process and device considerations for small grain polysilicon transistors (Invited Paper)”, H. Shichijo, S.D.S. Malhi, R. Sundaresan, S.K. Banerjee and H.W. Lam, Materials Research Society 1985 FaIl Meeting, Boston, Dec. 3-6,1985.
13) “Prospects for GaAs-on-Si”, H. Shichijo and J.W. Lee, Industrial Affiliates Program in Physical Electronics, Univ. of Illinois, Urbana, April 1986.
14) “GaAs MESFET on silicon substrate for digital IC applications”, H. Shichijo and J.W. Lee, Materials Research Society 1 986 Spring Meeting, Palo Alto, CA, April 16-18,1986.
15) “GaAs E/D MESFET 1 K-bit static RAM fabricated on silicon substrates”, H. Shichijo, J.W. Lee, W.V. McLevige and A.H. Taddiken, 13th International Symposium on GaAs and Related Compounds, Las Vegas, Sept.28-Oct.1, 1986.
16) “GaAs devices and circuits fabricated in GaAs-on-silicon substrates”, H. Shichijo, Cornell University Seminar, Cornell University, Ithaca, Oct.28, 1986.
17) “Characteristics of n-channel and p-channel heterostructure insulating gate FETs”, H. Shichijo and H.D. Shih, Conference on Selectively Doped Heterostructure Transistors, Keauhou-Kona, Hawaii, Dec.1-6, 1986.
18) “Performance of digital GaAs E/D MESFET circuits fabricated in GaAs-on-Si substrate”, H. Shichijo, J.W. Lee, W.V. McLevige and A.H. Taddiken, 1986 IEDM, Los Angeles, Dec.7-10, 1986.
19) “Prospects for GaAs-on-Si LSI circuits (Invited Paper)”, H. Shichijo, L.T. Tran, R.J. Matyi and J.W. Lee, Materials Research Society 1987 Spring Meeting, Anaheim, CA, April 21-23, 1987.
20) “Overview: Opportunities and Problems of GaAs/Si for digital and Microwave Application”, H. Shichijo, Workshop on Future Opportunities Though GaAs on Silicon, June 1 8-1 9,1 987, Marina del Rey, CA.
21) “GaAs/AlGaAs Heterojunction Emitter-Down Bipolar Circuits Fabricated on GaAs-on-Si Substrates, L.T. Tran, R.J. Matyi, H. Shichijo, H.-T. Yuan and J.W. Lee, 1987 Device Research Conf., June 1987.
22) “GaAs-on-Si Integrated Circuits; Savior for GaAs ? Or for Si ? (Invited Paper)”, H. Shichijo and R.J. Matyi, 1 987 International Electron Device Meeting, Dec. 6-9, 1987, Washington, D.C.
23) “GaAs Devices Fabricated on Si Substrates (Invited Paper)”, H. Shichijo, March Meeting of the American Physical Society, New Orleans, Louisiana, March 21-25, 1988
24) “Cointegration of GaAs MESFET and Si CMOS Circuits Using GaAs-on-Si Epitaxial Growth”, H. Shichijo, R.J. Matyi, and A.H. Taddiken, 1 5th International Symposium on GaAs and Related Compounds, Atlanta, Sept. 11-14, 1988.
25) “GaAs MESFET and Si CMOS Cointegration and Circuit Techniques”, H. Shichijo, A.H. Taddiken, and R.J. Matyi, 1988 GaAs IC Symposium, Nashville, Nov. 6-9, 1988.

26) "Monolithic Process for Co-integration of GaAs and Silicon Circuits", H. Shichijo, R.J. Matyi, and A.H. Taddiken, 1988 International Electron Devices Meeting, 1988 International Electron Devices Meeting, San Francisco, Dec. 11-14,1988.
27) "Material and Processing Issues for GaAs-on-Si Electronic Devices and Cointegration", 1989 State-Of-The-Art Program on Compound Semiconductors (SOTAPOCS X), Los Angeles, May 7-1 2,1989.
28) "Material Problems of GaAs on Si and Application to LSI", 16th International Symposium on GaAs and Related Compounds, Karuizawa, Japan, Sept.25-29, 1989.
29) "Trench Transistor DRAM Cell: Problems and Prospect", SEMI Technology Symposium 90, Chiba, Japan, Oct.22-24, 1990.

PUBLICATIONS

Book Chapters

1) "Full Band Monte Carlo Program for Electrons in Silicon", H. Shichijo, J.Y.Tang, J. Bude and D. Yoder, Chapter 10 in book "Monte Carlo Device Simulation: Full Band and Beyond" edited by Karl Hess, Kluwer Academic Publishers, 1991.
2) "DRAM and SRAM", H. Shichijo, Chapter 7 in book "ULSI Devices" edited by C.Y. Chang and S.M. Sze, John Wiley & Sons, Inc. 2000.

Journals

1) "Tunneling involving defects in LPE In(1 -x)Ga(x)P(1 -z)As(z) (x-0.1 2, z-0.26) double-heterojuction lasers", M.J. Ludowise, E.A. Rezek, H. Shichijo, P.D. Wright, N. Holonyak, Jr. and H.W. Korb, Appl. Phys. Lett. 30, 604 (1977).
2) "GaAs(1 -y)P(y) heterojunction lasers", R.Chin, N.Holonyak, Jr., H. Shichijo, W.O. Groves, D.L Keune and J.A. Rossi, J. Appl. Phys. 48, 3991(1977).
3) "Confined-carrier luminescence of a thin In(1 -x)Ga(x)P(1 -z)As(z) well (x-0.1 3, z-0.29, ~400 A) in a InP p-n junction", E.A. Rezek, H. Shichijo, B.A. Vojak and N. Holonyak, Jr., Appl. Phys. Lett. 31,534(1977).
4) "Tunnel injection into the confined-particle states of an In(1 -x)Ga(x)P(1 -z)As(z) well in InP", E.A. Rezek, N. Holonyak, Jr., B.A. Vojak and H. Shichijo, Appl. Phys. Lett. 31, 703 (1977).
5) "Single and multiple thin-layer (Lz<400A) In(1-x)Ga(x)P(1-z)As(z)-InP heterostructure light emitters and lasers (~1 .1 um, 77K)", E.A. Rezek, N. Holonyak, Jr., B.A. Vojak and H. Shichijo, J. Appl. Phys. 49, 69 (1978).
6) "Continuous operation of visible-spectrum In(1 -x)Ga(x)P(1 -z)As(z) laser diodes (6280 A, 77 K)", R. Chin, H. Shichijo, N. Holonyak, Jr., J.A. Rossi, D.L Keune and D. Finn, IEEE J. Quantum Electron. QE-14, 711(1978).
7) "Carrier collection in a semiconductor quantum well", H. Shichijo, R.M. Kolbas, N. Holonyak, Jr., R.D. Dupuis and P.D. Dapkus, Solid State Comm. 27,1029 (1978).

8) "Photopumped laser operation of MO-CVD AI(x)Ga(1 -x)As near a GaAs quantum well (~6200 A, 77 K)", R.D. Dupuis, P.D. Dapkus, R.M. Kolbas, N. Holonyak, Jr. and H. Shichijo, AppI. Phys. Lett. 33, 596 (1978).
9) "Negative differential resistance through real-space electron transfer", K. Hess, H. Morkoc, H. Shichijo and B.G. Streetman, Appl. Phys. Lett. 35, 469 (1979).
10) "The charge-handling capacity of buried channel structures under hot electron conditions", K. Hess and H. Shichijo, IEEE Electron Devices, ED-27, 503 (1980).
11) "Real-space electron transfer by thermionic emission in GaAsAl(1 -x)Ga(1 -x)As heterostructres: Analytical model for large layer width", H. Shichijo, K. Hess and B.G. Streetman, Solid-State Electron. 23, 81 7 (1980).
12) "Orientation dependence of ballistic electron transport and impact ionization", H. Shichijo, K. Hess and G.E. Stillman, Electron. Lett. 16, 208 (1980).
13) "Monte Carlo simulation of real-space electron transfer in GaAs-AlGaAs heterostructures", T.H. Glisson, J.R. Hauser, M.A. Littlejohn K.Hess, B.G. Streetman and H. Shichijo, J. Appl. Phys. 51, 5445 (1980).
14) "Theoretical and experimental investigation of the dynamics of pulsed laser annealing", A. Bhattacharyya, K. Hess, H. Shichijo and B.G. Streetman, Bull. Am. Phys. Soc. 25, 31 2 (1980).
15) "Simulation of high field transport in GaAs using a Monte Carlo method and pseudopotential band structures", H. Shichijo, K. Hess and G.E. Stillman, Appl. Phys. Lett. 38, 89 (1981).
16) "Measurements of hot electron conduction and real-space transfer in GaAs-AI(x)Ga(1 -x)As heterojunction layers", M. Keever, H. Shichijo, K. Hess, S. Banerjee, L. Witkowski, H. Morkoc and B.G. Streetman, Appl. Phys. Lett. 38, 36 (1981).
17) "Band structure dependent transport and impact ionization in GaAs", H. Shichijo and K. Hess, Phys. Rev. B23, 41 97 (1981).
18) "Theoretical and empirical distributions for ion implantation profile in lnP", J.D. Oberstar, H. Shichijo, M. Keever and B.G. Streetman, Radiation Effects, vol.61, no.1-2, 1982, pp.109-116.
19) "Band-structure dependent impact ionization in silicon and gallium arsenide", J.Y. Tang, H. Shichijo, M. Keever and G.J. lafrate, Proc. Intern. Conf. on Hot Carriers in Semicond., Montpellier, France, July 1981.
20) "A new transmission line model for silicided diffusions: impact on the performance of VLSI circuits", D.B. Scott, W.R. Hunter, and H. Shichijo, 1981 Symposium on VLSI Technology, Maui, Hawaii, Sept.1981.
21) "A re-examination of practical scalability limits of n-channel and p-channel MOS devices for VLSI", H. Shichijo, Tech. Digest, 1981 IEDM, p.119, Washington D.C., Dec.1981.
22) "Technology and design challenges of MOS VLSI (invited paper)", VLSI Laboratory, Texas Instruments, IEEE J. Solid-State Circuits, Vol. SC-17, pp.442,1982.

23) “A new transmission line model for silicided diffusions: impact on the performance of VLSI circuits”, D.B. Scott, W.R. Hunter, and H. Shichijo, IEEE Trans. Electron Devices, Vol. ED-29, pp.651,1982.
24) “Reply to Comments on Simulation of high-field transport in GaAs using a Monte Carlo method and pseudopotential band structures and band-structure dependent transport and impact ionization in GaAs”, K. Hess, J.Y. Tang, K. Brennan, H. Shichijo, and G.E. Stillman, J. AppI. Phys. Vol.53, pp.3327,1982.
25) “A subthreshold load element for high density static RAM”, K.L. Wang, A.H. Shah, H. Shichijo, C. Gosmeyer, and P.K. Chatterjee, Tech. Digest, 1982 IEDM, p.628, San Francisco, Dec.1982.
26) “Experimental Electrical Characterization of Submicrometer MOSFETs (abstract)”, H. Shichijo, Y.T. Lin, T.C. Holloway, Y.C. Lin, and W.R. Hunter, IEEE Trans. Electron Devices, Vol. ED-29, pp.1661, 1982.
27) “Modeling of small MOS devices and device limits”, P.K. Chatterjee, P. Yang, and H. Shichijo, lEEE Proc., Vol.1 30, pp.1 05-126,1983.
28) “Characteristics of p-channel MOSFETs in LPCVD polysilicon and effect of grain boundary passivation on device performance (abstract)”, S.D.S. Malhi, R.R. Shah, P.K. Chatterjee, H.W. Lam, R.F. Pinizzotto, C.E.C. Chen, H. Shichijo, and D.W. Bellavance, IEEE Trans. Electron Devices, Vol. ED-30, no.11, pp.1603,1983.
29) “P-channel MOSFETs in LPCVD polysilicon”, S.D.S. Malhi, P.K. Chatterjee, R.F. Pinizzotto, H.W. Lam, C.E.C. Chen, H. Shichijo, R.R. Shah and D.W. Bellavance, IEEE Elect. Device Lett., Vol. EDL-4, pp.369, 1983.
30) “A re-examination of practical performance limits of scaled n-channel and p-channel MOS devices for VLSI”, H. Shichijo, Solid-State Electron., Vol.26, pp.969,1983.
31) “Characterization of n-channel and p-channel LPCVD polysilicon MOSFETs”, H. Shichijo, S.D.S. Malhi, P.K.Chatterjee, R.R. Shah, M.A. Douglas, and H.W. Lam, Tech. Digest, 1983 IEDM, p.202, Washington D.C., Dec.1983.
32) “Effects of grain boundary passivation on the characteristics of p-channel MOSFETs in LPCVD polysilicon”, S.D.S. Malhi, R.R. Shah, H. Shichijo, R.F. Pinizzotto, C.E. Chen, P.K. Chatterjee, and H.W. Lam, Electron. Lett., Vol.19, no.23, pp.993-994, Nov.1983.
33) “Performance of submicron MOSFETs fabricated by edge-defined vertical etch technique”, H. Shichijo, Y.T. Lin, T.C. Holloway, Y.C. Lin and W.R. Hunter, The Physics of Submicron Structures, pp.11 5-1 25, Plenum Press, 1984.
34) “TITE RAM: A new SOI DRAM gain cell for Mbit DRAMs”, H. Shichijo, S.D.S.Malhi, A.H. Shah, G.P. Pollack, W.F. Richardson, M. Elahy, S. Banerjee, R. Womack, and P.K. Chatterjee, Extended Abstracts of the 1 6th (1984 International) Conference on Solid State Devices and Materials, Kobe, Japan, 1984, pp.265-268.
35) “Hydrogen Passivation of Polysilicon MOSFETs from a plasma nitride source”, G.P. Pollack, W.F. Richardson, S.D.S. Malhi, T. Bonifield, H. Shichijo, S. Banerjee, M. Elahy, A.H. Shah, R. Womack, and P.K. Chatterjee, IEEE Electron Device Lett., Vol. EDL-5, no.11, pp.468-470, Nov.1984.

36) “Comparison of accumulation and inversion mode LPCVD polysilicon MOSFET characteristics for memory applications (abstract)”, S.K. Banerjee, M. Elahy, H. Shichijo, G.P. Pollack, W.F. Richardson, S.D.S.Malhi, A.H. Shah, P.K. Chatterjee, H.W. Lam and R.H. Womack, IEEE Trans. Electron Devices, Vol. ED-31, No.12, pp.1983, Dec.1984.

37) “Polysilicon transistors in VLSI MOS memories (invited paper)”, H. Shichijo, S.D.S. Malhi, W.F. Richardson, G.P. Pollack, A.H. Shah, L.R. Hite, S.K. Banerjee, M. Elahy, R. Sundaresan, R.H. Womack, H.W. Lam and P.K. Chatterjee, Tech. Digest, 1984 IEDM, p.228, San Francisco, Dec.1984.

38) “N-channel and p-channel LPCVD polysilicon MOSFET:s and effects of grain boundary passivation”, H. Shichijo, S.D.S. Malhi, P.K. Chatterjee, A.H. Shah, G.P. Pollack, W.H. Richardson, R.R. Shah, M.A. Douglas and H.W. Lam, Mat. Res. Soc. Symp. Proc. Vol.33, pp.193-198 (1984).

39) “Trench Capacitor Leakage in Mbit DRAMs”, M. Elahy, H. Shichijo, P.K. Chatterjee, A.H. Shah, S.K. Banerjee and R.H. Womack, Tech. Digest, 1984 IEDM, p.248, San Francisco, Dec.1984.

40) “Characteristics and three-dimensional integration of MOSFETs in small-grain LPCVD polycrystalline silicon”, S.D.S. Malhi, H. Shichijo, S.K. Banerjee, R. Sundaresan, M. Elahy, G.P. Pollack, W.F. Richardson, A.H. Shah, L.R. Hite, R.H. Womack, P.K. Chatterjee and H.W. Lam, IEEE J. Solid-State Circuits, Vol. SC-20, No.1, pp.1 78-201, Feb.1985.

41) “Trench capacitor leakage in high-density DRAMs”, M. Elahy, H. Shichijo, P.K. Chatterjee, A.H. Shah, S.K. Banerjee and R.H. Womack, IEEE Electron Device Lett., Vol. EDL-5, No.1 2, pp.527-530, Dec.1984.

42) “Modeling of accumulation-mode MOSFETs in polysilicon thin films”, S.S. Ahmed, D.K. Kim and H. Shichijo, IEEE Electron Device Lett., Vol. EDL-6, pp.313-315,1985.

43) “Anomalous leakage current in LPCVD polysilicon MOSFETs”, J.G. Fossum, A. Ortiz-Conde, H. Shichijo, and S.K. Banerjee, IEEE Trans. Electron Devices, Vol. ED-32, No.9, pp.1878-1884, Sept.1985.

44) “Application of polysilicon transistors for 3-dimensional LSI memories (in Japanese)”, H. Shichijo, S.D.S. Malhi, R. Sundaresan, L.R. Hite, G.P. Pollack, A.H. Shah, H.W. Lam and P.K. Chatterjee, Nikkei Electronics, Oct.1985.

45) “A trench transistor cross-point DRAM cell”, W.F. Richardson, D.M. Bordelon, G.P. Pollack, A.H. Shah, S.D.S. Malhi, H. Shichijo, S.K. Banerjee, M. Elahy, R.H. Womack, C-P. Wang, J. Gallia, H.E. Davis and P.K. Chatterjee, Tech. Digest 1985 IEDM, p.714, Washington D.C., Dec.1985.

46) “A 4Mbit DRAM with cross-point trench-transistor cell”, A.H. Shah, C-P. Wang, H. Shichijo, R.H. Womack, J.D. Gallia, H.E. Davis, M. Elahy, S.K. Banerjee, G.P. Pollack, W.F. Richardson, D.M. Bordelon, S.D.S. Malhi, C. Pilch, B. Tran and P.K. Chatterjee, 1 986 IEEE ISSCC, Digest of Tech. Papers, p.268, Feb.1986.

47) “Trench transistor DRAM cell”, H. Shichijo, S.K. Banerjee, S.D.S. Malhi, G.P. Pollack, W.F. Richardson, D.M. Bordelon, R.H. Womack, M. Elahy, C-P. Wang, J. Gallia, H.E. Davis, A.H. Shah, and P.K. Chatterjee, IEEE Elect. Dev. Lett., Vol. EDL-7, no.2, pp.119-121, Feb.1986.

48) “Characterization of trench transistors for 3-D memories”, S.K. Banerjee, H. Shichijo, A. Nishimura, A.H. Shah, G.P. Pollack, W.F. Richardson, M. Bordelon, S.D.S. Malhi, M. Elahy, R.H. Womack, C-P. Wang, J. Gallia, H.E. Davis and P.K. Chatterjee, 1986 Symp. on VLSI Technology, Digest of Tech. Papers, VII-4, pp.79-80, May, 1986.

49) “Fabrication of 4Mbit CMOS dynamic RAM using trench transistor cell (in Japanese)”, H. Shichijo, A.H. Shah, C-P. Wang, R.H. Womack, J.D. Gallia, H.E. Davis, M. Elahy, S.K. Banerjee, G.P. Pollack, R.F. Richardson, D.M. Bordelon, S.D.S. Malhi, H.V. Tran, I-F. Wang, and P.K. Chatterjee, Nikkei Electronics, July 1986.

50) “A comprehensive analytic model for accumulation-mode MOSFET’s in polysilicon thin films”, D.M. Kim, S. Ahmed and H. Shichijo, IEEE Trans. Elect. Devices, Vol. ED-33, no.7,pp.973-985, July 1986.

51) “A 4Mb DRAM with trench-transistor cell”, A.H. Shah, C-P. Wang, R.H. Womack, J.D. Gallia, H. Shichijo, H.E. Davis, M. Elahy, S.K. Banerjee, G.P. Pollack, W.F. Richardson, D.M. Bordelon, S.D.S. Malhi, C. Pilch, B. Tran and P.K. Chatterjee, IEEE J. Solid-State Circuits, Vol. SC-21, no.5, pp.618-626, Oct.1986.

52) “Process and device considerations for small grain polysilicon transistors (Invited paper)”, H. Shichijo, S.D.S. Malhi, R. Sundaresan, S.K. Banerjee and H.W. Lam, Materials Research Society Symposia Proceedings, Vol.53, pp.419-428, 1986.

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