1. Consider the following different generations/types of operating systems.
   a. Multi-programming time sharing systems.
   b. Multi-programming batch systems.
   c. Pure batch systems.
   d. Personal computers that mainly focus on single users.
   e. An embedded computer that is used on your car to regulate the brake system. (It takes speed and brake pedal pressing level as input and brake pressure as output. The system has a simple CPU and some memory, but no disk.)
   f. A real time system that handles urgent events with different priorities. When a low priority task is in execution and some high priority tasks arrive, the system should switch to execute the one with the highest priority.

Which ones require an interrupt vector? For those that do require an interrupt vector, discuss what types of interrupts are required. For those that do not need an interrupt vector, discuss why not.

2. Consider the following pseudo assembly code for computing c = a + b. Assume that a, b, and c are assigned to consecutive memory “words” (memory is generally addressed byte by byte and assume that a word is 4 bytes) and address for “a” is 0x0000e308. Also, we have a = 20, b = 136, and c = 0 at the starting time. Assume that the first instruction of the code is stored in 0x00001018. Also, each instruction has the opcode in the first byte (most significant byte) and the remaining 3 bytes specify the corresponding address. The opcode for load is 1, store is 2, and add is 3.
   load a
   add b
   store c

(a) Show the memory addresses and contents for all the instructions and data involved. Use the format as follows to express your answer (but the following is not the answer). For all data, use hexadecimal representation.

<table>
<thead>
<tr>
<th>addresses</th>
<th>contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00002104</td>
<td>0x00000001</td>
</tr>
<tr>
<td>0x00002108</td>
<td>0x00000002</td>
</tr>
<tr>
<td>……</td>
<td>……</td>
</tr>
</tbody>
</table>

(b) Write the micro instructions for the code segment. Assume that current PC (program counter) is 0x00001018. For each micro-instruction, also indicate the data that is transferred (if it is a memory access). For all data, use the hexadecimal representation. The following are the first two micro-instructions and the data transferred. Complete the rest.

<table>
<thead>
<tr>
<th>Micro-instructions</th>
<th>data</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC → MAR</td>
<td>0x00001018</td>
</tr>
<tr>
<td>M → MBR</td>
<td>0x0100e308</td>
</tr>
</tbody>
</table>

3. Assume that at time 5 no system resources are being used except for the processor and memory. Now consider the following events:

At time 5: P₁ executes a command to read from disk unit 3.
At time 15: P₅'s time slice expires.
At time 18: P₇ executes a command to write to disk unit 3.
At time 20: P₃ executes a command to read from disk unit 2.
At time 24: \( P_5 \) executes a command to write to disk unit 3.
At time 28: \( P_3 \) is swapped out.
At time 33: An interrupt occurs from disk unit 2: \( P_3 \)'s read is complete.
At time 36: An interrupt occurs from disk unit 3: \( P_1 \)'s read is complete.
At time 38: \( P_8 \) terminates.
At time 40: An interrupt occurs from disk unit 3: \( P_3 \)'s write is complete.
At time 44: \( P_3 \) is swapped back in.
At time 48: An interrupt occurs from disk unit 3: \( P_5 \)'s write is complete.

For each time 22, 37, and 47, identify which state each process is in. If a process is blocked, further identify the event on which it is blocked.

4. Consider an assembly language with only four operations, load, store, add, and mul (multiplication). The following code is in a high-level language. Translate the code into the assembly language.

```plaintext
int a, b = 0;
a = 8;
b = a + 5;
```

Indicate in the assembly code, at which points, there are potential of context switches.

5. Additional questions will be given as the class goes.