

# Bayesian Inference with Muller C-Elements

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*Abstract*— Bayesian inference is a powerful approach for integrating independent conflicting information for decision-making. Though an important component of robotic, biological, and other sensory-motors systems, general-purpose computers perform Bayesian inference with limited efficiency. Here we show that Bayesian inference can be efficiently performed with stochastic signals, in which probabilities are represented by clocked bitstreams. This scheme is particularly adapted to novel low power nanodevices that exhibit faults and device variations. A simple Muller C-element directly implements Bayes' rule. Complex inferences can be performed by C-element trees, which compute the probability of an event based on multiple independent sources of evidence. A naïve Bayesian spam filter circuit is demonstrated as a pedagogical application, and design techniques for improving circuit functionality are described. Limitations of this structure are discussed in terms of signal autocorrelation. The stochastic inference structure is exceptionally robust to faults, an essential feature of decision circuits, and can therefore leverage the increased efficiency of emerging nanodevices. This hardware implementation of Bayesian inference is extremely area and power efficient, with an area-energy-delay product several orders of magnitude less than the conventional floating point implementation. These results open a pathway for a direct stochastic hardware implementation of Bayesian inference, enabling a new class of embedded decision circuits for robotics and medical applications. *This work was supported by the FP7 ICT BAMBI project (FP7-ICT-2013-C).*

*Keywords*— stochastic computing, Muller C-element, fault-tolerant circuit design, nanotechnology, variation-prone devices

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