Emitter-coupled spin-transistor logic

Joseph S. Friedman a,*, John A. Peters b, Gokhan Memik a, Bruce W. Wessels a,b, Alan V. Sahakian a,c

a Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL, United States
b Department of Materials Science and Engineering, Northwestern University, Evanston, IL, United States
c Department of Biomedical Engineering, Northwestern University, Evanston, IL, United States

HIGHLIGHTS

● First logic family with magnetoresistive semiconductor heterojunction transistors.
● Spintronic logic family with cascadable stages.
● High-permeability shielding material concentrates magnetic field.
● First logic family based on ECL to use the spin-degree of freedom.
● Potential to replace CMOS for general-purpose computing.

ARTICLE INFO

Article history:
Received 20 February 2013
Received in revised form 12 August 2013
Accepted 21 August 2013
Available online 5 September 2013

Keywords:
Beyond-CMOS
Spintronics
Magnetoresistance
Magnetoresistive transistor
Magnetic bipolar transistor
Spintronic logic
Bipolar magnetoresistive semiconductor heterojunction transistor

ABSTRACT

The recent invention of magnetoresistive bipolar spin-transistors makes possible the creation of new spintronic logic families. Here we propose the first logic family exploiting these devices, extending emitter-coupled logic (ECL) to achieve a greater range of basis logic functions. By placing the wire from the output stage of ECL logic elements near spin-transistors in other logic stages throughout the circuit, additional basis logic elements can be realized. These new logic elements support greater logic minimization, resulting in enhanced speed, area, and power characteristics. A novel magnetic shielding structure provides this logic family with the crucial ability to cascade logic stages. This logic family potentially achieves a power-delay product 10–25 times smaller than conventional ECL, and can therefore be exploited to increase the performance of very high-speed logic circuits while broadening the range of design choices for a variety of electronic applications.

© 2013 Elsevier Inc. All rights reserved.

1. Introduction

The ability to switch a logic gate through control of electron spin is the fundamental concept underlying spintronic logic circuits. By using electron spin along with charge, new avenues for manipulating signal flow become available [29]. It is therefore possible to develop logic devices with additional capabilities that are more efficient, leading to logic circuits with improved characteristics [31]. In this paper we present a logic family exploiting a newly developed spintronic switch. The power dissipation of circuits made from this logic family is nearly independent of frequency, providing an advantage over CMOS for very high-speed applications.

The recent invention of the bipolar magnetic junction transistor makes possible a new class of logic families [14,27]. This “spin-transistor” provides large signal amplification, and the ability to exploit spin as an additional control allows for the modification and improvement of existing logic families. Emitter-coupled logic (ECL), a bipolar family used in very high-speed electronics [19], can be modified and improved using spin-transistors. Circuits designed with ECL and potentially our new ECL-based logic families dissipate minimal dynamic power, causing the power dissipation to be nearly frequency-independent. This characteristic is in contrast to CMOS circuits, in which dynamic power dissipation increases proportionally with frequency, as depicted in Fig. 1. The power dissipation of the emitter-coupled spin-transistor logic family is significantly less than ECL across all frequencies. A leftward shift in the frequency at which the two design styles intersect can be noted, making this logic family an effective technology for high-speed applications.
The improved characteristics of this logic family are derived from exploiting the magnetic properties of the spin-transistors. We have constructed emitter-coupled spin-transistor logic circuits by routing the ECL differential amplifier currents to create magnetic fields that control the state of spin-transistors. This technique reduces current consumption, and allows for the logic stages to be cascaded similarly to conventional ECL circuits. The number of stages and devices required to implement logic functions is decreased, producing logic circuits that are superior in terms of speed, power, and area without any significant tradeoffs. In summary, the contributions of this work are:

- the first logic family based on magnetoresistive semiconductor heterojunction transistors,
- a spintronic logic family with cascadable stages using a high-permeability shielding material to concentrate a magnetic field, and
- the first logic family based on high-speed ECL structures making use of the spin-degree of freedom.

2. Spintronics background

The spin of an electron is a quantity that signifies its magnetic state within an atomic orbital and is related to its angular momentum. The spin of every electron is either positive or negative, and the Pauli exclusion principle prevents two electrons with similarly signed spins from occupying the same quantum state. Therefore, the total net spin of the electrons in most conventional materials is close to zero. In magnetic materials, interestingly, the presence of significant net spin magnetization results in a rich set of physical phenomena. While electron spin has found a ready application for computing in memory structures such as hard drives and magnetoresistive random-access memory (MRAM), the difficulty in cascading these devices has prevented its incorporation in logic structures.

2.1. Datta–Das current modulator

The original spintronic logic device is the field effect transistor proposed by Datta and Das in 1990 [9]. In their proposed switch, a source and drain composed of iron are separated by a semiconductor. The conductivity of electrons through the semiconductor is affected by the relative orientation of the spin in the semiconductor and iron boundaries. A gate voltage controls the spin-precession of electrons moving between the source and drain, thus controlling the flow of current through the transistor. There are many issues with this design, including the requirement that spin-polarized current be efficiently injected into the channel. This requires overhead for cascaded circuits that significantly degrades the utility of the current modulator.

2.2. Current-controlled magnetic tunnel junction

One prominent technique for designing spintronic logic gates uses a current-carrying wire to switch a magnetic tunnel junction (MTJ) between its conductive and resistive states [21,28]. An MTJ is composed of two ferromagnetic metals sandwiching a tunneling barrier. When the two ferromagnetic layers are aligned, there is minimal resistanceimpeding electron flow across the barrier; when the two magnetic layers are not aligned, there is a larger resistance. Using a current-carrying wire to create a magnetic field through the MTJ, the ferromagnet alignment can be manipulated, thereby switching the logic state. Multiple clock cycles are required to switch the MTJ state, requiring additional devices of another type that increase the delay and also consume area and power.

2.3. Magnetic quantum cellular automata

First proposed by a group at the University of Notre Dame in 1993, much has been achieved toward the use of quantum cellular automata (QCA) for logical computing. The original QCA logic family is based on the use of electric dipoles to define binary states. A circuit is divided into cells, in which there are two possible states, depending on the location of the electrons. Due to electrostatic repulsion between electrons, the state of one cell affects the state of neighboring cells. By setting the input to a QCA circuit, the remainder of the circuit is forced into the lowest energy state to minimize electron repulsion, thus producing the logical output. One of the primary strengths of this logic family is that signals can be propagated over long distances with only local transit of individual electrons. A functional majority gate was constructed in 1997, but operation has been demonstrated only at a temperature of 70 mK [2].

A modified QCA system has been proposed in which the spin of the electron is utilized. In this version of QCA, the spin of the electrons is used to create the repelling force rather than the electron charge. A simple magnetic QCA (MQCA) device was first published in 2000 [8], and an MQCA majority gate was demonstrated in 2006 [17]. Various researchers have also contributed to MQCA circuits [3,22,30]. Further development is challenged by signal integrity and other performance issues.

2.4. Magnetic domain-wall logic

Magnetic domain-wall logic makes unconventional use of the magnetic properties of nanowires. As nanowires can contain multiple regions of differing magnetic alignment called “domains”, the inventors of magnetic domain-wall logic perform logical computing by controlling the motion of domain boundaries [1]. A rotating magnetic field is applied to the spintronic circuit, and the flow of domain walls is affected by the shape of the nanowire junctions as well as the local domain orientations. This logic family performs computation without the motion of any particles, but through localized spin-flipping. This logic family faces several challenges, however, most notably the long period of time required to switch domain orientations through the cycling of the external magnetic field.

2.5. Spin accumulation

The logic family developed by Dery et al. utilizes spin accumulation to perform logical computation [10]. “Magnetologic gates” (MLGs) are the basis elements of this family, and consist of several
magnetic contacts aligned collinearly on the surface of a semiconductor. Due to spin-dependent conduction between the contacts, local electrical potentials develop within the semiconductor due to the accumulation of spin within the contacts. These voltage drops are dependent on the orientation of the contacts. Capacitive wires are connected across the output contacts; current flows through these wires due to the voltage differences. There is a large ratio of '1' to '0' current, allowing for clear signal differentiation. The general logical function of the MLG is

\[ M = (A \oplus X) \lor (B \oplus Y). \]  

The use of five-contact MLGs, as suggested by the authors, allows for the evaluation of several two-input logic functions with a single gate. The output and input are of different form, requiring a transistor with gain between each logic gate.

2.6. Spin wave phase

In this logic family, signals are defined by the phase of a spin wave [18]. The basis logic element is a magnetoelectric cell that uses an electric field to control a spin wave. The authors suggest the use of piezoelectric and piezomagnetic materials for this purpose, as the mechanical stress induced by an electric field shifts the alignment of a piezomagnetic material. The magnetic alignment of the piezomagnetic material, in turn, affects the phase of the spin wave. The logic family also includes spin wave modulators to invert or buffer a signal, waveguides to transmit the spin wave across the circuit, and converter elements to switch between voltage and spin wave representations of a signal. The authors state that this logic family allows for the creation of logic circuits with significantly less area and power dissipation than CMOS.

2.7. All-spin logic (spin-torque transfer)

Spin-torque transfer is the process by which an electric current flowing through a magnetic material affects the spin-polarization of the material. This phenomenon has been recently suggested for a new binary logic family named “All-Spin Logic” [4,6]. The basis logic element of this family outputs the sum of input spin states. This majority logic gate is sufficient for computing a complete set of logic functions. This gate requires multiple cycles to perform logic functions and external circuitry to manage the process. Additionally, the logic family assumes spin-coherence through the interconnect, which poses a significant challenge.

2.8. Summary

A variety of logic families have been proposed that make use of the spin degree of freedom. The capability of driving the input of one spin-based logic gate with the output of a second spin-based logic gate has been difficult to achieve without requiring additional control logic. This ability to cascade gates is a fundamental requirement of logic circuits, and is a primary challenge for spin-based logic. The logic family described in this work, emitter-coupled spin-transistor logic, has been developed with this principle as a primary consideration.

3. Bipolar magnetic junction transistor

A bipolar magnetic junction transistor is produced by doping the active layer with a transition metal to create a magnetic semiconductor junction that shows a large magnetoresistance. The collector–base junction functions conventionally, while the base–emitter junction behaves similarly to a magnetoresistive p–n junction [26]. Therefore, the gain of the magnetic transistor decreases with increasing magnetic field.
While this characteristic is an issue in terms of power dissipation, flow in ECL circuits during the static propagation of logical signals.

functions come with no tradeoffs; the only required change is a
functions reduce the number of transistors required in a circuit, thereby lowering the area, power, and signal delay. These new functions come with no tradeoffs; the only required change is a new set of rules for routing the wires.

A fundamental difference from CMOS is that large currents flow in ECL circuits during the static propagation of logical signals. While this characteristic is an issue in terms of power dissipation,

3.3. Control wires

The spin-transistor can be selectively controlled by adjacent wires, thus adding additional logical inputs. As we suggest in Fig. 2, two control wires can be placed near the spin-transistor, creating a magnetic field in the plane perpendicular to the current. A high-permeability material surrounds the wires, shielding the rest of the circuit from the magnetic field while simultaneously concentrating the field within the high-permeability material. The gap in the shield results in the concentrated field penetrating the spin-transistor, inducing sufficient magnetization within the emitter to make the base–emitter junction highly resistive.

In a mechanism similar to that exploited by spin-diode logic [15,16], the flow of current through the control wire results in the spin-transistor switching from the forward-active to the cut-off region. When there is no (or minimal) current through the control wires, or if there are equal and opposite currents, the spin-transistor behaves as a standard transistor, and its region of operation is dependent on its bias conditions. If exactly one wire carries current, or if the two wires carry current in the same direction, the spin-transistor will be cut off.

4. Emitter-coupled spin-transistor logic

The capabilities provided by this new magnetic junction transistor merit a reconsideration of BJT-based computing. Many logic families have been invented that utilize BJTs [20]. Each logic family has a unique set of advantages and tradeoffs, and the choice of logic family is therefore dependent on application-specific requirements. In particular, ECL consumes a relatively large amount of power, but its small delay time makes it useful for very high-speed applications [19]. Transistor–transistor logic (TTL), in contrast, is slower and uses less power than ECL, and is therefore more useful for general-purpose computing. However, TTL has been made largely obsolete by the superior characteristics of CMOS circuits while ECL is preferred over CMOS for very high-speed applications such as transmission lines [20].

The recently developed spin-transistors provide new opportunities for BJT logic families, particularly ECL. By replacing traditional BJTs with spin-transistors, a new logic family is created that can perform additional functions without adding any transistors, thus increasing the efficiency of the computing system. These new functions reduce the number of transistors required in a circuit, thereby lowering the area, power, and signal delay. These new functions come with no tradeoffs; the only required change is a new set of rules for routing the wires.

The transistor properties were measured in the common emitter mode where the p-InMnAs layer served as the emitter. The emitter–collector voltage was varied between 0 and 0.4 V and the base current was increased in steps of 1–5 µA. The transistor characteristics were measured in magnetic fields of 0–8 T perpendicular to the plane of the junction. In the presence of a magnetic field, the base–emitter junction becomes resistive, preventing current from flowing across the junction [24]. Thus, in the presence of a magnetic field, a forward-biased base–emitter junction in the bipolar magnetic junction transistor behaves similarly to a reverse-biased base–emitter junction in a conventional BJT. In both cases, the transistor does not produce large currents, and remains cut off rather than in the forward-active region. A more thorough discussion of the effect of a magnetic field on a spin-transistor can be found elsewhere [12]. The spin-transistor has the additional outstanding feature of a large magnetoresistance at room temperature.

The capabilities provided by this new magnetic junction transistor merit a reconsideration of BJT-based computing. Many logic families have been invented that utilize BJTs [20]. Each logic family has a unique set of advantages and tradeoffs, and the choice of logic family is therefore dependent on application-specific requirements. In particular, ECL consumes a relatively large amount of power, but its small delay time makes it useful for very high-speed applications [19]. Transistor–transistor logic (TTL), in contrast, is slower and uses less power than ECL, and is therefore more useful for general-purpose computing. However, TTL has been made largely obsolete by the superior characteristics of CMOS circuits while ECL is preferred over CMOS for very high-speed applications such as transmission lines [20].

The fundamental building block of ECL, as well as the proposed ECL-based logic family, is the differential amplifier illustrated in Fig. 3. In this circuit, one transistor always operates in the active region and the other transistor operates in the cut-off region. The relative base voltage of the two transistors determines their state. With npn transistors (chosen to be consistent with those fabricated in [27]), the transistor with a lower base voltage is in the active region, and the transistor with the higher base voltage is in the cut-off region. If Q1 is cut off and Q2 is in the active region, greater current passes through Q2 and R2 than Q1 and R1. There is therefore a greater voltage drop across R2 than R1, resulting in a high output voltage at V2 and a low output voltage at V1.

This differential amplifier is used with multiple inputs to form the ECL circuits. The logical gate that can be implemented with the fewest npn transistors is an AND/NAND gate, which therefore serves as the basic ECL function. This gate, shown in Fig. 4, accepts two (or more) inputs, and produces two outputs, the logical AND and – AND of the inputs. The gate functions as follows: the base of the reference transistor QR is held at a constant voltage \( V_{REF} \) which ensures that QR will switch between the active and cut-off regions depending on the behavior of the rest of the circuit. If either or both of the inputs are ‘0’, the corresponding input transistor Q1 or Q2 is in the active region, and QR is cut off. There is therefore a large current through \( R_{IN} \) and a small current through \( R_{REF} \), causing, respectively, large and small voltage drops across those resistors. Therefore, the – AND output is ‘1’ and the AND output is ‘0’. If both inputs are ‘1’, QR is in the active region and both Q1 and Q2 are cut off, resulting in an AND output of ‘1’ and – AND output of ‘0’.

We route the current through \( R_{IN} \) or \( R_{REF} \) near a spin-transistor, as discussed above, to create an additional control signal for the spin-transistor. The general basis circuit using this scheme is

**Fig. 3.** Differential amplifier with npn transistors.
shown in Fig. 5, with two control wires for each spin-transistor, with directions arbitrarily chosen. There are thus two voltage inputs and six current inputs for a total of eight inputs. The presence of a net current through the control wires forces the spin-transistor into the cut-off region. Each spin-transistor can therefore perform three-input logic computation. This structure permits the computation of more complex logic within a single stage without requiring additional transistors. As each stage requires the same amount of current, the use of fewer stages implies less supply current flow. Since fewer transistors are required to perform a logic function, there is increased circuit efficiency in terms of power dissipation, propagation delay, and physical area.

4.2. XOR/XNOR gate

This new logic family can be used to design highly compact circuits. XOR/XNOR circuits, for example, can be reduced to a single stage. A specific implementation of the general circuit depicted in Fig. 5 is shown in Fig. 6 that performs the XOR and XNOR functions. In this circuit, input currents A and B create magnetic fields in opposite directions through Q1. As the base is constantly grounded, Q1 is in the active region whenever A and B both carry ‘0′ currents or both carry ‘1′ currents. When Q1 is in the active region, a large current flows through $R_{IN}$, leading to a high XNOR output voltage. Minimal current flows through $R_{REF}$, leading to a small XOR output voltage. When exactly one of the two inputs are a ‘1′, Q1 is cut off, resulting in an XOR output of ‘1′ and XNOR output of ‘0′. Due to the differential nature of this logic family, this circuit computes both XOR and its complement XNOR.

4.3. Multiplexer

Full-swing multiplexer circuits can also be reduced to a single stage, shown in Fig. 7 to perform the (a) 2:1 and (b) 4:1 multiplexing functions. In the 2:1 multiplexer, when the Sel wire carries current, Q1 is always in the cut-off region. When Sel does not carry current, the Sel wire carries current, causing Q2 to be cut-off. Sel chooses which spin-transistor responds to its input. The correct signal is propagated to the output in both inverted and non-inverted forms.

A 4:1 multiplexer can be structured in a similar way. An additional spin-transistor is required for each additional input, and two control wires are used for each spin-transistor. The control wires implement a NOR function to select the spin-transistor in operation; if either of a spin-transistor’s control wires carries current, that spin-transistor is cut off. Therefore, exactly one spin-transistor is in operation at all times, and the selected input is propagated to the output along with its complement.

These multiplexer circuits are far more compact than conventional ECL multiplexer circuits, which require multiple stages of logic and at least 20 transistors. These circuits are also more compact than standard CMOS circuits, which require twelve transistors and two stages, and are comparable to CMOS transmission gate multiplexers, which represent one of the greatest strengths of CMOS [19].

4.4. Full adder

The full adder achieved with this logic family is also highly efficient, as demonstrated in Fig. 8. This circuit contains two distinct
sections, one each for the Sum and COUT logic. The functions have been specifically optimized for emitter-coupled spin-transistor logic using De Morgan’s Laws:

\[ C_{\text{OUT}} = (A \land B) \lor (A \land C_{\text{IN}}) \lor (B \land C_{\text{IN}}) \]

\[ \text{Sum} = A \oplus B \oplus C_{\text{IN}} = \overline{A} \land \overline{B} \land C_{\text{IN}} \lor (A \land \overline{B} \oplus C_{\text{IN}}). \]

In the center of the circuit, a voltage divider sets a reference voltage \( V_R \) for the two reference spin-transistors, QR_S and QR_C. For the Sum logic, the control wires carry current in opposite directions, and therefore implement the XOR function. Q1 is in the active region when both A and B \( \oplus C_{\text{IN}} \) are ‘0’, and is otherwise cut off. Q2 is in the active region when A is ‘1’ and B \( \oplus C_{\text{IN}} \) is ‘0’. If either or both Q1 or Q2 are in the active region, significant current flows through \( R_{\text{IN}} \). This current causes \( C_{\text{OUT}} \) to reach a high voltage, and \( \text{Sum} \) a low voltage. The logic for COUT and \( C_{\text{OUT}} \) functions similarly.

This full adder is unique in its use of only a single stage of logic to produce all of the outputs. As each stage of logic adds to a signal’s propagation time, the use of a single stage provides exceptional speed characteristics. It is also compact, using only 7 spin-transistors. This circuit compares favorably to a standard ECL full adder, which requires 24 transistors, and the CMOS version which requires 28 transistors. In addition, both of these conventional circuits require multiple stages of logic, limiting circuit speed. Emitter-coupled spin-transistor logic therefore provides circuits with higher performance while also decreasing power and area consumption.

In addition to being compact, this logic family can be cascaded for application to large computing systems and scaled to very small dimensions without adverse effects. Scaling leads to substantial speed-up and decreased power dissipation, presenting the opportunity for large-scale adaptation of emitter-coupled spin-transistor logic.

5. Analysis of logic family

In this section, an analysis of the logic family summarized in the previous section is presented. The potential for replacing CMOS is discussed.

5.1. Model of a spin-transistor

Experimental data from the device presented in [27] exhibits a positive magnetoresistance in an InMnAs spin-transistor. Small changes in the base current result in clear changes in the collector current and correspond to a positive amplification. The amplification \( \beta_{\text{dc}} \) of the transistor is defined as:

\[ \beta_{\text{dc}} = (I_C(l_B) - I_C(0)) / I_B \]

where \( I_C(l_B) \) is the collector current for a constant base current of \( l_B \) and \( I_C(0) \) is the collector current for zero base current.

In the presence of an external magnetic field, a change in the amplification is observed. This magneto-amplification \( MA \) is calculated as:

\[ MA = (\beta_{\text{dc}}(B) - \beta_{\text{dc}}(0)) / \beta_{\text{dc}}(0) \times 100 \]

where \( \beta_{\text{dc}}(B) \) is the amplification at a magnetic field of B and a voltage \( V_{VCE} \), and \( \beta_{\text{dc}}(0) \) is the zero magnetic field amplification at the same bias. The magneto-amplification is calculated for a
constant emitter–collector bias for a given base current. In the room-temperature data provided in Fig. 9, amplification decreases with increasing magnetic field.

This transistor, an initial exploration into magnetoresistive spin-transistors that was designed as a proof-of-concept, will be improved significantly in future work. In particular, by optimizing the fabrication technique, it is possible to achieve much higher amplification in these spin-transistors, approaching those achieved with InAs by Wicks [5]. Additionally, by increasing the Mn concentration, it is possible to increase the giant magnetoresistance (GMR) of the junction, resulting in a greater change in amplification with magnetic field (magneto-amplification). It should be noted that the GMR increases with decreasing temperature, providing an even greater magnetoresistive effect at low temperatures. Despite its issues, this exploratory spin-transistor demonstrates its suitability for advanced logic functionality.

The modified Ebers–Moll model is used to relate the magnetoresistance of the collector–base junction to the magneto-amplification of the transistor [11]. The observed magneto-amplification is related to the magnetoresistance of the base-emitter (n-InAs/p-InMnAs) junction. The magnetoresistance in turn depends on spin-dependent transport through the base-emitter junction. When a magnetic field is applied, spin-selective transport in the reverse biased collector–base junction leads to an increase in $R(B)$ (Fig. 10) that in turn leads to a decrease in the collector current both for a zero base current and finite base current. The decrease in the collector current for a finite base current is higher than the decrease in the collector current at zero base current leading to the observed negative magneto-amplification. For a given emitter–collector bias $V_{EC}$ and given base current $I_B$, a change in the resistance in InMnAs/InAs junction results in changes in both the forward and reverse diode currents as these diodes are coupled.

5.2. Magnetic field strength

The magnetic field produced by a control wire through the shield is determined using Ampère’s Law for the structure shown in Fig. 2.

$$B = \frac{\mu_r \mu_0 I_{total}}{\pi D},$$

(6)

where $D$ is the diameter of the magnetic shield, $I_{total}$ is the magnitude of the net current in the control wires, $\mu_0$ is the permeability of free space, and $\mu_r$ is the relative permeability of the mu-metal shield. The boundary conditions of Maxwell’s Equations state that the strength of a magnetic field is constant across a boundary perpendicular to the direction of the field. This implies a field of equal strength through the spin-transistor, though stray field lines and other parasitic effects will cause attenuation. Given conservative estimates for these parameters, the magnetic field is more than sufficient to induce magnetoresistive behavior in the spin-transistor.

5.3. Circuit simulation

Simulations based on the experimental data in Fig. 9 and the aforementioned spin-transistor model and magnetic field calculation have been performed using Synopsis HSPICE. The output voltages from the differential amplifier are listed in Figs. 11–13, for the XOR/XNOR, 2:1 multiplexer, and full adder circuits. Unlike CMOS, these voltages are amplified with an ECL emitter-follower stage to complete a functional circuit. Conventional emitter-followers consist of a transistor and resistor that ensure that the output voltage levels match the input voltage levels. The voltage difference between the ‘1’ and ‘0’ outputs is about 0.7 V in most implementations of ECL.

The simulations show correct outputs that are always clearly identifiable as a ‘1’ or ‘0’, though different combinations of inputs produce slightly different output voltages. These slight variations are due to the difference in the mechanisms caused by the magnetic and electronic inputs. Additionally, it can be seen that the presence of multiple active input transistors results in a stronger signal than is caused by a single active input.

5.4. Scaling

The functionality of the devices is not expected to change significantly when dimensions are reduced. This is because the
magnetoresistance of the InMnAs layer is independent of the device size since it is an inherent property of the magnetic material. Experiments have shown that for p–n junctions of decreased size and equal Mn content, the magnetoresistance of the InMnAs layer remains nearly constant [27].

As the magnetic field created by the control wires is inversely proportional to the shield diameter, this technology is suitable for scaling. A constant $I_{\text{total}}/D_{\text{ratioproducesaconstant}}$ magnetic field, making it possible to decrease the current, and therefore the power, with scaling. This behavior is in contrast to conventional circuit technologies based purely on electron charge, which are difficult to scale to ever smaller dimensions.

### 5.5. Device improvements

The primary challenge facing emitter-coupled spin-transistor logic is the need for large magnetic fields. For practical applications, a magnetic field on the order of 1 T or less is required. Achieving this goal will depend upon a fundamental understanding the factors that determine spin transport in these heterojunctions.

A required magnetic field depends on the rate of change of the conductance of the diode. The conductance of the diode is related to device properties like the magnetocurrent ratio and to material properties like the $g$-factor. Controlling the device material properties can lead to devices that switch on and off at lower magnetic fields. The effective $g$-factor determines the magnetoresistance properties of the semiconductor heterojunction. For a p-type DMS the effective $g$-factor $g_{\text{eff}}$ is given by two terms and can be written as [7]:

$$g_{\text{eff}} = g^* + x_{\text{eff}}N_0\beta S \mu_B H B_5 \left( \frac{g_{\text{Mn}}\beta S H}{k_B (T + T_{\text{AF}})} \right)$$

where $x_{\text{eff}}$ is a function of the Mn$^{2+}$ ion concentration, $N_0$ is the number of cations per unit volume, and $B_5$ is the Brillouin function. For Mn, $S = 5/2$ and $g_{\text{Mn}} = 2$. The functions $x_{\text{eff}}(x) < x$ and $T_{\text{AF}}(x) > 0$ describe the reduction of magnetization due to antiferromagnetic interactions between Mn$^{2+}$ spins $\mu_B$. The above equations indicate that the effective $g$-factor is an explicit function of Mn concentration and temperature. Thus, we should be able to modify the junction magnetoresistance and increase the value of $g_{\text{eff}}$ by increasing either the concentration of Mn ions in the magnetic semiconductor or decreasing the temperature [23].

Shown in Fig. 14 is the conduction as a function of applied magnetic field for different values of $g$ [25]. This calculation is based on the two channel conduction model discussed in Ref. [26]. We see that increasing the effective Landé factor $g_{\text{eff}}$ changes the conductance data significantly. For a $g$ value of 500, the magnetic field required for the conductance of the diode to reach 50% of its zero field value is much smaller, on the order of $\sim 0.5$ T. A similar decrease in the magnetic field required can be achieved by lowering the temperature of operation as shown in Fig. 15.

### 5.6. Computing implications

As demonstrated in Section 3, logic circuits designed with this emitter-coupled spin-transistor logic family can execute logical functions using 20%–30% of the number of devices required for conventional ECL while drawing the same amount of current per device. In this new logic family as well as conventional ECL, the delay and power dissipation of a computing circuit are proportional to the number of logic stages. Therefore, a speedup of $3 \times$ to $5 \times$ is achievable, along with a decrease in power consumption of 70%–80%, resulting in a decrease in power-delay product by a factor of 10–25 depending on the logic circuit. This greater than an order-of-magnitude power efficiency improvement increases the performance of high speed computing while also enhancing the range of applications for which ECL-based logic is effective.

### 6. Conclusion

In contrast to other proposed spintronic logic families, emitter-coupled spin-transistor logic potentially provides the critical property of logic elements that can drive cascaded stages without amplification or modulation. The differential amplifier permits clearly defined binary states despite a relatively small on–off ratio, enabling robust and fault-tolerant integrated spintronic circuits. This ability to cascade logic stages is necessary for logic circuits capable of replacing Si CMOS in the post-Dennard scaling era [13]. By modifying ECL to leverage the unique behavior of

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>$C_{\text{IN}}$</th>
<th>$C_{\text{OFF}}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.02</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.62</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0.62</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0.64</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0.62</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0.62</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.62</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0.62</td>
</tr>
</tbody>
</table>
magnetic junction transistors, this logic family may achieve a 10−25× improvement in power-delay product. Emitter-coupled spin-transistor logic provides significant improvements in speed, power, and area, promising to be a very high-performance logic family for the next generation of computing.

References


J. Archibald Peters is a Research Associate in Materials Science & Engineering Department of Northwestern University. He received the B.Sc. degree in Mathematics & Physics from the University of Ghana in 1997 and the Ph.D. degree in Physics from the Ohio University, Athens, in 2006. Dr. Peters has more than 10 years of experience in developing semiconductor materials and devices for optoelectronic and spintronic applications. His research interests include the application of nanoscale and quantum mechanical phenomena to the design of large-scale computing systems, with particular emphasis on beyond-CMOS logic families.

Gokhan Memik is an Associate Professor at the Electrical Engineering and Computer Science Department of Northwestern University. He received the B.S. degree in computer engineering in 1998 from Bogazici University and the Ph.D. in electrical engineering from the University of California at Los Angeles (UCLA) in 2003. He is the author of 2 book chapters and over 100 refereed journal/conference publications. Papers co-authored by him have been nominated for a best paper award at DAC (2005) and MICRO (2008) and won the Best Student Paper Award at Supercomputing (2007). He has served on over 30 program committees, was the co-chair for the Advanced Networking and Communications Hardware Workshop (ANCHOR) and the program co-chair of 2007 International Symposium on Microarchitecture (MICRO-40). He is also an associate editor of the International Journal on Reconfigurable Computing. Gokhan Memik is the recipient of the Wiessner-Slivia Junior Chair (2006–2009), National Science Foundation CAREER Award (2008–2013), and Department of Energy Early CAREER PI Award (2005–2008).

Bruce W. Wessels received the B.S. degree from the University of Pennsylvania, Philadelphia, in 1968 and the Ph.D. degree in materials science from the Massachusetts Institute of Technology, Cambridge, in 1972. From 1972 to 1977, he was a Member of Technical Staff of the General Electric Research and Development Center. In 1977, he joined the faculty of the McCormick School of Engineering, Northwestern University, Evanston, IL, where he is currently a W.P. Murphy Professor of Materials Science and Engineering, and Electrical Engineering and Computer Science. His research interests include the electronic, magnetic and optical properties of semiconductor and dielectric materials and devices.

Prof. Wessels is a senior member of OSA and a fellow of APS and ASMI.

Joseph S. Friedman received the A.B. degree in engineering sciences from Dartmouth College, Hanover, NH, and the B.E. degree from the Thayer School of Engineering at Dartmouth College, both in 2009. He received the M.S. degree in electrical and computer engineering from Northeastern University, Evanston, IL, in 2010, and is currently working toward the Ph.D. degree in electrical and computer engineering.

He has interned at Intel Corporation, where he worked on logic design automation at both the 130 and 90 nanometer processes. His research interests include the application of nanoscale and quantum mechanical phenomena to the design of large-scale computing systems, with particular emphasis on beyond-CMOS logic families.