Threshold Logic With Electrostatically Formed Nanowires

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Abstract—The modulation of current through an electrostatically formed nanowire (EFN) is controlled by the voltage on the four input gates. The behavior of this multi-gate transistor can be interpreted as a complex four-input switching process, enabling the computation of multiple-input threshold logic functions using a single device. We have therefore created a novel threshold logic family leveraging these unique capabilities that enables the efficient computation of complex logic functions. Experimental and simulation data are provided to demonstrate feasibility and evaluate behavior. This logic family overcomes the challenge posed by the input–output voltage mismatch inherent to EFNs and produces circuits with one-eighth the number of active logic devices and one-quarter the number of transistors required by CMOS.

Index Terms—Beyond-CMOS computing, FETs, nanowire, threshold logic.

I. INTRODUCTION

The availability of additional inputs to control a transistor permits advanced logical functionality, prompting significant research toward the realization of transistors with multiple gates. In an electrostatically formed nanowire (EFN) [1], a four-gate transistor similar to the G4-FET [2], [3], a current is controlled by four independent gate voltages. As shown in Fig. 1, an EFN is composed of a doped semiconductor region surrounded by two lateral junction gates (JGs) and two metal-oxide-semiconductor (MOS) gates. A nanowire surrounded by depletion regions is electrostatically formed between the source and the drain, allowing majority carriers to flow through a region determined by the voltages on the four gates. The nanowire channel width is decreased through reverse biasing of the JGs, while the MOS gates modulate the current through vertical positioning of the nanowire [4].

Though the independent gate control in EFN devices offers exceptional capabilities, the inability to cascade EFN gates prevents its use in logic circuits. In particular, the JG voltages must be below both the source and drain voltages to modulate the current without forward biasing. Therefore, the output voltage of each EFN logic gate cannot be used as an input voltage for the JG of another EFN logic gate. The development of EFN logic is thus prevented by the same challenge that impeded junction field-effect transistor (JFET) logic [5]. Though several $G^4$-FET logic circuit structures have been presented [6]–[8], none have permitted cascaded logic gates, an essential feature necessary for useful logic circuits.

This brief proposes EFN threshold logic, the first EFN or $G^4$-FET logic structure in which gates can be cascaded. Level shifters between each gate overcome the JG voltage mismatch challenge, enabling the computation of any logic function. For maximal efficiency, a novel threshold logic paradigm leverages the inherent threshold nature of the multi-input EFN gate. Experimental measurements and simulated characteristics are provided that demonstrate threshold logic functionality, and the compact nature of the proposed EFN threshold logic is shown through the analysis of a full adder circuit.

II. EFN THRESHOLD DEVICE

Threshold logic is an unconventional binary logic style in which each gate outputs a binary value $F$ determined by the comparison between a threshold $T$ and the weighted sum of the inputs. That is,

$$F(X_1, X_2, \ldots, X_N) = \begin{cases} 1, & \text{if} \sum_{i=1}^{N} W_i X_i \geq T \\ 0, & \text{otherwise} \end{cases}$$

for $N$ inputs $X_1, X_2, \ldots, X_N$ with weights $W_1, W_2, \ldots, W_N$. For the simple two-input case with $W_1 = W_2 = 1$, this function can be understood as an AND gate when $T = 2$ and an OR gate when $T = 1$. Threshold functions permit the simplification of logic functions, but the lack of suitable

Fig. 1. EFN device with two lateral JGs and two MOS gates. An EFN channel is controlled through independent control of the four gates.
electronic devices has impeded integration into practical circuits. In particular, the ability of a threshold gate to perform complex logic functions is limited by its noise margin [9]. With conventional single-input devices, the threshold is compared to a sum of voltages or currents, restricting the input combination to the resolution of the device. Though sense-amplifier-based differential structures have been suggested for threshold logic with novel nanodevices [9], the availability of only one input is a fundamental limitation.

As a multi-input device with inherently threshold behavior, the EFN is suitable for threshold logic applications. The complete device was simulated with a 3-D device simulator (Synopsis Sentaurus) considering the experimental process parameters, where for each mesh point, the Poisson and continuity equations were numerically solved. The EFN device has a length of 0.7 \( \mu \text{m} \), a width of 0.54 \( \mu \text{m} \), front gate (FG) and back gate (BG) oxide thicknesses of 6 nm, an \( n \) doping of \( 3 \times 10^{17} \text{ cm}^{-3} \), and a \( p \) doping of \( 2 \times 10^{19} \text{ cm}^{-3} \). Table I shows the simulated source–drain resistance for a source–drain voltage of 3 V for all combinations of 0 V and \(-3\) V gate voltage inputs. As seen in the table, the resistance is greater than \( 10^{12} \Omega \) whenever \(-3\) V is applied to (a) the FG and at least one other gate or (b) all three gates. The source–drain resistance is less than \( 10^9 \Omega \) otherwise, where the weighted sum of the binary inputs is less than the threshold of 3.

### III. EFN Threshold Logic Circuits

Connected to a pull-up resistor in the NMOS-type structure of Fig. 2, the output voltage is large whenever the EFN is in a conductive state. This threshold behavior can be observed in the rightmost column of Table I, with binary ‘1’ outputs representing voltages close to 3 V. This threshold logic gate can be described by

\[
V_{\text{OUT}} \approx \begin{cases} 
3 \text{ V}, & \text{if } 2X_{FG} + X_{BG} + X_{JG1} + X_{JG2} \geq 3 \\
0 \text{ V}, & \text{otherwise}.
\end{cases}
\]

The eight ‘1’ states thus have weighted sums greater than or equal to 3, and the eight ‘0’ states have weighted sums less than 3.

As the input voltage range (\(-3\) V to 0 V) differs from the output voltage range (0 V to 3 V), the outputs cannot directly be used as inputs to other gates. As mentioned previously, this challenge has impeded previous attempts to use the EFN (or \( G^4 \)-FET) for logic [6]–[8]. We overcome this difficulty by using level-shifting stages between EFN gates, with binary ‘0’ represented by 0 V and ‘1’ represented by 3 V or \(-3\) V.

The cascaded EFN threshold logic structure is demonstrated in the one-bit full adder circuit of Fig. 3. This circuit consists of five gate stages and is composed of three EFNs, three \( n \)-type MOSFETs, and four resistors. The three inputs (\( A, B \), and \( C_{\text{PN}} \)) are applied to the series EFNs \( E_1 \) and \( E_2 \), which function similarly to the threshold gate described above and output \( C_{\text{OUT}+} \). (+ subscript denotes the range 0 V to 3 V). In order to propagate the signal to another EFN gate, the conventional transistors \( M_1 \) and \( M_2 \) create \( C_{\text{OUT}−} \) and \(-C_{\text{OUT}−} \) to shift the voltage (− subscript denotes the range \(-3\) V to 0 V).

The propagation of the binary signals and their respective voltage values are shown in the full adder truth table of Table II. As the voltage is in the proper range, \(-C_{\text{OUT}−} \) can be an input to \( E_3 \). Similarly, the full adder
Fig. 3. EFN threshold logic full adder with three EFN logic devices and three level-shifting MOSFETs (M1 and M3 are noninverting, M2 is inverting).

TABLE II
ONE-BIT FULL ADDER ELECTRICAL BEHAVIOR

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C IN</th>
<th>C OUT+</th>
<th>C OUT-</th>
<th>Sum+</th>
<th>Sum-</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>-3.00 V</td>
<td>-2.04 V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>-3.00 V</td>
<td>-3.00 V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>2.96 V</td>
<td>2.96 V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>-0.05 V</td>
<td>-0.05 V</td>
</tr>
<tr>
<td>1</td>
<td>-3.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>2.96 V</td>
<td>3.00 V</td>
</tr>
<tr>
<td>1</td>
<td>-3.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>0.00 V</td>
<td>2.96 V</td>
<td>3.00 V</td>
</tr>
<tr>
<td>1</td>
<td>-3.00 V</td>
<td>1.30 V</td>
<td>0.00 V</td>
<td>-3.00 V</td>
<td>3.00 V</td>
<td>3.00 V</td>
</tr>
<tr>
<td>1</td>
<td>-3.00 V</td>
<td>1.30 V</td>
<td>0.00 V</td>
<td>-3.00 V</td>
<td>-0.05 V</td>
<td>-0.05 V</td>
</tr>
</tbody>
</table>

IV. EXPERIMENTAL REALIZATION

In initial experiments, we have demonstrated an EFN threshold device with a 500 nm wide and 5 μm long n-doped (4 × 10^{17} cm^{-3}) channel flanked by two p-type doped (6 × 10^{19} cm^{-3}) junction gates, as shown in Fig. 4 (fabricated by TowerJazz, Migdal Haemek, Israel). The SiO2 front gate dielectric thickness is 6 nm, while the back gate dielectric thickness is 1.5 μm. Though the back gate oxide is too thick to have a sufficiently strong effect on nanowire formation, we use a 50 mV source–drain bias to experimentally demonstrate three-input control of the nanowire in Table III. As four states each have resistances greater than 2.7 × 10^{9} Ω or less than 1.1 × 10^{6} Ω, this device can be interpreted to perform a threshold logic function with \( W_{FG} = W_{JG1} = W_{JG2} = 1 \) and \( T = 2 \) such that

\[
R_{EFN} = \begin{cases} 
> 2.7 \times 10^{9} \, \Omega, & \text{if } X_{FG} + X_{JG1} + X_{JG2} \geq 2 \\
< 1.1 \times 10^{6} \, \Omega, & \text{otherwise.}
\end{cases}
\]

(4)

This is equivalent to a majority gate, one of the simplest threshold functions. We are currently working on decreasing the back gate oxide thickness to achieve the function shown in simulation, and have also proposed an EFN device with additional inputs that could enable advanced threshold logic functionality [8].

Each EFN device performs a four-input logic function, whereas an NMOS transistor and a PMOS transistor are required for each input to a CMOS function. Therefore, though each EFN device requires more overhead than a MOSFET, the computation of a function with EFN threshold logic requires roughly one-eighth the number of EFN devices as transistors required by CMOS. Some circuits are even more compact, such as the majority function, which requires only one EFN device. Though the level shifters add to the power consumption and delay and require additional NMOS transistors, the complete full adder requires a total of only six transistors.

Further improvements may add to the performance, especially the development of a p-type EFN to preclude the need for level shifters and prevent static power dissipation. Further miniaturization would also be beneficial, as would voltage scaling. The resistors can also be replaced by depletion-mode transistors to decrease the area and simplify circuit integration.

V. CONCLUSIONS

EFN threshold logic provides full-swing compact logic, fully leveraging the device properties to solve the signal integrity challenges of threshold logic. We use level-shifting stages for the first logic circuit proposal in which EFN devices can be cascaded. This logic family provides significantly increased logic efficiency compared to CMOS, making EFN threshold logic a viable technology to replace CMOS for general-purpose computing.
REFERENCES


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