# A Spin-Diode Logic Family

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***Abstract*—While most modern computing technologies utilize Si complementary metal-oxide-semiconductor (CMOS) transistors and the accompanying CMOS logic family, alternative devices and logic families exhibit significant performance advantages. Though heretofore impractical, diode logic allows for the execution of logic circuits that are faster, smaller, and dissipate less power than conventional architectures. In this paper, magnetoresistive semiconductor heterojunctions are used to produce the first complete logic family based solely on diodes. We utilize the diode magnetoresistance states to create a binary logic family based on high and low currents in which a full range of logic functions is executed. The diode is used as a switch by manipulating its magnetoresistance with current-carrying wires that generate magnetic fields. Using this device structure, we present basis logic elements and complex circuits consisting of as few as 10% of the devices required in their conventional CMOS counterparts. This diode logic family is therefore an intriguing potential replacement for CMOS technology as Si scaling reaches its inherent limits.**

***Index Terms*—Beyond CMOS computing, diode logic, logic circuits, magnetoresistance, spintronics.**

## I. Introduction

CONTINUED reduction in transistor size has provided the technological basis for marked circuit performance improvements, making possible billion transistor integrated circuits operating at gigahertz frequencies. The smaller size of these devices, however, results in increased fabrication difficulties, higher power densities, and parasitic effects that threaten to limit the further improvement of Si-based circuits [1]. In an effort to provide continued improvements in computing performance, newly available materials and devices have been evaluated as building blocks for next generation computing [2]. These technologies include devices derived from single-electron transistors [3], carbon nanotubes [4] and related graphene structures [5], [6], nanowires [6], [7], and molecular switches [8].

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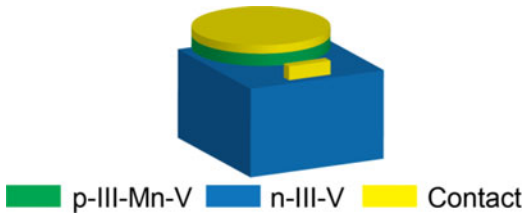


Fig. 1. Magnetoresistive spin-diode.

Additionally, there has been much interest in devices and logic design techniques that utilize electron spin [9]–[20].

The emergence of new materials and devices has inspired reconsideration of conventional logic styles and circuit architectures. While CMOS transistors and logic have dominated Si-based circuits [21], other devices and logic families exhibit significant advantages. Diode logic is elegant in several respects, such as simple OR gates and single junction devices that allow for compact circuit structures. Circuits based on diode logic use fewer devices than their CMOS counterparts, and therefore potentially consume less power and area while operating at higher speeds. Diode logic, however, has historically been impractical due to the inability of a diode to act as an inverter [22]. As inversion is a necessary function of a complete logic family, diodes, prior to these results, could only perform complex logic functions in concert with transistors.

The recent invention of the magnetoresistive spin-diode solves this problem, as these spin-diodes can be used individually as inverters [14], permitting the development of a complete diode logic family. This diode logic family performs logical functions with significantly fewer devices than CMOS, and is therefore a potential replacement for Si CMOS computing. The rest of this paper is organized as follows: the material properties of the spin-diodes are discussed in Section II. In Section III, the logic family is explained. The computing implications of this diode logic family are discussed in Section IV. The paper is concluded in Section V.

## II. Magnetoresistive Spin-Diode

A magnetoresistive spin-diode is produced by doping a semiconductor p-n junction with an element that has a strong interaction with a magnetic field. A common dopant element is Mn. In this semiconductor heterojunction, shown in Fig. 1, Mn is added to form a p-type III-V layer, leading to spin interactions near the junction.

The spin-diode acts as a conventional diode in the presence of zero or low-magnetic fields, with a high ratio of forward current to reverse current. However, when a magnetic field is applied across the junction, there is splitting in the valence and conduction bands in the magnetic semiconductor [23]. As

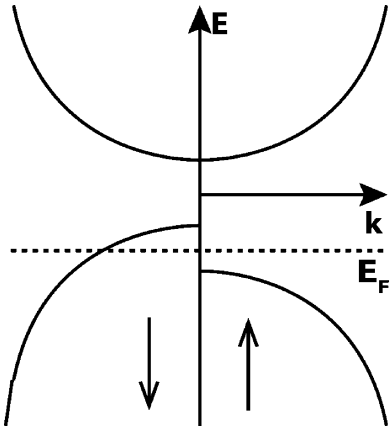


Fig. 2. Splitting of energy bands under magnetic field.

depicted in Fig. 2, the presence of a magnetic field results in decreased energy band level for states with spin aligned with the field, and increased energy band level for spin states opposed to the field. As energy states close to the Fermi energy level, $E_F$, have an increased probability of occupation by free charge carriers, there is a decreased number of holes with spins in the same direction as the field, and an increased number of holes with opposite spin. Furthermore, there is increased scattering for holes aligned opposite to the field. Because the holes are the dominant carriers, these effects cause an increase in resistivity with magnetic field. Thus, under forward bias, it is possible to define two distinct states: a resistive state in the presence of a magnetic field, and a conductive state in its absence.

## III. Spin-Diode Logic Family

While the spin-diode is interesting in its own right, the ability to cascade these devices to implement logical functions presents exciting opportunities. By routing a wire near the diode, a magnetic field can be created that switches the state of the diode. A spin-diode logic family is therefore proposed in which logic functions are executed by using the electric current through spin-diodes to control the magnetic field through other spin-diodes.

This logic family is composed solely of spin-diodes; no transistors are required. It is therefore the first example of a complete diode logic family. As such, it provides the simplicity advantages of a two-terminal device structure while exploiting the efficiencies of diode logic.

### A. Digital States

In this spin-diode logic family, a digital "1" is defined as the "high" current produced by the spin-diode conductive state and a digital "0" is defined as the "low" current produced by the resistive state. Each spin-diode is forward biased, with the positive and negative terminals connected, respectively, to the positive voltage, $V_{DD}$, and ground. The wires that form these connections are routed to control the magnetoresistance of other spin-diodes. A spin-diode propagating a "1" thus creates a magnetic field in another spin-diode, while a spin-diode propagating a "0" does not.

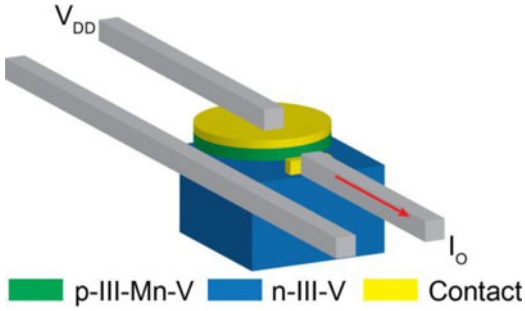


Fig. 3. Magnetoresistive spin-diode with one control wire.

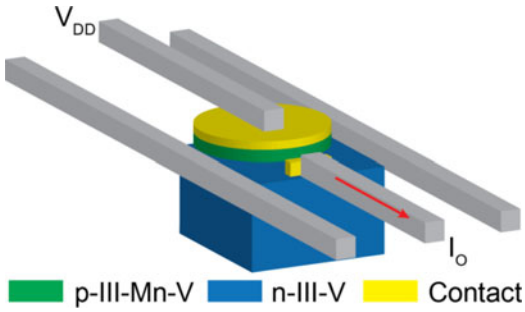


Fig. 4. Magnetoresistive spin-diode with two control wires.

As shown in Fig. 3, a metal wire is placed parallel to the plane of the junction, isolated by an insulator. This wire controls the diode's magnetoresistive state, as the current through the wire creates a magnetic field perpendicular to the plane of the junction. Under zero or small current, the diode is in its conductive state; a large control current asserts the diode's resistive state.

A second control wire can be added to this structure, as shown in Fig. 4. This second wire behaves in a similar fashion as the first wire, and, depending on the relative direction of the currents, these currents interfere either constructively or destructively. If the currents in the two wires travel in opposite directions, the fields will add, doubly suppressing the diode current; if the currents are in the same direction, the fields will cancel, allowing current to flow through the diode. These features form the building blocks of spin-diode logic.

### B. Basis Logic Elements

In Fig. 5, each of this family's basis logic elements is illustrated using at most a single diode: an inverter, NOR gate, XNOR gate, and OR gate. In each of these configurations, the positive terminal of the diode is connected to $V_{DD}$, while the negative terminal is routed through the circuit before eventually being grounded. Therefore, in the absence of current through the various control wires, each of these diodes propagates a "1," and the configuration of the control wires dictates the logical function of each gate.

An inverter, the simplest gate, is shown in Fig. 5(a). The input current $I_A$ is routed alongside the diode, and induces a field proportional to its current. If $I_A$ is a "1," it creates a large magnetic field, thereby reducing the current through the diode, and causing the output current $I_O$ to propagate a "0." If $I_A$ is

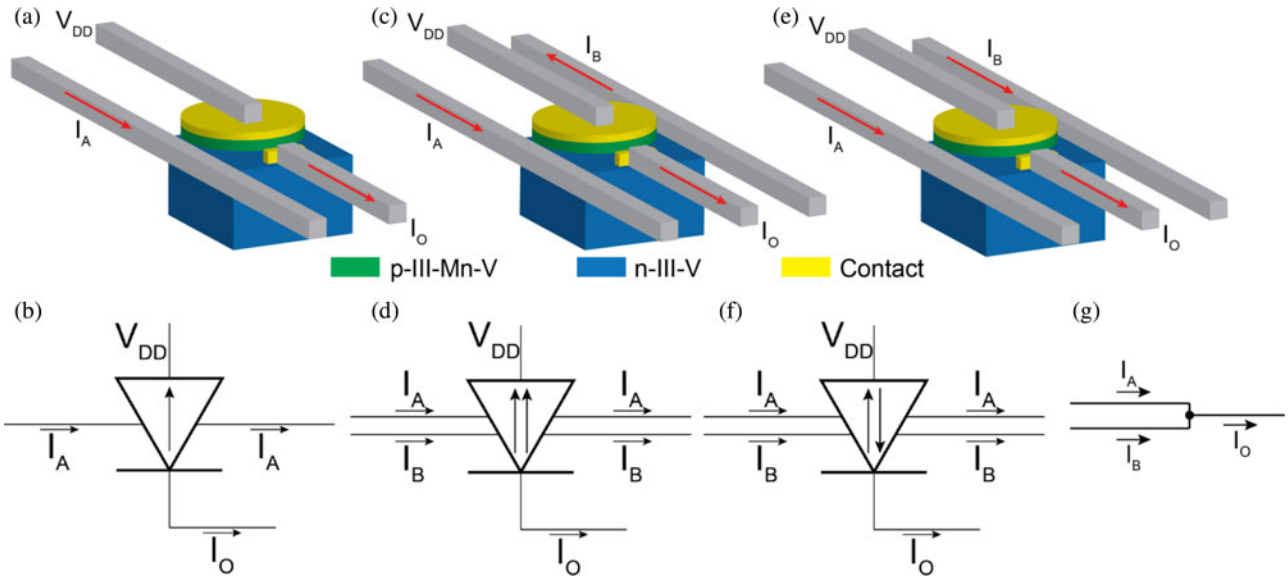


Fig. 5. (a) Inverter consisting of input wire with current $I_A$ routed alongside the diode to control the output current $I_O$. The positive terminal is connected to $V_{DD}$ and the negative terminal is connected to ground at some distant part of the circuit. A high input current results in a magnetic field that suppresses the output current. (b) Symbol for spin-diode inverter. (c) Additional input current $I_B$ results in a NOR gate. A high current on either input suppresses the output current. In the case of high currents on both inputs, the output current is doubly suppressed. (d) Symbol for spin-diode NOR gate. (e) Inverting the direction of $I_B$ produces an XNOR gate. In this configuration, a high current on exactly one of the input wires suppresses the output current. Unlike the NOR gate, high currents on both inputs create canceling magnetic fields, allowing a high current to flow through the output. (f) Symbol for spin-diode XNOR gate. (g) OR gate formed by the summation of currents satisfying the principle of conservation of charge.

a "0," it does not create a sufficient magnetic field through the junction, and a "1" is propagated.

The addition of a second input current $I_B$ results in a NOR gate, shown in Fig. 5(c). In this arrangement, the presence of a current in either of the two inputs results in a magnetic field through the diode oriented in the same direction. Therefore, if at least one of the two inputs is a "1," the output propagates a "0"; otherwise, the output is a "1."

The XNOR is identical to the NOR gate in terms of device structure, but its relative placement within a circuit produces a different function. As the two currents flow in the same direction, each current creates a magnetic field through the diode in the opposite direction. Therefore, if both inputs are "1," there is no net magnetic field through the diode, and a large current flows, propagating a "1." This structure is shown in Fig. 5(e). This single device XNOR gate is significantly more compact than the standard ten device CMOS implementation.

As the magnitude of the currents defines the digital states, an OR gate is constructed simply by merging two wires (therefore, no symbol is needed). As shown in Fig. 5(g), the output current $I_O$ is equal to the sum of the two input currents. By placing an OR gate as an input to another gate, a variety of logic functions with more than two inputs can be implemented.

### C. Example Circuits

The four basis logic elements can be arranged to implement any logical circuit. A common circuit is a one-bit full adder, shown in Fig. 6, which calculates a one-bit sum and carry-out based on the addition of two bits and a carry-in [24]. There are three inputs ($A$, $B$, and $C_{\text{in}}$) and two outputs ($C_{\text{out}}$ and Sum), optimized for this logic style as

$$\begin{aligned} C_{\text{out}} &= (A \wedge B) \vee (A \wedge C_{\text{in}}) \vee (B \wedge C_{\text{in}}) \\ &= \overline{\overline{A \vee B} \vee \overline{A \vee C_{\text{in}}} \vee \overline{B \vee C_{\text{in}}}} \end{aligned} \tag{1}$$

$$\text{Sum} = A \oplus B \oplus C_{\text{in}} = \overline{\overline{A \oplus B} \oplus C_{\text{in}}}. \tag{2}$$

As illustrated in the figure, Sum is generated by cascading two XNOR gates. In XNOR1, $A$ and $B$ are inputs, and in XNOR2, one input is $C_{\text{in}}$, and the other input is from XNOR1. In both gates, if the two inputs are the same, a "1" is propagated. If the two inputs are different, a "0" is produced. Similarly, $C_{\text{out}}$ is achieved with three NOR gates, an OR gate, and an inverter. NOR1, NOR2, and NOR3 each propagate a "0" if either input is a "1"; when these propagated currents are summed in OR1, a "0" is propagated unless at least two of the initial inputs are "0." This value is inverted to output $C_{\text{out}}$. This adder uses only six spin-diodes, which is far more compact than the typical CMOS 28-transistor implementation. Furthermore, the use of a single device type simplifies the fabrication process.

A two-to-one multiplexer is another useful circuit that can be built with this logic family. As shown in Fig. 7, INV1 produces an inverted select signal. The select and inverted select signals are routed, respectively, through NOR gates alongside A and B. Each NOR gate propagates a "0" unless a signal with a "0" has been selected. These signals are combined and inverted such that a "1" is propagated unless a signal with a "0" has been selected.

This logic family also enables constructing an intriguing and simple SR latch, shown in Fig. 8. As seen in the diagram, each latch NOR gate output is routed to the other's input, forcing the

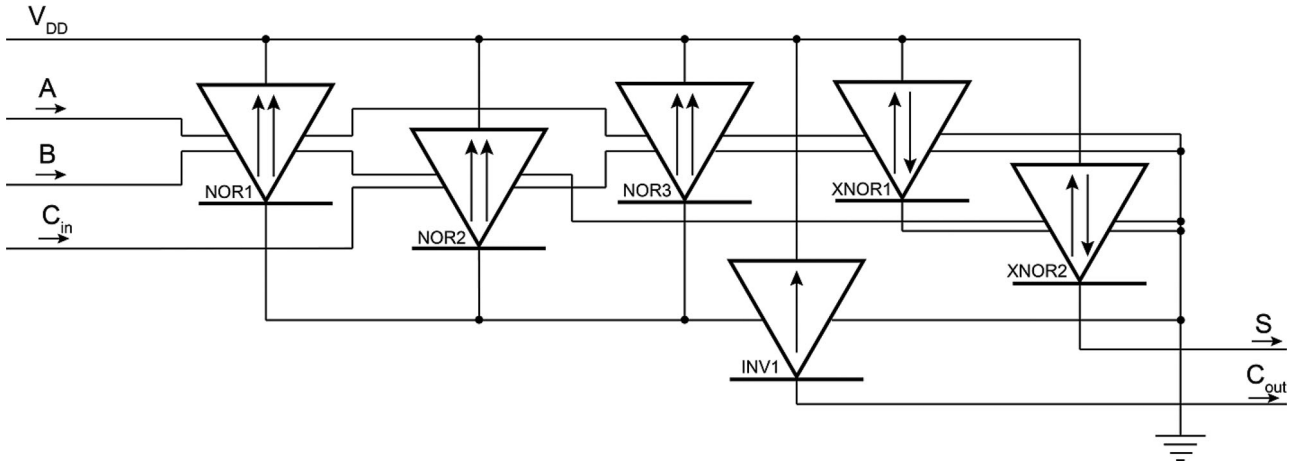


Fig. 6. Spin-diode adder.

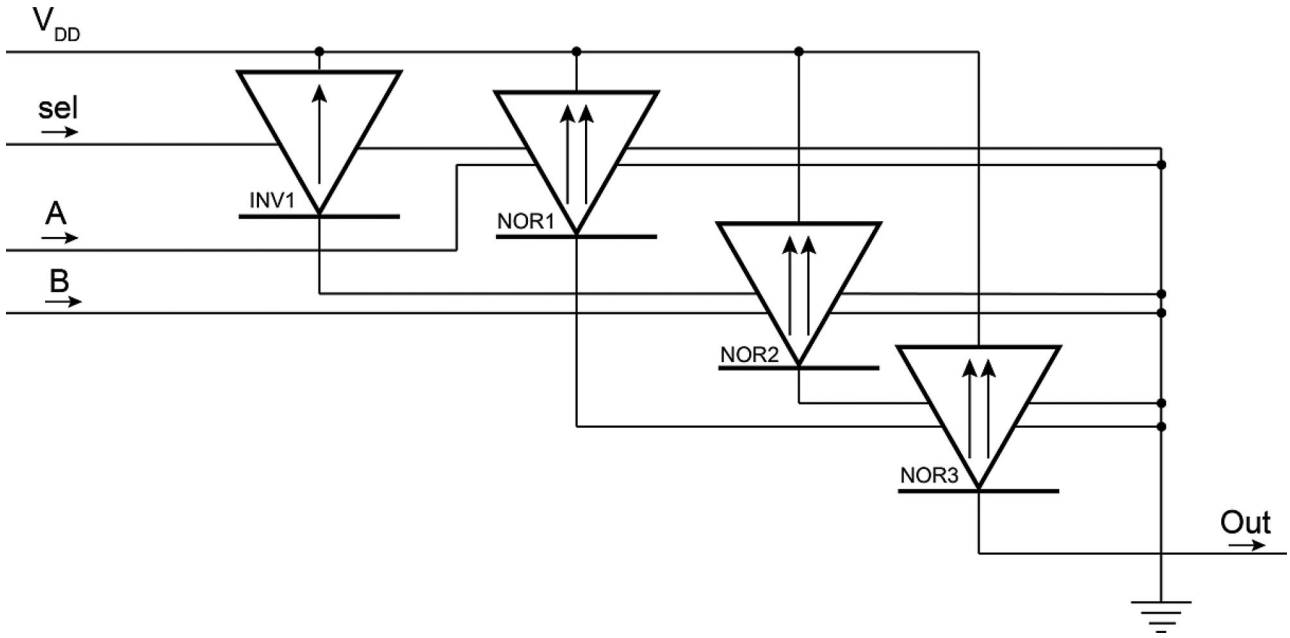


Fig. 7. Spin-diode two-to-one multiplexer.

propagation of opposite values. When one of the diodes propagates a high current, the current is suppressed in the second diode, which allows the first diode to propagate a high current, thereby maintaining a self-consistent state. To set the value stored in the latch, an external current is passed through one of the diodes. To set a "1," a current is passed through NOR1, and to set a "0," a current is sent through NOR2. This circuit is a bistable inverter chain, and can be used to create stable memory storage.

## IV. Computing Implications

Recent developments in magnetic semiconductors suggest that integrated circuits based on this technology will be possible in the near future. In particular, magnetoresistive III-Mn-V heterojunction spin-diodes have been fabricated by depositing III-Mn-V magnetic thin films on III-V semiconductor substrates followed by standard photolithographic processes [14], [17]. The fabricated InMnAs diodes are 300 $\mu$m in diameter and can support current densities greater than $10^7$ A/m$^2$ [17]. The size of these spin-diodes can be significantly reduced with existing microfabrication techniques. The magnetic field response of this diode exhibits the characteristics necessary to create magnetoresistive spin-diode logic, and the diode has the additional outstanding feature of a positive magnetoresistance that persists even at room temperature. As the measurements in Fig. 9 make clear, the current I decreases significantly as the magnetic field is increased. When the voltage is increased, the $I_{\rm on}/I_{\rm off}$ ratio increases, where $I_{\rm on}$ is the zero-field current and $I_{\rm off}$ is the

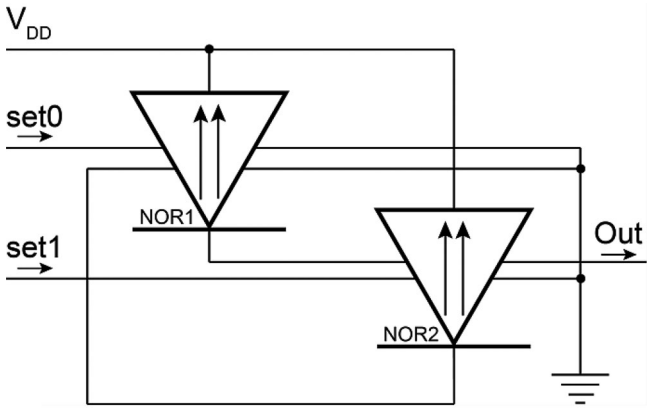


Fig. 8. Spin-diode SR latch.

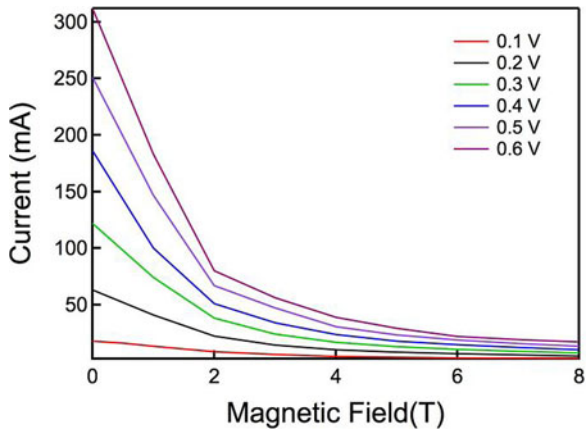


Fig. 9. Spin-diode current as a function of magnetic field at various voltage biases [17].

current at a higher field (e.g., 5 T). A high ratio is useful as it supports differentiation between two digital states. It is expected that increasing the Mn content of the heterojunction will lead to increased sensitivity to magnetic fields (i.e., increased g-factor) thereby reducing the current, field, power, and area requirements [25]. Operation below room temperature will also reduce the system's structural requirements [20].

Scaled spin-diode circuits can be produced with reduced current by adding a high-permeability magnetic shield to the logic gate structure. This structure, illustrated in Fig. 10, concentrates the magnetic field through a loop of a material with a relative permeability greater than 2000 [26]. With control current $I$, permeability of free space $\mu_o$, shield relative permeability $\mu_r$, and a distance $R$ from the shield to the control wires, the magnetic field $B$ is

$$B = \frac{\mu_r \mu_0 I}{2\pi R}. \tag{3}$$

Given control current wires 50 nm from the shield, a 100 $\mu$A control current will produce a 0.8 T field through the shield. According to Maxwell's equations, the magnetic fields normal to a boundary are equal on each side of the boundary. Further improvement of the spin-diode properties should reduce the

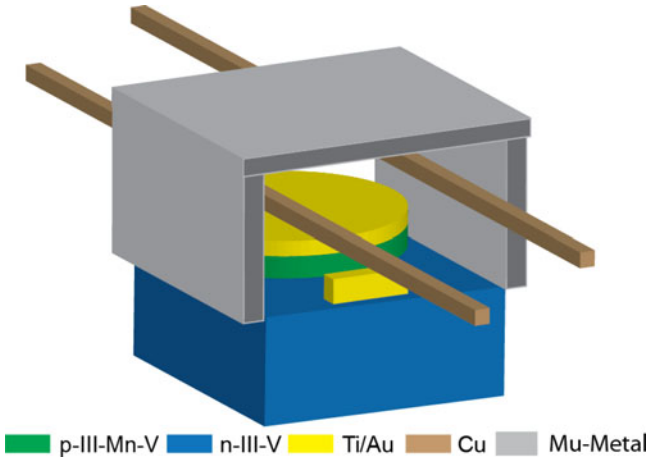


Fig. 10. Spin-diode, control wires, and high-permeability shielding metal.

required magnetic field to less than 1 T, making this structure effective for scaled logic circuits. Note that if this structure is used, the control wire currents of NOR gates are in the same direction and the control currents of XNOR gates are in opposite directions.

The use of this spin-diode logic family for computing has significant implications for circuit design. As the spin-diode has unique properties, such as its timing, power dissipation, and fan-out characteristics, the circuit design process must fundamentally change.

Switching speed in this logic family is determined by the time required for a change in magnetic field to affect the magnetic polarization of the spin-diode p-region. This is in contrast to conventional CMOS circuits, in which switching speed is limited by the formation or destruction of a channel through the motion of electrons. The process of magnetic polarization switching is faster than channel formation, as the time required to switch spin states is less than the speed of electrons within the substrate. Preliminary experimental results show a spin relaxation time of about 1 ps [27]. As this logic family is based on current rather than voltage, there is no need for the buildup of charge. Therefore, capacitive effects in the spin-diodes will not add significantly to the delay through an *RC* interconnect. However, the inductance of the magnetic shield will add to the wire impedance, slowing the spin-diode circuits through mechanisms similar to those found in conventional CMOS circuits.

The mechanism of power dissipation is profoundly different in this logic family. In CMOS circuits, there are two sources of power dissipation: the dynamic power used to switch the state of a gate, and the static power used when a gate is at steady state. In this spin-diode logic family, there is only static power dissipation, and no dynamic power dissipation. This behavior is because the anode and cathode of each spin-diode are always connected to $V_{DD}$ and ground, respectively, and no charge needs to accumulate to switch a voltage state.

The low power-delay product (PDP) of this logic family shows the potential of spin-diode logic to replace CMOS. This

value is calculated as

$$\mathrm{PDP} = \frac{I_{\mathrm{ON}} + I_{\mathrm{OFF}}}{2} V_{\mathrm{DD}} t_D. \tag{4}$$

Assuming a circuit in which speed is limited by spin-switching, the propagation delay $t_D$ is about 1 ps, as discussed above. Based on previously measured spin-diodes and a $V_{DD}$ of 0.4 V, $I_{\mathrm{on}}$ is about 200 mA, resulting in a PDP of about $10^{-13}$ J. This is close to the CMOS value of $10^{-16}$ J, despite the significantly smaller size of CMOS devices [28]. Provided a significant increase in paramagnetism, the current through a spin-diode scaled to 30 nm will decrease by a factor of $10^8$, resulting in a PDP of approximately $10^{-21}$ J. The realization of a computing system with such high efficiency would be revolutionary.

As implied in Section III, the spin-diode is most effective when implementing inverters, NOR gates, XNOR gates, and OR gates. While other logic functions, such as AND and NAND, can be implemented with combinations of these basis gates, these logic functions require additional gates, resulting in greater area, delay, and power consumption. It is thus worthwhile to consider the implementation of larger logic blocks, as it may frequently be difficult to optimize smaller logical functions. Most logical functions can be implemented in this logic family with many fewer devices than their Si CMOS counterparts, as each diode has the equivalent functionality of at least two transistors. For example, an adder is implemented with six diodes, which is far more compact than is possible in CMOS. The multiplexer, however, is not easily optimized in this logic family. When a multiplexer is an element of a combinational logic circuit, it should be considered as part of a larger circuit.

Another unique aspect of this logic family is its concept of "fan-out." As an "input" to a device is merely a wire that runs near the diode, this wire can be used as an input to multiple devices without degrading the signal. This structure is possible because the positive and negative terminals of each diode are connected through wires directly to $V_{DD}$ and ground, respectively, and there is no constraint on the wire path or length.

## V. Conclusion

The introduction of magnetoresistive semiconductor diodes makes possible the creation of a diode logic family providing significant improvements over CMOS. Spin-diode logic can be exploited to use fewer devices than comparable CMOS circuits, potentially resulting in increased speed and density without the excessive power and manufacturing complexity caused by Si transistor scaling. Spin-diode logic not only exhibits advantages for particular specialized circuits, but for logic in general. These devices and the accompanying logic family have the potential to replace CMOS and thereby have a major impact on the future of computing.

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