Invited Paper

High-performance spintronic computing with magnetoresistive semiconductor heterojunctions

Joseph S. Friedman[a]*, Bruce W. Wessels[a,b], and Alan V. Sahakian[a,c]

[a]Electrical Engineering & Computer Science
[b]Materials Science & Engineering
[c]Biomedical Engineering
Northwestern University, Evanston, IL 60208 USA

ABSTRACT

Two recently proposed spintronic logic families, spin-diode logic and emitter-coupled spin-transistor logic, provide an opportunity for high-performance cascaded logic circuits. These logic families make use of magnetoresistive semiconductor heterojunctions, in which the presence of a magnetic field causes a large increase in resistance. Spin-diode logic and emitter-coupled spin-transistor logic produce highly compact circuits with superior speed and power characteristics. In particular, circuits realized in these logic families use three to ten times fewer devices than conventional CMOS. Additionally, there is minimal dynamic power dissipation, presenting a pathway for low power high performance computing beyond 10 GHz.

Keywords: Spintronics, beyond-CMOS computing, spin-diode logic, emitter-coupled spin-transistor logic, magnetoresistive semiconductor heterojunction, spintronic logic, emerging technology, next generation computing

1. INTRODUCTION

Electrical computation of logical functions is performed by a set of switching devices that guide the flow of electrons through a circuit. The switches are structured as a logic family, in which devices are connected in an organized manner to efficiently evaluate logical operations. Numerous logic families are used for computation based on an assortment of devices, each featuring unique characteristics and tradeoffs. Logic families need to be designed to exploit the particular properties of their component devices.

The utility and effectiveness of a logic family for general computing is measured by its ability to efficiently perform computations on a large scale. The superior characteristics of the complementary metal oxide semiconductor (CMOS) logic family have resulted in its dominance in general-purpose computing. This logic family derives its strengths from its component devices, complementary metal oxide field-effect transistors (MOSFETs) fabricated with Si.

The impressive and increasing prevalence of computers and computing technology is a result of rapidly increasing processing capabilities. These increasing capabilities are primarily a result of improvements in device characteristics derived from miniaturization[1]. The impending end of the scaling of Si MOSFETs, however, threatens to impede further advancements in electrical computing[2]. In order to maintain the rapid progress of computing capabilities, new devices and/or logic families are required. Not only must individual gates be highly efficient, but it must also be possible to cascade these gates to perform complex logic functions.

The ability to switch a logic gate through control of electron spin is the fundamental concept underlying spintronic logic circuits. By using electron spin along with charge, new avenues for manipulating signal flow become available[3]. It is therefore possible to develop logic devices with additional capabilities that are more efficient, leading to logic circuits with improved characteristics[4]. While electron spin has found a ready application for computing in memory structures

*jf@u.northwestern.edu

Spintronics VI, edited by Henri-Jean Drouhin, Jean-Eric Wegrowe, Manijeh Razeghi, Proc. of SPIE Vol. 8813, 88132E · © 2013 SPIE
CCC code: 0277-786X/13/$18 · doi: 10.1117/12.2023117

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

such as hard drives and magnetoresistive random-access memory (MRAM), the difficulty in cascading these devices has prevented its incorporation in logic structures.

The recent development of magnetoresistive semiconductor heterojunction devices makes possible the creation of new spintronic logic families. In particular, spin-diode logic (SDL) and emitter-coupled spin-transistor logic (ECSTL) exploit the unique characteristics of these devices to perform cascaded logic using entirely different principles than with conventional CMOS. These novel logic families have the potential to provide computation with exceptional efficiency and performance, and may therefore replace CMOS as the primary building block for general-purpose computing.

2. MAGNETORESISTIVE SEMICONDUCTOR HETEROJUNCTION DEVICES

Various materials and devices have been created that exhibit magnetoresistance; that is, the resistance of the material is affected by an externally applied magnetic field. Positive (negative) magnetoresistance has been defined as an increased (decreased) resistance in response to this magnetic field. While negative magnetoresistance has been observed for some materials, recent experiments with Mn-doped III-V semiconductor heterojunction diodes and bipolar junction transistors (BJTs) exhibit large positive magnetoresistance.

2.1 Spin-Diode

A magnetoresistive semiconductor heterojunction spin-diode is produced by doping a semiconductor p-n junction with an element that has a strong interaction with a magnetic field. In an example semiconductor heterojunction, shown in Figure 1, Mn is added to a III-V material to form the paramagnetic p-type layer[5,6]. The spin-diode acts as a conventional diode in the presence of zero or low magnetic fields, with a high ratio of forward current to reverse current. However, when a magnetic field is applied across the junction, the current I decreases significantly. When the voltage is increased, the I_{ON}/I_{OFF} ratio increases, where I_{ON} is the zero-field current and I_{OFF} is the current at a higher field. A high ratio is useful as it supports differentiation between two digital states.

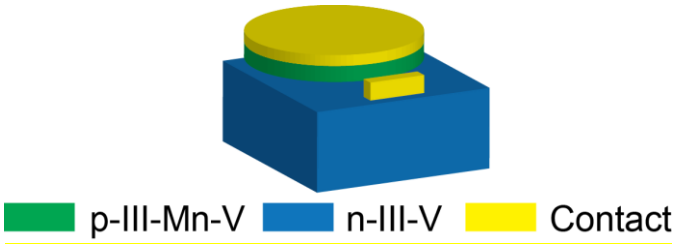

Figure 1. III-V/III-Mn-V heterojunction diode.

2.2 Spin-Transistor

Analogous to the spin-diode, the recently developed pnp bipolar magnetic junction transistor[7] has been created by doping the emitter of a InAs transistor with Mn, as shown in Figure 2. The base-emitter junction exhibits magnetoresistivity and similar to the spin-diodes discussed previously, while the base-collector junction behaves conventionally. In the presence of a magnetic field, the base-emitter junction becomes resistive, preventing current from flowing across the junction[8]. Therefore, in the presence of a magnetic field, a forward-biased base-emitter junction in the spin-transistor will behave similarly to a reverse-biased base-emitter junction in a conventional BJT. In both cases, the transistor will not produce large currents, and will remain cut-off rather than in the forward-active region. A more thorough discussion of the effect of a magnetic field on a spin-transistor can be found elsewhere[9].

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

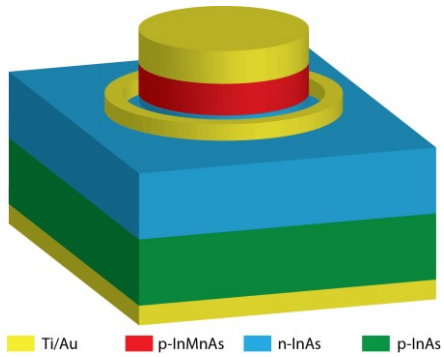

Figure 2. InAs/InMnAs spin-transistor.

2.3 Control Wire

While these magnetoresistive devices are interesting in their own right, the ability to cascade these devices to implement logical functions presents exciting opportunities. As the flow of charged particles produces a magnetic field, a current flowing near a magnetoresistive device will affect its resistivity. Therefore, control wires alongside a spin-diode or the base-emitter junction of a spin-transistor can be exploited to perform logic.

As shown in Figure 3, metal wires are placed parallel to the plane of the junction, isolated by an insulator. These wires control the junction's magnetoresistive state, as the current through the wire creates a magnetic field perpendicular to the plane of the junction. Under zero or small current, the junction is in its conductive state; a large control current supports the resistive state. Depending on the relative direction of the two currents, the associated fields combine either constructively or destructively. If the currents in the two wires travel in opposite directions, the fields will add, again suppressing the current; if the currents are in the same direction, the fields will cancel, allowing current to flow through the device. These features form the building blocks of the logic families discussed below.

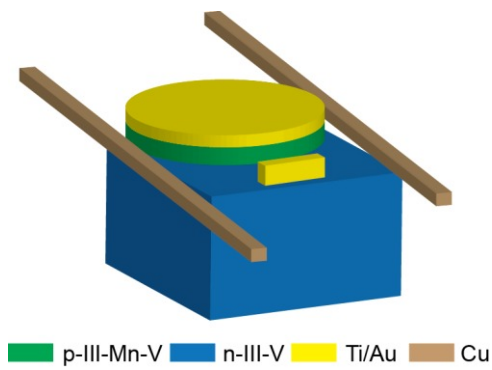

Figure 3. Magnetoresistive heterojunction with two control wires.

3. SPIN-DIODE LOGIC

Logic styles and circuit architectures should be reconsidered in order to fully utilize new materials and devices. While CMOS transistors and logic have dominated Si-based circuits[10], other devices and logic families exhibit significant advantages. Diode logic is elegant in several respects, such as simple OR gates and single junction devices that allow for compact circuit structures. Circuits based on diode logic use fewer devices than their CMOS counterparts, and therefore potentially consume less power and area while operating at higher speeds. Diode logic, however, has historically been impractical due to the inability of a diode to act as an inverter[11]. As inversion is a necessary function of a complete logic family, standard diodes can only perform complex logic functions in concert with transistors.

The recent invention of the magnetoresistive spin-diode solves this problem, as it allows for the creation of a complete cascaded logic family composed solely of spin-diodes, including an inverter[12,13]. This logic family is composed solely of spin-diodes; no transistors are required. SDL is therefore the first example of a complete diode logic family. As such,

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

SDL provides the simplicity advantages of a two-terminal device structure while exploiting the efficiencies of diode logic.

3.1 Logic Family Structure

The SDL family is constructed by connecting the n- and p-regions of spin-diodes directly to ground and the circuit's high voltage, V_{DD}, respectively. Each spin-diode is therefore forward biased. The wires making these connections are routed through the circuit to form the control wires for other spin-diodes. These control wires produce magnetic fields through these other spin-diodes, affecting their states without an electrical connection. The output current of a spin-diode can therefore be used as the input of a large number of other spin-diodes. As the spin-diodes are connected directly between V_{DD} and ground, there is a constant flow of current that is minimally affected by switching frequency.

The SDL state variable is current. The binary SDL states are the currents produced by the spin-diodes in their conductive and resistive states. A digital '1' is defined by the spin-diode conductive state resulting from a control wire propagating the '0' state; a digital '0' is defined by the resistive state resulting from a control wire propagating the '1' state. As discussed above, metal wires control the diode's magnetoresistive state, as the currents through the wires create magnetic fields perpendicular to the plane of the junction. Under zero or small net current, there is minimal magnetic field through the spin-diode. The spin-diode therefore functions as a conventional forward-biased diode, allowing a large current to flow in this conductive state. This small net current can be achieved either through having minimal current flow through the control wires, or two equal currents through control wires oriented such that the resulting magnetic fields through the spin-diode are in opposite directions. The flow of a large net current through the control wires produces a large magnetic field through the spin-diode. This activates the magnetoresistive properties of the spin-diode to suppress current flow and force the spin-diode into a resistive state.

3.2 Basis Logic Gates

Every SDL basis logic element is composed of at most a single diode: inverter, NOR gate, XNOR gate, and OR gate. In each of these configurations, the positive terminal of the diode is connected to V_{DD}, while the negative terminal is routed through the circuit before eventually being grounded. Therefore, in the absence of current through the various control wires, each of these diodes propagates a '1', and the configuration of the control wires dictates the logical function of each gate.

An inverter, the simplest gate, is shown with its symbol in Figure 4(a,b). The positive terminal of the spin-diode is connected to V_{DD} and the negative terminal is connected to ground through the output loop. The input current I_A is routed alongside the diode and induces a field proportional to its current. If I_A is a '1', it creates a large magnetic field, thereby reducing the current through the diode, and causing the output current I_O to propagate a '0'. If I_A is a '0', it does not create a sufficient magnetic field through the junction, and a '1' is propagated. In conventional CMOS circuits, two transistors are required to perform this inversion function.

The addition of a second input current I_B results in the NOR gate of Figure 4(c), for which the symbol is shown in Figure 4(d). In this arrangement, the presence of a current in either of the two inputs I_A or I_B results in a magnetic field through the diode oriented in the same direction. This magnetic field activates the spin-diode magnetoresistance, forcing the diode into the resistive state and attenuating the current. In the case of high currents on both inputs, the output current is doubly suppressed. Therefore, if at least one of the two inputs is a '1', the output propagates a '0'; otherwise, there is no magnetic field through the spin-diode, and the output is a '1'.

The XNOR in Figure 4(e) is identical to the NOR gate in terms of device structure, but its relative placement within a circuit produces a different function. As the two currents flow in the same direction, each current creates a magnetic field through the diode in the opposite direction. Therefore, if both inputs are '1', there is no net magnetic field through the diode, and a large current flows, propagating a '1'. The XNOR symbol is shown in Figure 4(f). This single device SDL XNOR gate is significantly more compact than the standard twelve device CMOS implementation.

As the magnitude of the currents defines the digital states, an OR gate is constructed simply by merging two wires (therefore, no symbol is needed). As shown in Figure 4(g), the output current I_O is equal to the sum of the two input currents. By placing an OR gate as an input to another gate, a variety of logic functions with more than two inputs can be implemented.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

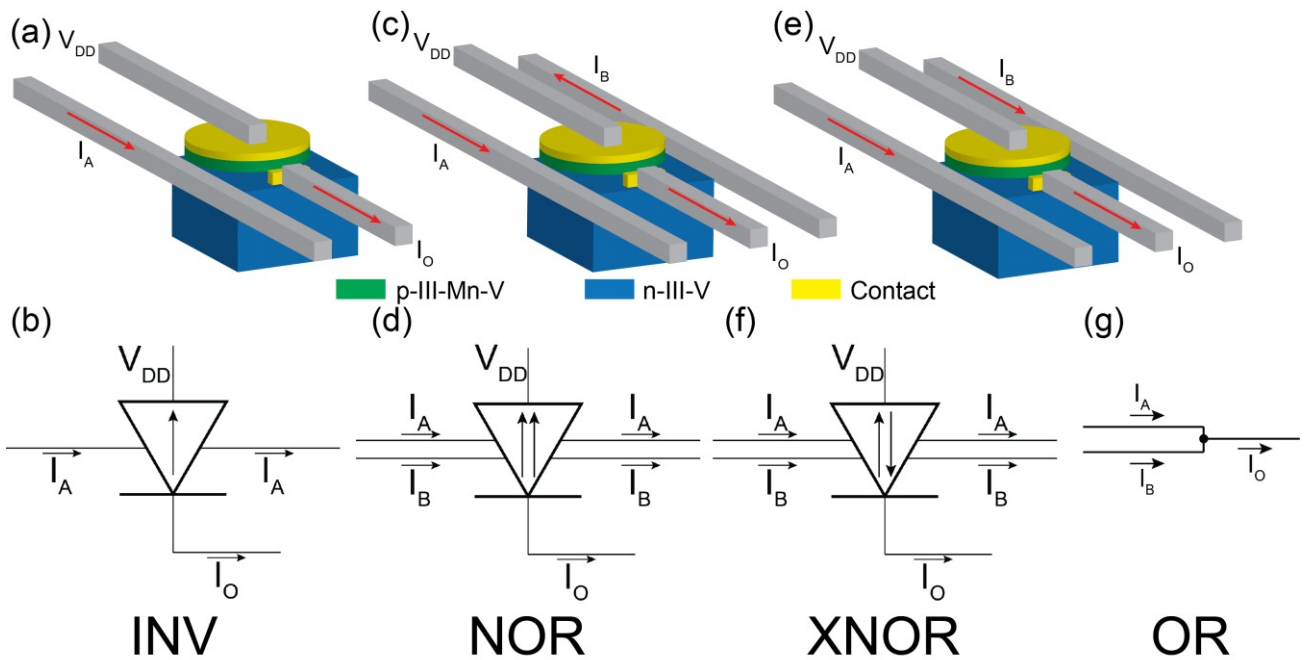

Figure 4. (a) Inverter consisting of input wire with current I_A routed alongside the diode to control the output current I_O. The positive terminal is connected to V_{DD} and the negative terminal is connected to ground at some distant part of the circuit. A high input current results in a magnetic field that suppresses the output current. (b) Symbol for SDL inverter. (c) Additional input current I_B results in a NOR gate. A high current on either input suppresses the output current. In the case of high currents on both inputs, the output current is doubly suppressed. (d) Symbol for SDL NOR gate. (e) Inverting the direction of I_B produces an XNOR gate. In this configuration, a high current on exactly one of the input wires suppresses the output current. Unlike the NOR gate, high currents on both inputs create canceling magnetic fields, allowing a high current to flow through the output. (f) Symbol for SDL XNOR gate. (g) OR gate formed by the summation of currents satisfying the principle of conservation of charge.

3.3 Circuits

These four basis logic elements can be arranged to implement any logical circuit. While the functions are logically equivalent to traditional CMOS circuits, this spin-diode logic family has a starkly different structure. A common circuit is a one-bit full adder, shown in Figure 5, which calculates a one-bit sum and carry-out based on the addition of two bits and a carry-in[14]. There are three inputs (A, B, and C_{IN}) and two outputs (C_{OUT} and Sum), optimized for this logic style as

$$C_{OUT} = (A \wedge B) \vee (A \wedge C_{IN}) \vee (B \wedge C_{IN}) = \overline{\overline{A \vee B} \vee \overline{A \vee C_{IN}} \vee \overline{B \vee C_{IN}}} \tag{1}$$

$$Sum = A \oplus B \oplus C_{IN} = \overline{\overline{A \oplus B} \oplus C_{IN}} \tag{2}$$

As illustrated in the figure, Sum is generated by cascading two XNOR gates. In XNOR1, A and B are inputs, and in XNOR2, one input is C_{IN}, and the other input is the signal propagated by XNOR1. In both gates, if the two inputs are the same, a '1' is propagated. If the two inputs are different, a '0' is produced. Similarly, C_{OUT} is achieved with three NOR gates, an OR gate, and an inverter. NOR1, NOR2, and NOR3 each propagate a '0' if either input is a '1'; when these propagated currents are summed in OR1, a '0' is propagated unless at least two of the initial inputs are '0'. This value is inverted to generate C_{OUT}.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

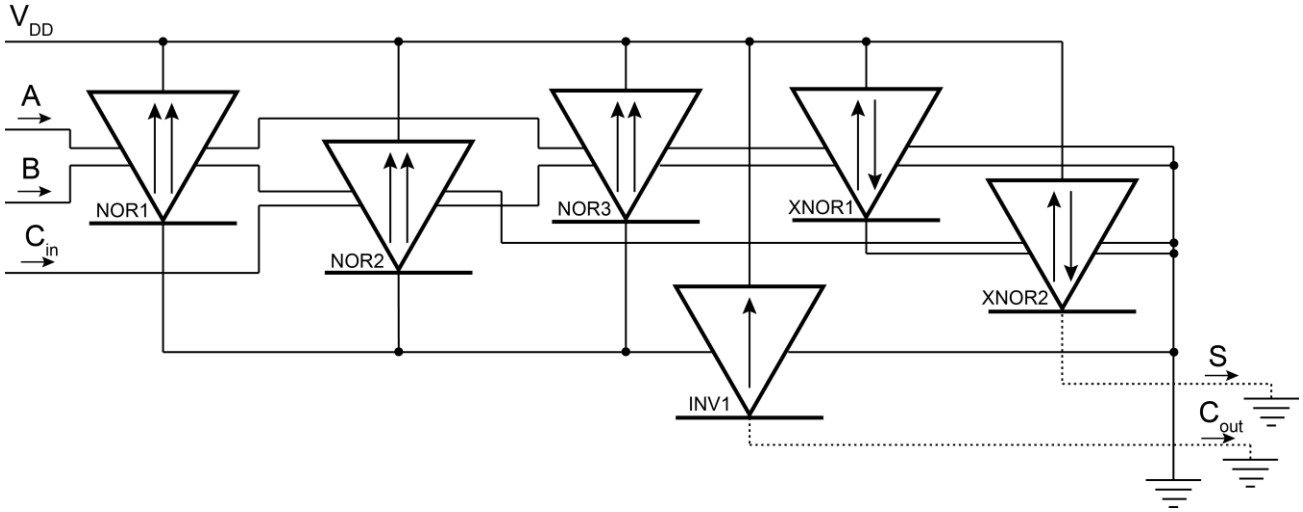

Figure 5. SDL full adder.

A two-to-one multiplexer is another useful circuit that can be built with this logic family. As shown in Figure 6, INV1 produces an inverted select signal. The select and inverted select signals are routed, respectively, through NOR gates alongside A and B. Each NOR gate propagates a '0' unless a signal with a '0' has been selected. These signals are combined and inverted such that a '1' is propagated unless a signal with a '0' has been selected.

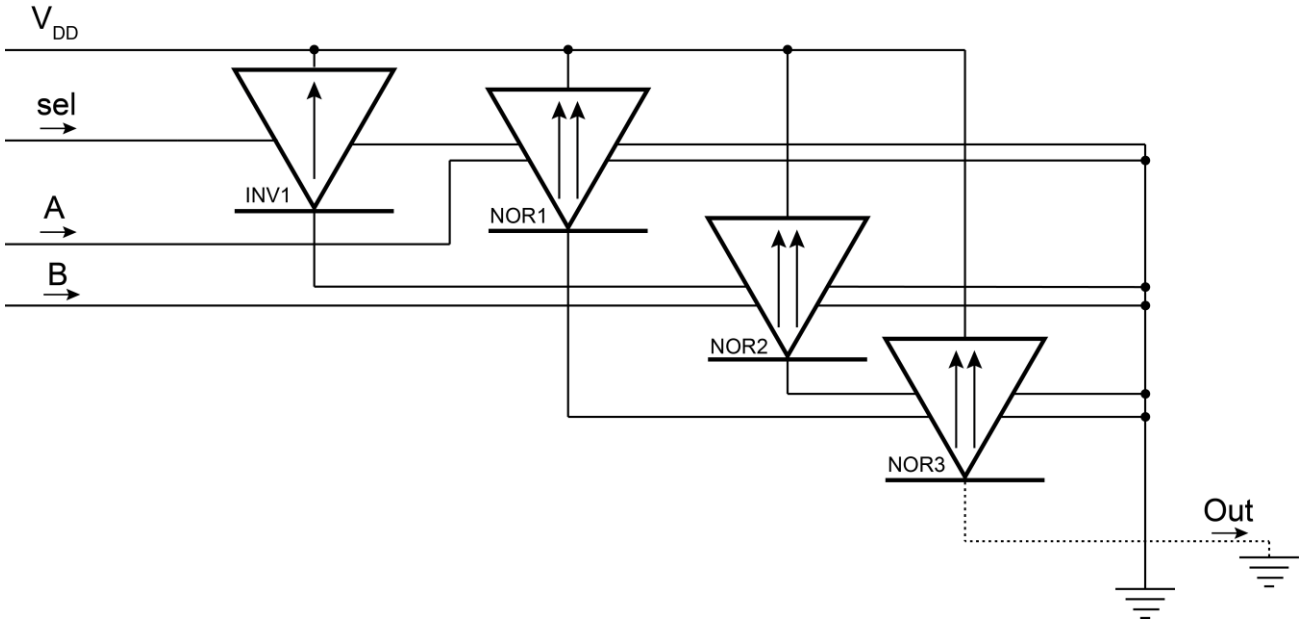

Figure 6. SDL 2:1 multiplexer.

SDL also enables an intriguing and simple latch, shown in Figure 7. As seen in the diagram, each NOR latch output is routed to the other NOR input, forcing opposite values to be propagated. When one of the diodes propagates a high current, the current is suppressed in the second diode, which allows the first diode to propagate a high current, thereby maintaining a self-consistent state. To set the value stored in the latch, an external current is passed through one of the diodes. To set a '1', a current is passed through NOR1. To set a '0', a current is passed through NOR2. This circuit is a bistable inverter chain, and can be used to create stable memory storage.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

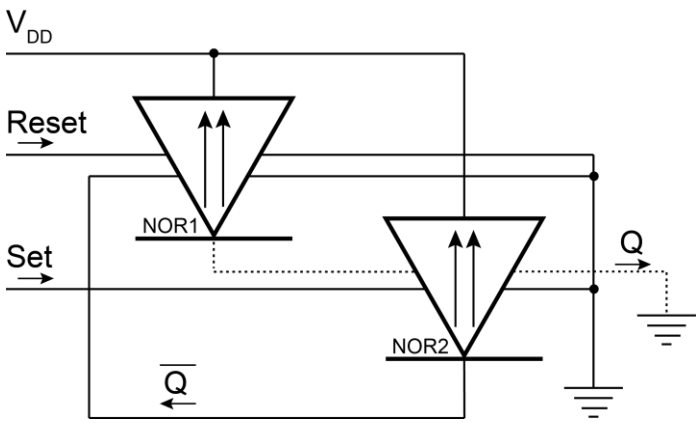

Figure 7. SDL SR latch.

These circuits are far more compact than conventional fully complementary CMOS implementations. For example, the full adder uses only six spin-diodes, which is far more compact than the typical CMOS 28-transistor implementation. The multiplexer and latch use only four and two transistors, respectively, which is roughly one-quarter the number used in CMOS. Furthermore, the use of a single device type simplifies the fabrication process.

4. EMITTER-COUPLED SPIN-TRANSISTOR LOGIC

The capabilities provided by the new spin-transistor discussed in section 2.2 inspire a reconsideration of BJT-based computing. Many logic families have been invented that utilize BJTs. Each logic family has a unique set of advantages and tradeoffs, and the choice of logic family is therefore dependent on application-specific requirements. In particular, ECL consumes a relatively large amount of power, but its small delay time makes it useful for very high-speed applications[17]. Transistor-transistor logic (TTL), in contrast, is slower and uses less power than ECL, and is therefore more useful for general-purpose computing. However, TTL has been made largely obsolete by the superior characteristics of CMOS circuits while ECL is preferred over CMOS for very high-speed applications[18].

The recently developed spin-transistors provide new opportunities for BJT logic families, particularly ECL. By replacing traditional BJTs with spin-transistors, a new logic family is created that can perform additional functions without adding any transistors, thus increasing the efficiency of the computing system[19]. These new functions reduce the number of transistors required in a circuit, thereby lowering the area, power, and signal delay. These new functions come with no tradeoffs; the only required change is a new set of rules for routing the wires.

A fundamental difference from CMOS is that large currents flow in ECL circuits during the static propagation of logical signals. While this characteristic is an issue in terms of power dissipation, it makes ECL quite suitable for exploiting the potential of spin-transistors. By carefully routing a wire whose current varies according to the logical state, it is possible to realize more complex logical functions without adding any additional circuitry.

4.1 Logic Family Structure and Basis Logic Gates

The fundamental building block of ECL, as well as our ECL-based logic family, is the differential amplifier shown in Figure 8. In this circuit, one transistor always operates in the active region and the other transistor is in the cut-off region. The relative base voltage of the two transistors determines their state. As we have used pnp transistors, the transistor with a lower base voltage is in the active region, and the transistor with the higher base voltage is in the cut-off region. If Q_1 is cut off and Q_2 is in the active region, greater current passes through Q_2 and R_2 than Q_1 and R_1. There is therefore a greater voltage drop across R_2 than R_1, resulting in a high output voltage at V_2 and a low output voltage at V_1.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

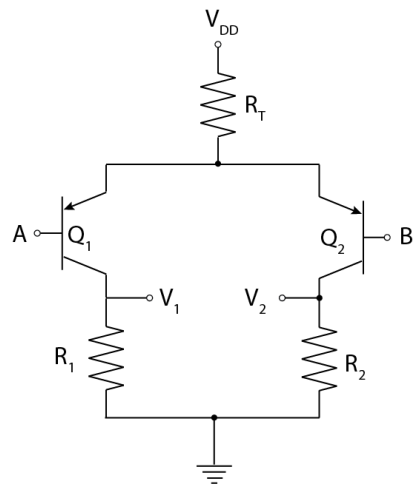

Figure 8. Differential amplifier.

This differential amplifier is used with multiple inputs to form the ECL circuits. The logical gate that can be implemented with the fewest pnp transistors is an AND/NAND gate, which therefore serves as the basis ECL function. This gate, shown in Figure 9, accepts two (or more) inputs, and produces two outputs, the logical AND and ¬AND of the inputs. The gate functions as follows: the base of the reference transistor Q_R is held at a constant voltage V_R which ensures that Q_R will switch between the active and cut-off regions depending on the behavior of the rest of the circuit. If either or both of the inputs are '0', the corresponding input transistor Q_A or Q_B is in the active region, and Q_R is cut-off. There is therefore a large current through R_{IN} and a small current through R_{REF}, causing, respectively, large and small voltage drops across those resistors. Therefore, the ¬AND output is '1' and the AND output is '0'. If both inputs are '1', Q_R is in the active region and both Q_A and Q_B are cut-off, resulting in an AND output of '1' and ¬AND output of '0'.

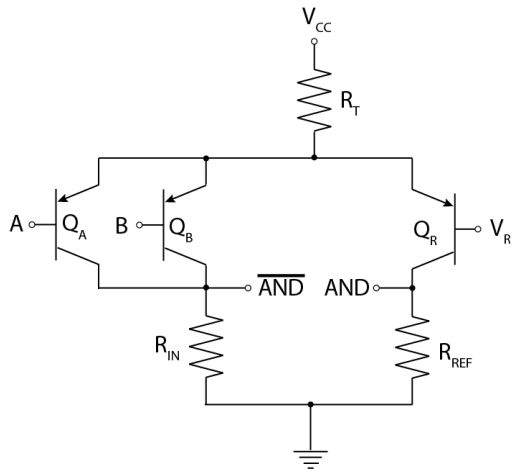

Figure 9. ECL AND/NAND gate.

We route the current through R_{IN} or R_{REF} near a spin-transistor, as discussed in section 2.3, to create an additional control signal for the spin-transistor. The general basis circuit using this scheme is shown in Figure 10, with two control wires for each spin-transistor, with directions arbitrarily chosen. There are thus two voltage inputs and six current inputs for a total of eight inputs. The presence of a net current through the control wires forces the spin-transistor into the cut-off region. Each spin-transistor can therefore perform three-input logic computation. This structure permits the computation of more complex logic within a single stage without requiring additional transistors. As each stage requires the same amount of current, the use of fewer stages implies less current flow. Since fewer transistors are required to perform a logic function, there is increased circuit efficiency in terms of power dissipation, propagation delay, and physical area.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

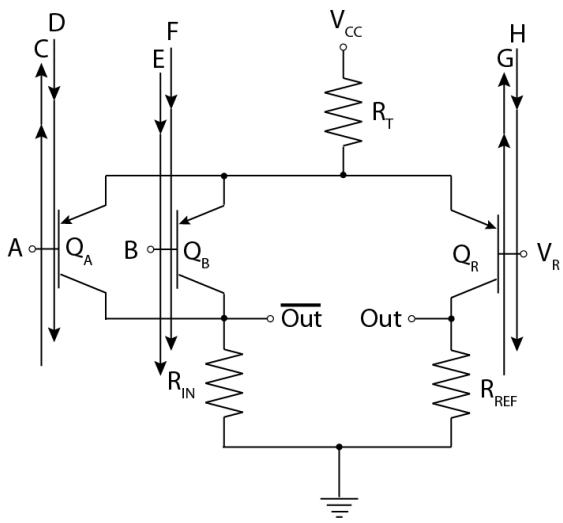

Figure 10. ECSTL basis logic gate.

4.2 Circuits

This new logic family can be used to design highly compact circuits. Multiplexer circuits, for example, can be reduced to a single stage. Specific implementations of the general circuit depicted in Figure 11 which perform (a) 2:1 and (b) 4:1 multiplexing functions. In the 2:1 multiplexer, when the Sel wire carries current, Q_1 is always in the cut-off region. When Sel does not carry current, the ¬Sel wire carries current, causing Q_2 to be cut-off. Sel chooses which spin-transistor responds to its input. The correct signal is propagated to the output in both inverted and non-inverted forms.

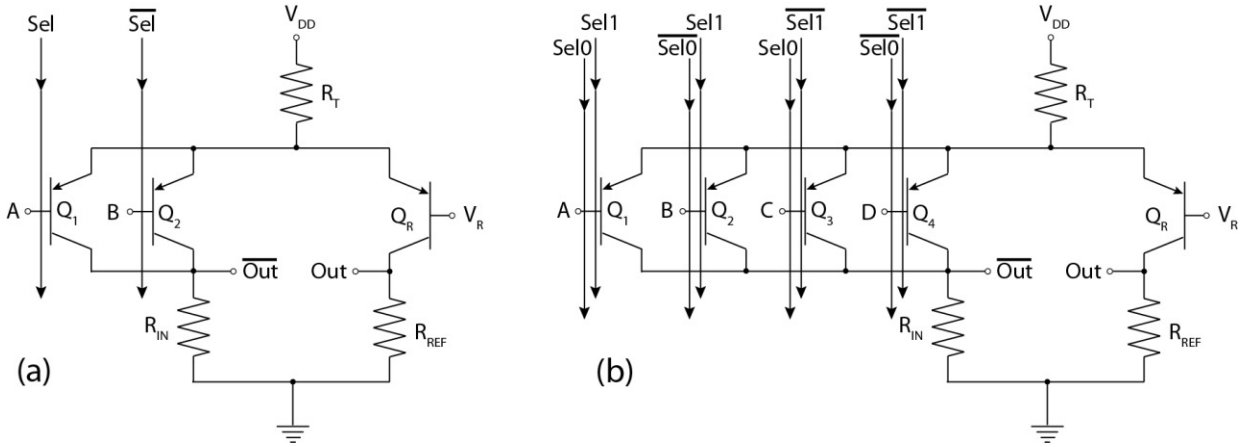

Figure 11. (a) 2:1 multiplexer and (b) 4:1 multiplexer implemented with ECSTL.

A 4:1 multiplexer can be structured in a similar way. An additional spin-transistor is required for each additional input, and two control wires are used for each spin-transistor. The control wires implement a NOR function to select the spin-transistor in operation; if either of a spin-transistor's control wires carries current, that spin-transistor is cut-off. Therefore, exactly one spin-transistor is in operation at all times, and the selected input is propagated to the output along with its complement.

These multiplexer circuits are far more compact than conventional ECL multiplexer circuits, which require multiple stages of logic and at least 20 transistors. These circuits are also more compact than standard CMOS circuits, which require twelve transistors and two stages, and are comparable to CMOS transmission gate multiplexers, which represent one of the greatest strengths of CMOS[17].

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

The full adder achieved with this logic family is also highly efficient, as demonstrated in Figure 12. This circuit contains two distinct sections, one each for the *Sum* and C_{OUT} logic. The functions have been specifically optimized for ECSTL using De Morgan's Laws:

$$C_{OUT} = (A \wedge B) \vee (A \wedge C_{IN}) \vee (B \wedge C_{IN}) = (A \wedge B) \vee (A \wedge C_{IN}) \vee (\overline{A} \wedge \overline{\overline{B} \vee \overline{C_{IN}}}) \tag{3}$$

$$Sum = A \oplus B \oplus C_{IN} = \overline{\overline{A} \wedge \overline{B \oplus C_{IN}} \vee (A \wedge \overline{\overline{B} \oplus C_{IN}})} \tag{4}$$

In the center of the circuit, a voltage divider sets a reference voltage V_R for the two reference spin-transistors, QR_S and QR_C. For the *Sum* logic, the control wires carry current in opposite directions, and therefore implement the XOR function. Q_1 is in the active region when both *A* and $B \oplus C_{IN}$ are '0', and is otherwise cut-off. Q_2 is in the active region when *A* is '1' and $\overline{B} \oplus C_{IN}$ is '0'. If either or both Q_1 or Q_2 are in the active region, significant current flows through R_{IN}. This current causes ¬*Sum* to reach a high voltage, and Sum a low voltage. The logic for C_{OUT} and $\neg C_{OUT}$ functions similarly.

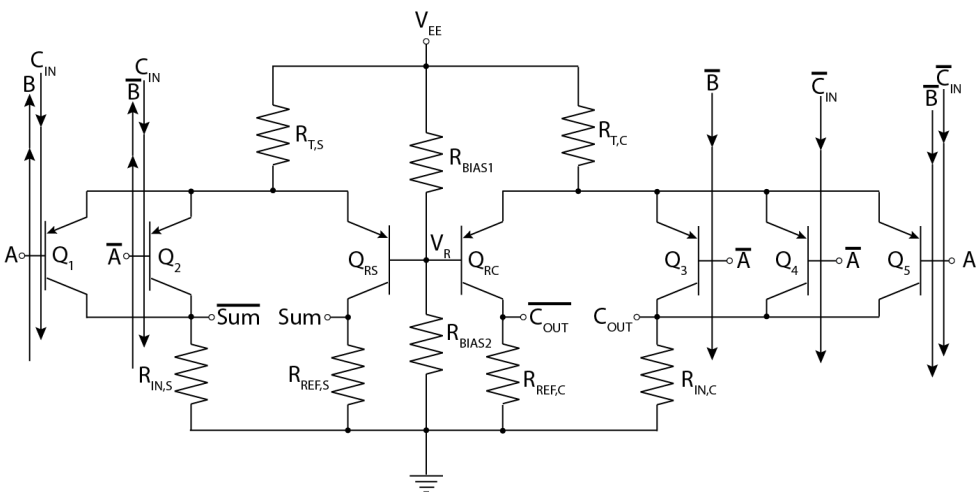

Figure 12. InAs/InMnAs spin-transistor.

This full adder is unique in its use of only a single stage of logic to produce all of the outputs. As each stage of logic adds to a signal's propagation time, the use of a single stage provides exceptional speed characteristics. It is also compact, using only seven spin-transistors. This circuit compares favorably to a standard ECL full adder, which requires 24 transistors, and the CMOS version which requires 28 transistors. In addition, both of these conventional circuits require multiple stages of logic, limiting circuit speed. ECSTL therefore provides circuits with higher performance while also decreasing power and area consumption.

5. CONCLUSIONS

SDL and ECSTL are exciting potential replacements for CMOS as Si MOSFET scaling approaches its fundamental limits. While the potential efficiency of SDL is difficult to determine as a result of its unique structure and early stage of device development, the similarities between ECL and ECSTL permit a useful and intriguing analysis. As shown in Figure 13, the power dissipation of ECL and ECSTL are nearly constant as a function of frequency, while CMOS power dissipation increases linearly with frequency. The need for temperature regulation limits the acceptable amount of power dissipation, preventing the use of ECL and beyond-3 GHz CMOS operation for general computing. Higher operating speeds are possible; however, this is not economically efficient for the vast majority of applications.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

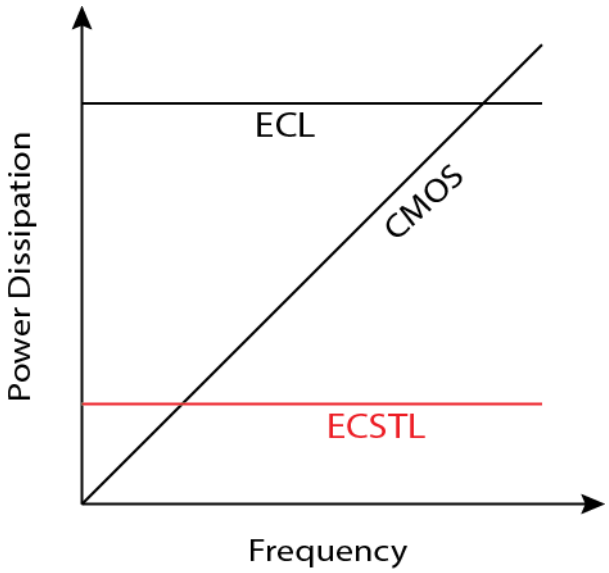

Figure 13. Power dissipation of ECSTL is less than CMOS at high frequencies and ECL at all frequencies.

The reduced power dissipation of ECSTL provides a possibility for computing beyond 10 GHz to become a reasonable economic prospect. Above this speed, ECSTL may dissipate less power than CMOS, and further speed increases do not incur substantial costs in terms of power. It might therefore become worthwhile to operate ECSTL computers at speeds on the order of 40 GHz despite the increased cooling costs. SDL provides similar possibilities for high-performance computing, potentially leading to the replacement of Si CMOS by magnetoresistive semiconductor heterojunction devices.

REFERENCES

[1] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, “Design of ion-implanted MOSFET’S with very small physical dimensions,” IEEE Journal of Solid-State Circuits 9, 256-268, Oct. 1974.
[2] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, “Device scaling limits of Si MOSFETs and their application dependencies,” Proc. IEEE 89, 259-288, Mar. 2001.
[3] E. Y. Tsymbal and I. Zutic, Eds., Handbook of spin transport and magnetism. Boca Raton, FL: CRC Press, 2012.
[4] S. A. Wolf, J. Lu, M. R. Stan, E. Chen, and D. M. Treger, “The promise of nanomagnetics and spintronics for future logic and universal memory,” Proc. IEEE 98, 2155-2168, Dec. 2010.
[5] S. J. May and B. W. Wessels, “High-field magnetoresistance in p-(In,Mn)As/n-InAs heterojunctions,” Appl. Phys. Lett. 88, 072105, Feb. 2006.
[6] N. Rangaraju, P. C. Li, and B. W. Wessels, “Giant magnetoresistance of magnetic semiconductor heterojunctions,” Phys. Rev. B 79, 205209, May 2009.
[7] N. Rangaraju, J. A. Peters, and B. W. Wessels, "Magnetoamplification in a bipolar magnetic junction transistor," Phys. Rev. Lett. 105, 117202, Sep. 2010.
[8] J. A. Peters, N. Rangaraju, C. Feeser, and B. W. Wessels, “Spin-dependent magnetotransport in a p-InMnSb/n-InSb magnetic semiconductor heterojunction,” Appl. Phys. Lett. 98, 193506, May 2011.
[9] J. Fabian, I. Zutic, S. D. Sarma, "Magnetic bipolar transistor," Appl. Phys. Lett. 84, 85-87, Jan. 2004.
[10] F. M. Wanlass, “Low stand-by power complementary field effect circuitry,” US Patent # 3,356,858, Dec. 1967.
[11] R. H. Katz, Contemporary Logic Design. Redwood City, CA: Benjamin/Cummings, 1994.
[12] J. S. Friedman, N. Rangaraju, Y. I. Ismail, and B. W. Wessels, “A spin-diode logic family,” IEEE Trans. Nanotechnology 11, 1026-1032, Sep. 2012.
[13] J. S. Friedman, N. Rangaraju, Y. I. Ismail, and B. W. Wessels, “InMnAs magnetoresistive spin-diode logic,” Proc. Great Lakes Symposium on VLSI, May 2012.
[14] J. Sklansky, “Conditional-sum addition logic,” IRE Trans. Electronic Computers 9, 226-231, Jun. 1960.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms

[15] M. Bhowmick, T. R. Merritt, K. Nontapot, B. W. Wessels, O. Drachenko, and G. A. Khodaparast, "Time-resolved spectroscopy of InMnAs using differential transmission techniques in mid-infrared," Phys. Procedia 3, 1167–1170, Jan. 2010.
[16] Mayler G. A. Martins, Felipe S. Marranghello, Joseph S. Friedman, Alan V. Sahakian, Renato P. Ribas, and Andre I. Reis, "Spin diode network synthesis using functional composition," Proc. Symposium on Integrated Circuits and Systems Design, Sep. 2013.
[17] J. Millman, Microelectronics: Digital and Analog Circuits and Systems. New York: McGraw-Hill, 1979.
[18] D. Neamen, Electronic Circuit Analysis and Design, 2nd ed. New York: McGraw-Hill, 2001.
[19] J. S. Friedman, Y. I. Ismail, G. Memik, A. V. Sahakian, B. W. Wessels, "Emitter-Coupled Spin-Transistor Logic," IEEE/ACM International Symposium on Nanoscale Architectures, July 2012.

Downloaded From: http://proceedings.spiedigitallibrary.org/ on 12/03/2013 Terms of Use: http://spiedl.org/terms