Energy efficiency challenges for all-spin logic

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As complementary metal-oxide semiconductor (CMOS) technology scaling reaches its limits, new compute-in-memory technologies such as "all-spin logic" (ASL) are being explored. Preliminary predictions indicate that ASL implemented with perpendicular magnetic anisotropy will exhibit power-delay product (PDP) and energy-delay product (EDP) compared to CMOS, supporting its candidacy as a replacement for CMOS. In recent evaluations of ASL, unrealistic parameters have been used, leading to overly-optimistic efficiency figures. This paper uses micromagnetic simulations with realistic parameters to analyze the relationships between the various device parameters and circuit parameters, and the resulting impact on PDP and EDP. This analysis indicates that the PDP and EDP of ASL is greatly inferior to CMOS with the technological parameters that are currently available. In order to overcome these challenges relating to energy efficiency, this paper also evaluates the potential to modify the device parameters to improve the energy efficiency.

1. Introduction

The "all-spin logic" (ASL) family has received much interest as a potential alternative to complementary metal-oxide semiconductor (CMOS) for the next generation of computing. ASL is based on a non-volatile spintronic device in which electron spin is used to perform logic functions in memory. Many spintronic devices have the advantage of zero static power and instant on-off abilities making them exciting candidates to replace CMOS [1–5]; however, previous evaluations of ASL's power efficiency do not use realistic values. This paper thoroughly analyzes the efficiency of ASL, revealing that ASL is less power efficient than standard CMOS with currently-available device and fabrication parameters. Given that ASL switching requires the flipping of a non-volatile magnetization with a high energy barrier, it is unsurprising that the volatile switching of CMOS devices is far faster and requires less energy consumption.

An early analysis of ASL with in-plane magnetic anisotropy by Calayir et al. [6] indicated that CMOS is more energy-efficient than ASL by several orders of magnitude. An improvement to the device structure by Iraei et al. [7] leveraging magnetostriction reduces the energy dissipation, but is still less energy-efficient than CMOS. Relatedly, Su et al.

studied the breakdown current of ASL devices, and its dependence on technological parameters [8].

Whereas these previous analyses indicated that ASL is significantly less energy-efficient than CMOS, Kim et al. [9] proposed parameters that would enable ASL with out-of-plane anisotropy to be more efficient than CMOS. While their analyses suggest that perpendicular magnetic anisotropy (PMA) ASL has lower power-delay product (PDP) than CMOS, Kim et al. does not fairly calculate the CMOS PDP and uses technological parameters for ASL that are not currently available. In particular, Kim et al.:

1. use magnetic parameters that enable an unrealistically small switching current,
2. compare 32 nm CMOS to nanomagnets with a 5 nm feature size, and,
3. reduce the CMOS supply voltage,
4. reduce the CMOS clock frequency to 25 MHz

The unrealistic parameters and unfair comparison methodology skew the resulting efficiency predictions to suggest that ASL can reasonably become more energy-efficient than CMOS.

To resolve these contradictory efficiency predictions, this paper provides a micromagnetic analysis of the energy efficiency of ASL that
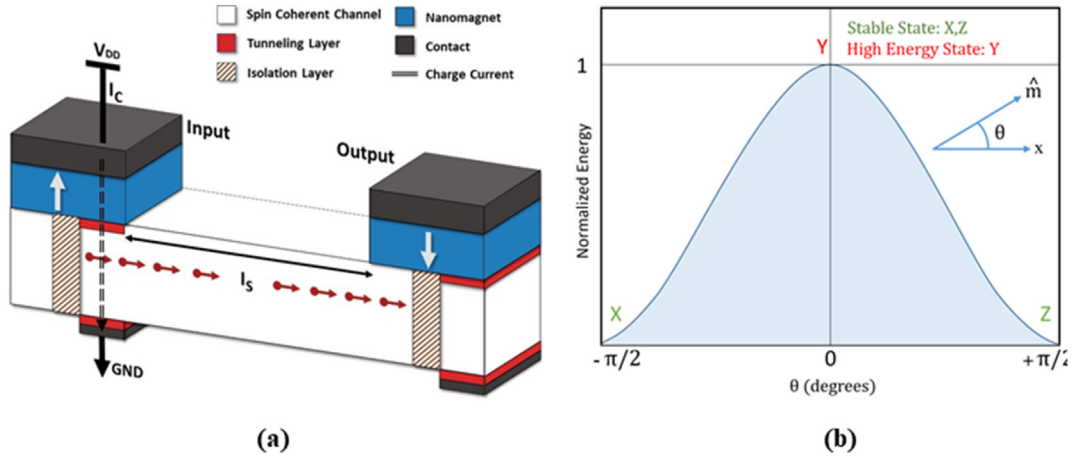

Fig. 1. (a) Illustration of an ASL unit cell. (b) Energy landscape showing the bistable nature of the nanomagnets. States X and Z are located at the zero normalized energy state and represent the two stable states. θ is the angle between output nanomagnet polarization and nanomagnet plane.

demonstrates that CMOS is indeed more energy-efficient than ASL. By using more realistic parameters, this paper shows that ASL is less efficient than CMOS with technological parameters that can be reasonably predicted.

2. ASL signal propagation

This paper begins with an introduction of the basics of the ASL design and the theory behind its structure. Simulation results are presented using various saturation magnetizations, channel lengths, nanomagnet sizes, thermal stability factor, and perpendicular anisotropy constant to evaluate the impact of these parameters on energy efficiency. Realistic values for these parameters lead to the conclusion that ASL is less power-efficient than CMOS.

In the ASL family, binary information is carried across the system via a nonlocal spin transport mechanism while logical operations are performed by the switching of a nanomagnet. Nonlocal spin transport is an energy-efficient communication method between nanomagnets without physical movement of electrons (i.e., charge current).

Device Structure and Operation. Fig. 1(a) shows an ASL unit cell that can perform both invert and buffer operations. The unit cell consists of two nanomagnets (an input and an output) connected by a spin-coherent channel which acts as the path for nonlocal spin transport. The nanomagnets have PMA for power-efficient magnetic switching [10]. The tunneling layers act as a spin filter and the insulation layer prevents feedback from output to input [11].

The nanomagnets can relax to either point X or point Z in the energy landscape of Fig. 1(b), which correspond to either a logical high (1) or a low (0) state. The input magnet polarizes the charge current produced by the applied voltage between the supply (V_{DD}) and ground (GND). For positive supply voltage, the current is polarized antiparallel to the input nanomagnet polarization while negative supply voltage polarizes the current parallel to the input magnet. The pure spin component of the polarized current diffuses through the spin coherent channel by the nonlocal spin transport mechanism and exerts a torque on the output magnet. When V_{DD} is positive, the nonlocal spin transfer torque switches the output nanomagnet antiparallel to the input nanomagnet polarization. Thus, the logical inversion operation is performed. Conversely, when V_{DD} is negative, the transfer torque switches the output nanomagnet parallel of the input nanomagnet polarization, thereby performing the buffer operation.

An alternative switching mechanism has also been proposed where the output nanomagnet is forced into the metastable energy state Y by an external power supply. Then, information carried by nonlocal spin transport determines the ultimate state of the logical operation [11].

However, this clocking scheme requires a complex overhead control circuit.

Transport Theory. The spin current flowing through the output nanomagnet can be expressed in relation to charge current (I_C) which flows through the input nanomagnet [12]as

$$|I_S| = P|I_C|exp(-L/\lambda_N) \tag{1}$$

where P is the spin-to-charge polarization factor at the interface between the input tunneling layer [8,9,13–15] and the spin-coherent channel, L is channel length, and λ_N is the spin diffusion length of the channel material [16]. The above expression can be used to define the spin polarization efficiency of electrical charge current I_C at the interface between the spin-coherent channel and the output nanomagnet as

$$\eta_{ch} = I_S/I_C = Pexp(-L/\lambda_N) \tag{2}$$

The spin current diffuses through the spin coherent channel and exerts a nonlocal spin-transfer torque (STT) on the output nanomagnet. The Landau-Lifshitz-Gilbert (LLG) equation explains the dynamics of the output nanomagnet [17–19], with an additional term for the nonlocal STT

$$\frac{\partial \hat{m}_O}{\partial t} = -\gamma \hat{m}_O \times \vec{B}_{net} + \alpha \hat{m}_O \times \frac{\partial \hat{m}_O}{\partial t} + \frac{\gamma \hbar J_C \eta_{ch}}{2eM_{sat}t_F} \hat{m}_O \times (\hat{m}_O \times \hat{m}_I) \tag{3}$$

where $\hat{m}_O$ and $\hat{m}_I$ are the normalized magnetization of the output and input magnet respectively, γ is the gyromagnetic ratio, J_C is the charge current density through the input nanomagnet, M_{sat} is the saturation magnetization, and $\vec{B}_{net}$ is the summation of demagnetization, anisotropy, exchange, and thermal magnetic field of the output nanomagnet.

3. Relationship between device parameters and energy efficiency

The theory described above is used in concert with micromagnetic simulations [20] to determine the critical current and time to switch the output nanomagnet. The PDP value is then calculated by the product of the switching time and the resistive power determined by the critical current value. It should be noted that this PDP can also be considered to be the ASL switching energy. The EDP value is determined by the product of the PDP value and the switching time. The resistance of the ferromagnet tunnel barrier is best approximated by considering the resistance across a rectangular cross-sectional area and considering the isolation layer of the ASL device in the channel beneath the ferromagnets. The parameters used in the various simulations are indicated in Table 1.

Table 1
Summary of parameters.

| Symbol	Quantity	Value
N/A	Nano-magnet dimension	40 nm × 40 nm × 1 nm [10], 10 nm × 10 nm × 2 nm [8], 5 nm × 5 nm × 4 nm [9]
A_{ex}	Exchange Stiffness	$1.3 \times 10^{-11} \mathrm{Jm}^{-1}$ [21]
λ	Spin Diffusion Length	920 nm [12], 3 μm [9]
$\mu_0 M_{sat}$	Saturation Magnetization	1.58 T [10], 1 T [20]
α	Gilbert Damping Constant	0.0055 [9]-0.007 [8]
K_u	Perpendicular Anisotropy Constant	$1.2 \times 10^6 \mathrm{Jm}^{-3}$ (for 40 nm × 40 nm × 1 nm) [10], $6 \times 10^5 \mathrm{Jm}^{-3}$ to $6.5 \times 10^5 \mathrm{Jm}^{-3}$ (for 10 nm × 20 nm × 2 nm and 5 nm × 5 nm × 4 nm) [8]
RA	Resistance-Area Product of Tunnel Barrier	0.08 $\Omega\mu\mathrm{m}^2$, 18.84 $\Omega\mu\mathrm{m}^2$ [10]
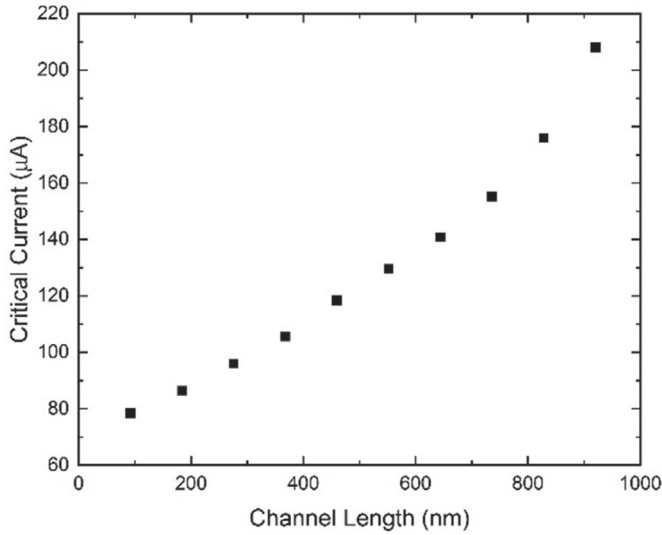
Fig. 2. Critical current as a function of channel length for PMA ASL with nanomagnet size 40 nm × 40 nm × 1 nm.

Fig. 3. Current and PDP as a function of switching time for various channel lengths and a nanomagnet size 40 nm × 40 nm × 1 nm, where the dotted and solid lines show the current and PDP respectively.

Fig. 4. EDP as a function of current for various channel lengths with nanomagnet size of 40 nm × 40 nm × 1 nm.

Relation between Channel Length and Critical Current. There is a direct relationship between channel length and critical switching current. As seen in Fig. 2, decreasing the channel length decreases the critical switching current of PMA ASL. When the spin current enters the channel, there is a minimum PDP and EDP related to the transfer of that current to the other nanomagnet. If a channel is too long or insufficient current is provided, the ASL circuit will be non-functional, as the spin current fails to cross the entire channel. A longer channel length requires a higher switching current to cover the entire distance of the channel. Therefore, the longer the channel length, the greater the critical current needed to successfully perform ASL in-memory computing operations.

It is worth noting that in ASL circuits, the impact of a fan-out greater than one on the minimum switching current is equivalent to that of a longer channel length. Fan-out requires a single nanomagnet to be cascaded through multiple spin-coherent channels [22], requiring sufficient electrical current to overcome the critical spin-current for the fan-out nanomagnets along each of spin-coherent fan-out channels. For PDP and EDP calculations, this fan-out is equivalent to an ASL gate in which one nanomagnet drives another through a longer spin-coherent channel.

Relation between Switching Current and PDP. As can be seen on the graph of PDP as a function of switching time in Fig. 3, there is a minimum PDP that is dependent on channel length. The EDP graph of Fig. 4, however, shows that the EDP continues to decrease in response to increasing currents up to 1 mA. A comparison between Figs. 3 and 4 makes it immediately clear that the minimum PDP point does not
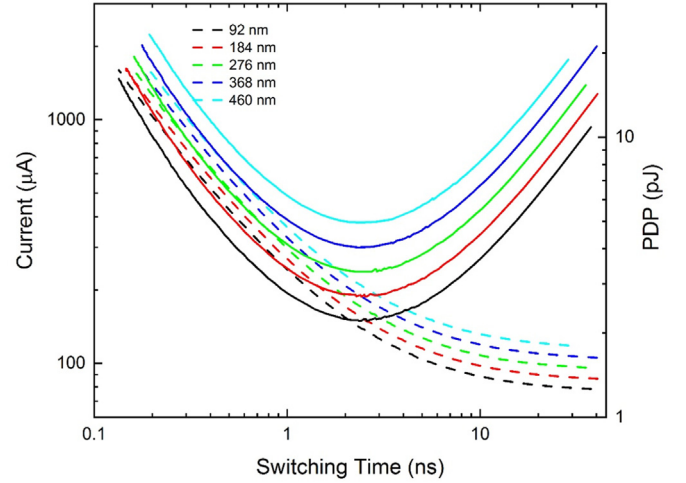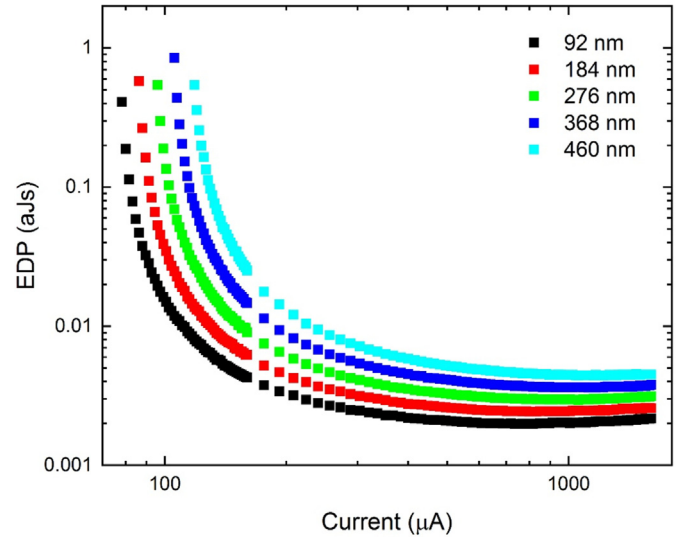
provide minimum EDP for ASL.

The relation between the current and power absorbed by the input nanomagnet in Fig. 5 shows that absorbed power increases as the critical switching current increases. Again, to reduce the EDP, the critical current needs to increase. Therefore, maximally reducing EDP increases
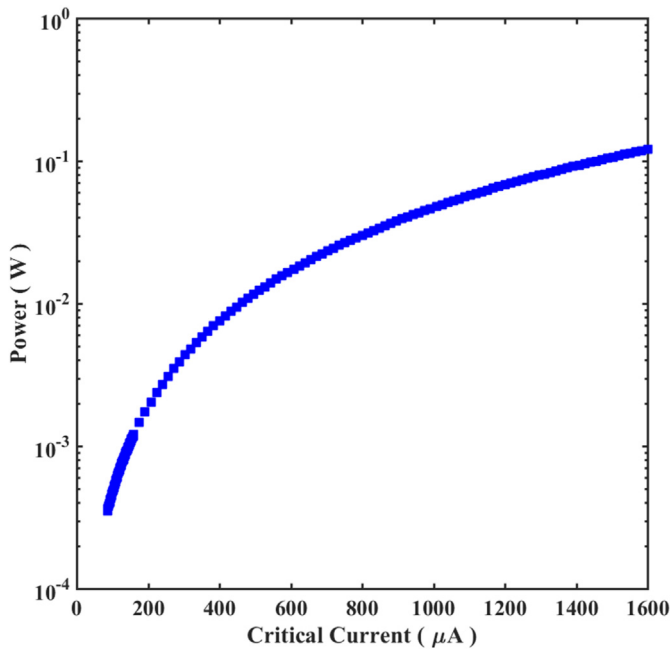
Fig. 5. Absorbed power as a function of critical switching current with nanomagnet of size 40 nm × 40 nm × 1 nm.
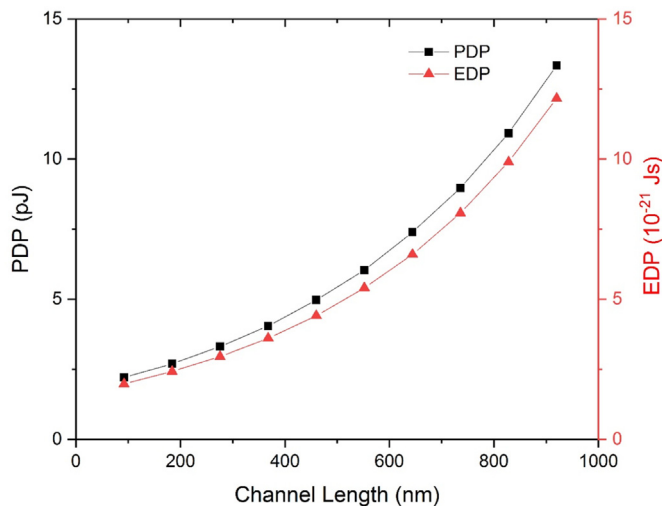

Fig. 6. Minimum PDP and EDP as a function of channel length for nanomagnet size of 40 nm × 40 nm × 1 nm.

the absorbed power density for ASL, which can lead to overheating and failure. Despite an attempt to minimize EDP, this optimized EDP is still worse than the EDP of CMOS.

Relation between Channel Length and PDP. Fig. 6 shows the direct relationship between channel length and PDP and EDP. As the channel length increases, the PDP and EDP increase as well. A longer channel length requires more power to transfer the spin from one end of the channel to the other. Without sufficient power, insufficient spin current will reach the other nanomagnet. Less power is needed to transfer the spin across a smaller distance. Therefore, the smaller the channel length in the ASL device, the smaller the PDP and EDP of the logic-in-memory operation.

As additional ASL devices are incorporated into cascaded logic circuits, the channel length continues to increase. As seen in Fig. 6, this increase drastically impacts the PDP of the system. For a channel length of 90 nm, the EDP of ASL is greater than 1000 times than that of 90 nm
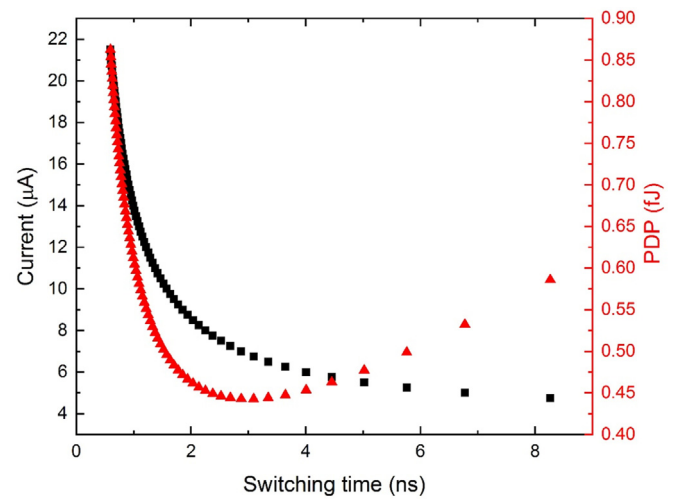

Fig. 7. Current and PDP as a function of switching time for 5 nm × 5 nm × 4 nm nanomagnet with realistic parameters.

CMOS. This enormous ratio persists across channel lengths, indicating that ASL is significantly less energy efficient than equivalently-scaled CMOS.

4. Energy efficiency superiority of CMOS over ASL

The size of the nanomagnet and the value of the magnetic parameters drastically impact the PDP and EDP of ASL. With the parameters reported by Kim et al. - nanomagnet size 5 nm × 5 nm × 4 nm with a graphene channel (spin diffusion length: 5 μm) - the PDP is in the order of 10^{-17} J [9]. However, that work used magnetic parameters that enable an unrealistically small switching current. In particular, a high thickness of 4 nm in concert with a low damping factor of 0.0055 would result in in-plane anisotropy and would not be thermally stable [10,20]. Using a more realistic set of parameters, the PDP is on the order of 10^{-16} J. The PDP of 5 nm CMOS is less than 10^{-17} J.

With the parameters reported by Su et al. for nanomagnet size 10 nm × 10 nm × 2 nm with a graphene channel (spin diffusion length: 3 μm) the PDP and EDP are on the order of 10^{-15} J and 10^{-24} Js, respectively. For 10 nm CMOS, the PDP and EDP are on the order of 10^{-17} J and 10^{-29} Js, respectively, orders of magnitude more energy-efficient than ASL in terms of both PDP and EDP.

5. Parameter improvement for increased efficiency

Given the energy efficiency advantages of CMOS over ASL, it is worthwhile to consider the possibility of increasing ASL efficiency by improving the device parameters. It is of particular interest to consider the impacts of nanomagnet size, saturation magnetization, perpendicular anisotropy constant, and thermal stability factor on energy efficiency.

Impact of Nanomagnet Size on Efficiency. Reduction in the size of the nanomagnet plays an important role in the reduction of PDP, switching time, and switching current. The larger the nanomagnet, the more PDP is required to switch its magnetization. This means the switching current takes more energy to transfer. A smaller nanomagnet means less power needed. A comparison of Figs. 7 and 8 shows that reduction in nanomagnet size decreases the switching time for critical PDP. Figs. 9 and 10 show that decreasing the nanomagnet sizes results in a reduction in EDP. To bring the PDP and EDP of PMA ASL to the order of present CMOS technology PDP (i.e. 10^{-18} J), a significant reduction in the size of nanomagnet is required.

Impact of Saturation Magnetization on Efficiency. For ASL in-memory computing to function properly, the material needs to be ferromagnetic,
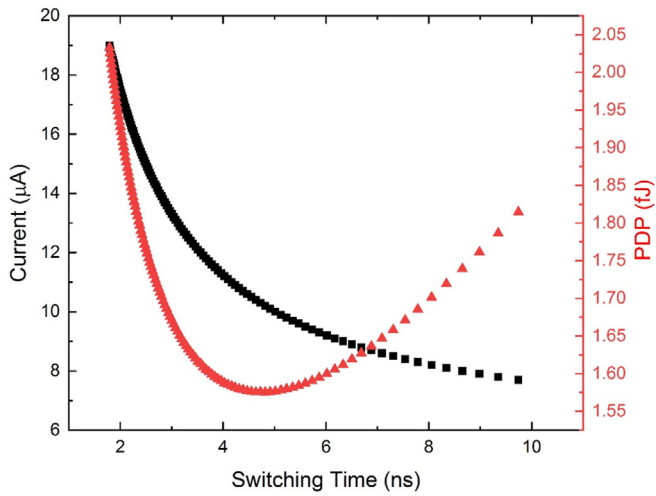
Fig. 8. Current and PDP as a function of switching time for 10 nm × 10 nm × 2 nm nanomagnet with realistic parameters.
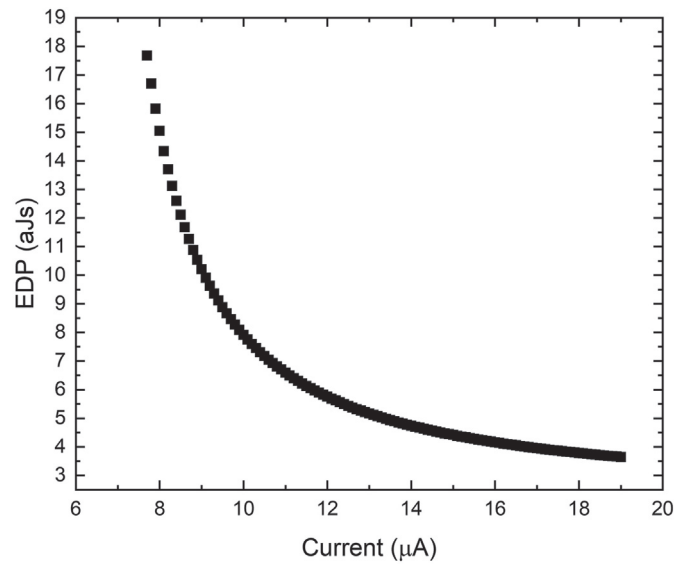

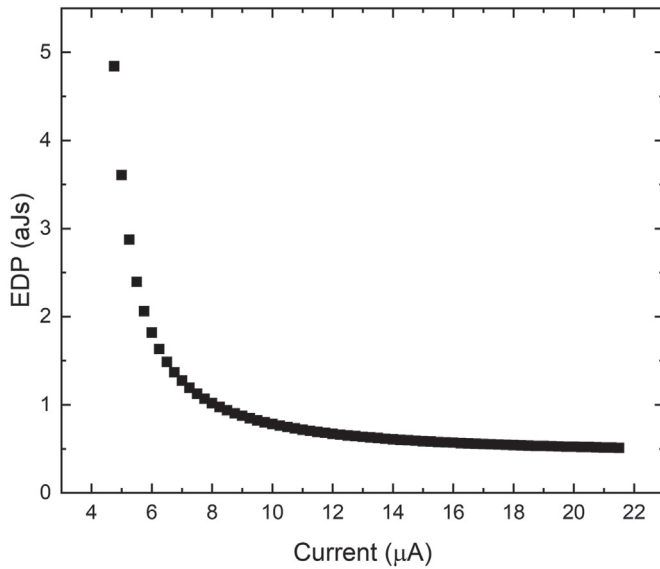**Fig. 10.** EDP as a function of current for 10 nm × 10 nm × 2 nm nanomagnet.

Fig. 9. EDP as a function of current for 5 nm × 5 nm × 4 nm nanomagnet with realistic parameters.
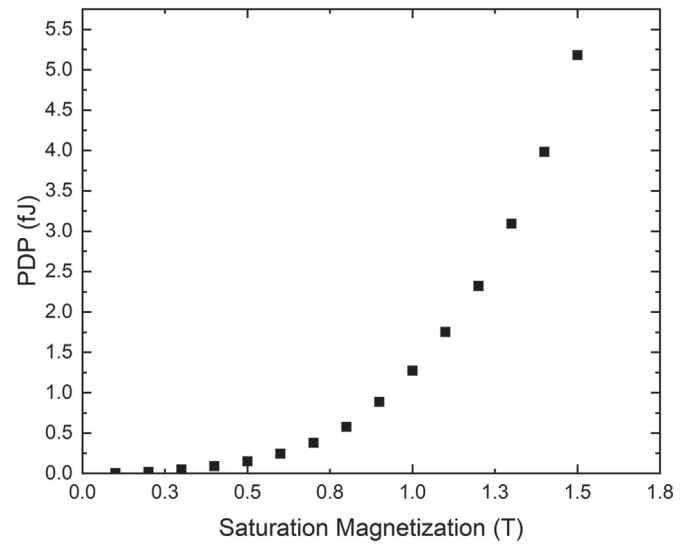

Fig. 11. PDP as a function of saturation magnetization for PMA ASL with nanomagnet size 10 nm × 10 nm × 2 nm and 20 nm channel length.

thereby requiring saturation magnetization values within a particular range. Changing the saturation magnetization of the material greatly impacts the PDP of PMA ASL. Fig. 11 shows that the smaller the saturation magnetization, the lower the PDP. The higher this saturation magnetization is, the more power is needed to switch the magnetization. Therefore, reducing the saturation magnetization leads to a reduction in PDP, but saturation magnetization reduction is limited by the ferromagnetic material's properties [23].

Impact of Perpendicular Anisotropy Constant and Thermal Stability Factor on Efficiency. The thermal stability factor is a measurement of non-volatility of the nanomagnets that is dependent on the perpendicular anisotropy constant. In memory applications, a higher thermal stability factor is required to achieve longer data retention time [10]. For ASL logical operations, reducing the thermal stability factor may result in logical failures due to thermal nanomagnet switching [9]. As shown in the micromagnetic simulation results of Fig. 12, a reduction in thermal stability factor decreases the PDP of PMA ASL. However, this reduction occurs at a slower rate than achieved by reducing saturation magnetization. While saturation magnetization reduction is limited by the ferro-

magnetic properties of the nanomagnet, the perpendicular anisotropy constant can be feasibly reduced by increasing the thickness of the nanomagnet [10]. However, Fig. 12 demonstrates that reducing the perpendicular anisotropy constant is not sufficient to reduce the PDP below that of CMOS. Furthermore, efforts to reduce the thermal stability factor and perpendicular anisotropy constant will also result in computational errors due to the thermal nanomagnet switching.

6. Discussion

While Kim's evaluation of PDP may indicate a significant improvement over conventional CMOS, the magnetic parameters considered in that work do not enable thermally-stable perpendicular anisotropy. As thermal stability is necessary for ASL logic-in-memory, the system would not function as desired with the parameters from Kim. (It is worth noting, however, that ASL may be found useful for alternative models of computation beyond logic-in-memory.) Moreover, Kim et al. unfairly treats 32 nm CMOS technology by analyzing it with reduced voltage and 25 MHz frequency and comparing it with a 5 nm ASL fea-
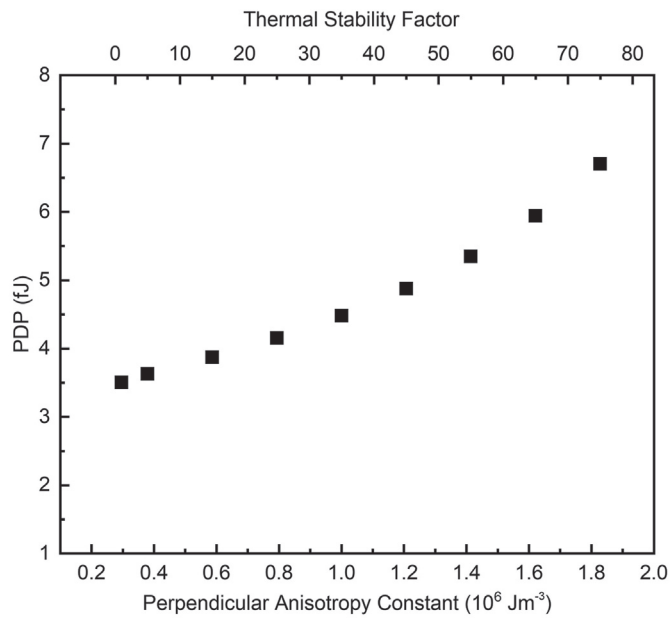
Fig. 12. PDP as a function of perpendicular anisotropy constant and thermal stability factor for PMA ASL with nanomagnet size 10 nm × 10 nm × 2 nm and 20 nm channel length.
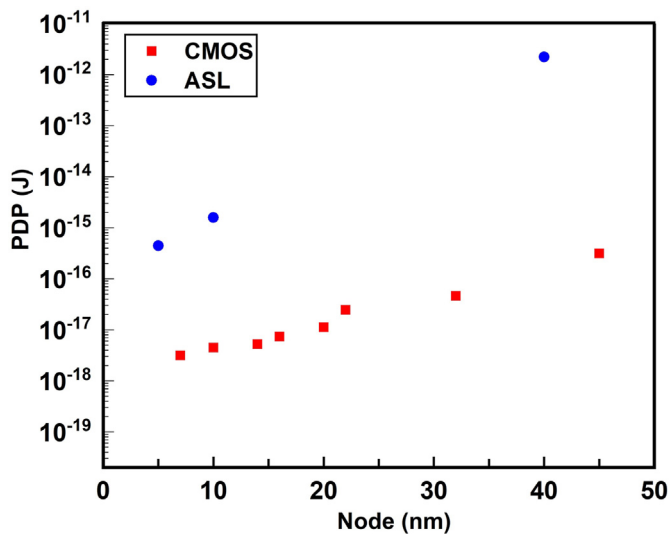

Fig. 13. Comparison of PDP of CMOS (red squares) and ASL (blue circles) across various technology nodes.

ture size. For practical ferromagnets in sub-10-nm technology nodes, the PDP required by ASL is at least 100 times the PDP required by CMOS logical operation, as shown in Fig. 13.

While a system-level simulation is necessary for predicting the total energy consumption of complete systems, preliminary comparisons between technologies can be performed by evaluating equivalent elementary logical operations under the assumption that the total energy scales linearly with the number of elementary operations required. This analysis neglects non-linearities in this scaling, as well as static power dissipation, the potential leveraging of in-memory computing, and the clock distribution network required to clock every ASL gate during each clock cycle. While these simplifications may impact the comparison, their impacts will be far smaller than the enormous inferiority of ASL efficiency relative to CMOS. In this work, we consider the invert and buffer operations as the elementary unit operations for both CMOS and

PMA ASL. The results shown in Fig. 13 clearly demonstrate that the PDP of PMA ASL is multiple orders of magnitude higher than the PDP of CMOS.

7. Conclusion

A thorough analysis of ASL reveals that under current technological conditions, the PDP and EDP of ASL is significantly greater than CMOS. Past studies of the PDP and EDP of PMA ASL presumed technological capabilities that may be unrealistic, and these unrealistic assumptions enabled the invalid conclusion that ASL is more efficient than equivalently-scaled CMOS. With reasonable parameters, CMOS is orders-of-magnitude more efficient than ASL. This paper also analyzes the parameter improvements necessary to improve the energy efficiency of ASL. In particular, energy efficiency can be enhanced by decreasing saturation magnetization, decreasing the thermal stability factor, decreasing the perpendicular anisotropy constant, reducing nanomagnet size, shortening the channel length, and decreasing the critical currents. These technological improvements are necessary to enable ASL to compete with CMOS for the next generation of computing.

Author contributions statement

N.H. conceptualized the evaluation approaches. D.S. and N.H. performed the micromagnetic simulations. All authors contributed to the analysis and manuscript preparation. J.S.F supervised the research.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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