(FM) wire with a *long* MTJ in the center. Spin transfer/orbit torque is used to switch a DW in the FM. By controlling the DW position, we control the MTJ ratio that is parallel and use the conductance levels as gray-scale weights. We model the FM wire as 500 nm x 64 nm x 4 nm, with notches every 64 nm. We find there is a trade-off between notch depth and DW width to determine the depinning current. Using the largest notch at left of 16 nm deep and decreasing notch size by 1.6 nm per notch, we apply 10 ns current pulses to translate the DW. Starting with the DW in the lowest-energy state sitting at the largest notch, we find reliable depinning currents to move the DW to specific pinning sites (Fig. 1, top-down view). Using numbers from our MTJ measurements of TMR = 166% and RA product = 20 Ω-μm^2, we obtain analog MTJ resistance vs. applied current (Fig. 2). Each resistance is a weight controlled by an input current. We see at least 50 Ω between each weight, large enough to distinguish between weights. We will show results on integrating 3T-MTJ synapses and neurons, where firing of the neuron sets the synapse at a given weight. We believe this is an important step forward in building full neuromorphic computers using magnetic materials. While notches are not favorable for scaling, the functionality shown can implemented in other ways, e.g. through voltage-controlled DW traps[7].

[1] S. Lequeux, J. Sampaio, V. Cros, et al. Sci Rep 6, 31510 (2016). [2] J. Torrejon, M. Riou, F. A. Araujo, et al. Nature 547, 428-431 (2017). [3] A. Vansteenkiste, J. Leliaert, M. Dvornik, et al. AIP Adv. 4, 107133 (2014). [4] J. A. Currivan-Incorvia, S. Siddiqui, S. Dutta, et al. Nat. Commun. 7, 10275 (2016). [5] N. Hassan, X. Hu, L. Jiang-wei, et al. Submitted. [6] Q. Dong, K. Yang, L. Fick, et al. IEEE Int. Symp. on Circuits and Systems, 1–4 (2017). [7] U. Bauer, S. Emori, & G. S. D. Beach. Nat. Nanotechnol. 8, 411–416 (2013).

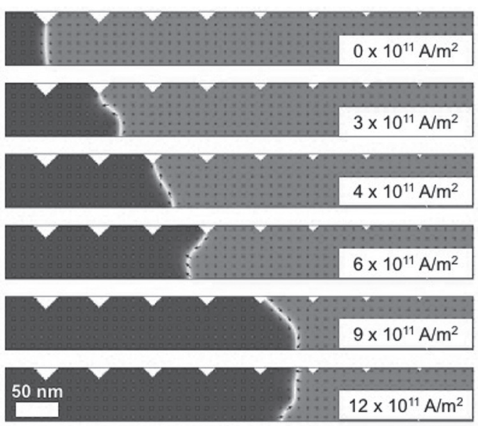
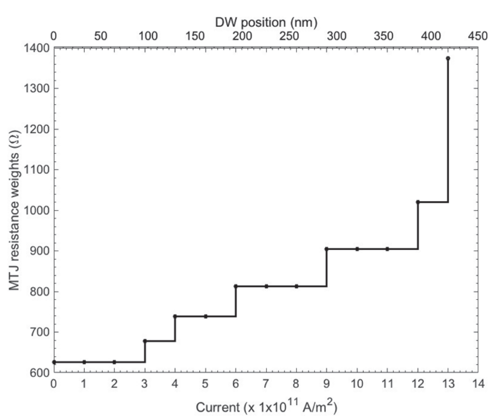


Fig. 1. Micromagnetic images showing domain wall position vs. current.



Analog synapse weights vs. current.

8:54

CC-03. Neuromorphic Computing with Domain Wall-Based Three-Terminal Magnetic Tunnel Junctions: Neurons. *N. Hassan*[1], X. Hu[1], L. Jiang-Wei[2], W.H. Brigner[1], O.G. Akinola[3], F. Garcia-Sanchez[4], M. Pasquale[4], C.H. Bennett[5], J.C. Incorvia[3] and J.S. Friedman[1] *1. Electrical & Computer Engineering, The University of Texas at Dallas, Richardson, TX, United States; 2. Computer Science, The University of Texas at Dallas, Richardson, TX, United States; 3. Electrical & Computer Engineering, The University of Texas at Austin, Austin, TX, United States; 4. Istituto Nazionale di Ricerca Metrologica, Torino, Italy; 5. Centre de Nanosciences et de Nanotechnologies, Université Paris-Saclay, Orsay, France*

The core building blocks of neuromorphic computing systems are neurons and synapses, and it is critical that these bio-inspired device components can be fabricated with compatible material structures. As domain wall (DW)-based three-terminal magnetic tunnel junctions (3T-MTJs) [1] also realize synapse behavior [2], this work proposes a 3T-MTJ artificial neuron [3] that enables the development of an integrated neuromorphic computing system composed solely of 3T-MTJ devices. The proposed spintronic leaky integrate-and-fire (LIF) [4] neuron manipulates the DW position to perform the leaking, integration, and firing functions, while also providing lateral inhibition. Lateral inhibition [5] is critical to the capability of biological systems to prevent neighboring neurons from firing simultaneously, but previous artificial neuron proposals based on emerging technologies require the assistance of external CMOS circuits to provide this lateral inhibition capability [6]–[8]. By exploiting the stray magnetic fields, the proposed 3T-MTJ neuron [3] eliminates the need for CMOS circuitry and intrinsically provides the leaking, integrating, firing, and lateral inhibition capabilities. Input currents applied to the neurons enable integration behavior by pushing the DWs through spin-transfer or spin-orbit torque. The leaking is performed by a hard ferromagnet under the 3T-MTJ neuron tracks that creates a magnetic field to constantly push the neuron DWs opposite the direction of integration. Firing occurs when the DW crosses below the MTJ hard layer, switching the MTJ from the anti-parallel to the parallel state and enabling a large output current. Finally, analog lateral inhibition is achieved by dipolar fields from each neuron that attempt to orient neighboring neurons antiparallel by repulsive coupling. An integrating neuron thus pushes slower neighboring neurons' DWs in the direction opposite of integration. Applying this lateral inhibition to a ten-neuron output layer within a neuromorphic crossbar structure enables the identification of handwritten digits with a 94% success rate [3].

[1] J.A. Currivan-Incorvia, S. Siddiqui, S. Dutta, *et al.*, *Nat. Commun.*, Vol. 7, p. 10275 (2016). [2] O. G. Akinola, E. J. Kim, N. Hassan, *et al.*, submitted to *2019 Joint MMM-INTERMAG.* [3] N. Hassan, X. Hu, L. Jiang-Wei, *et al.*, *J. Appl. Phys.* (under review). [4] A. N. Burkitt, *Biol. Cybern.*, Vol. 95, pp. 97–112 (2006). [5] E. Meir, G. Von Dassow, E. Munro, G. M. Odell, *Curr. Biol.*, Vol. 12, pp. 778–786 (2002). [6] A. Jaiswal, S. Roy, G. Srinivasan, K. Roy, *IEEE Trans. Electron Devices*, Vol. 64, pp. 1818–1824 (2017). [7] A. Jaiswal, A. Agrawal, P. Panda, K. Roy, *arXiv*:1705.06942 (2017). [8] A. Sengupta, P. Panda, P. Wijesinghe, *et al.*, *Sci. Rep.*, Vol 6, p. 30039 (2016).

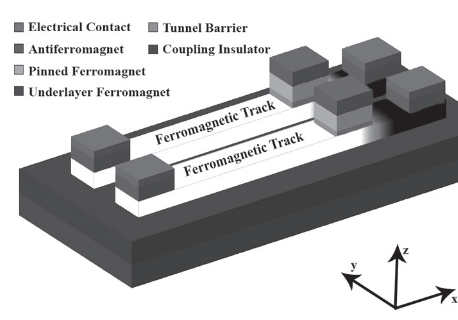


Fig. 1. 3T-MTJ neuron structure with two neurons above a shared ferromagnet.

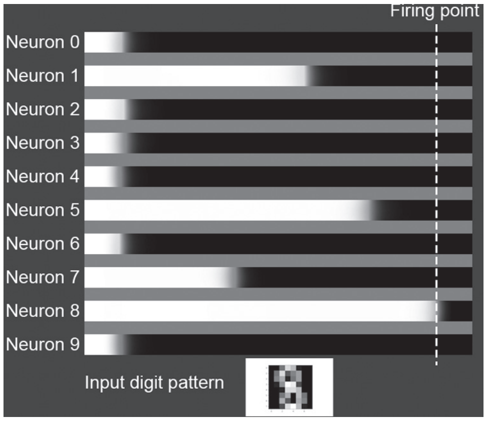


Fig. 2. Recognition of the digit "8" by ten-neuron output layer.

9:06

CC-04. Implementation of on-chip learning for domain wall and skyrmion based feedforward neural networks using transistor based feedback circuitry that executes back-propagation algorithm.

A. Dankar[1], A. Verma[1], D. Kaushik[1], U. Saxena[1], S. Chatterjee[1] and *D. Bhowmik*[1] *1. Deaprtment of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India*

Spintronic devices have been proposed as synapses in hardware Artificial Neural Networks (ANN)[1-4]. However most reports[2,3] only show simulation of "off-chip" learning i.e. ANN is trained on traditional computer first to obtain synaptic weights and then current pulses are applied to "write" those weights on spintronic synapses of its hardware equivalent. Thus advantage of hardware ANN is used only partially. Here we perform micromagnetic simulation on "mumax3" and circuit simulation on Cadence Virtuso to implement "on-chip" learning for spintronic ANN (Fig. 1a,2a). Domain Wall (DW) and Skyrmion (Sk) based synapses as described in ref. 4 are chosen as synapses owing to their nonvolatility. Fig.1b,c show current controlled conductance characteristics of the DW and Sk synapses. Smaller magnitude of current pulses with longer duration is used to move Sk compared to DW because defects pin DW but not Sk[4]. Neuron and backpropagation[5] caclulation circuitry are implemented by transistors and operational amplifiers due to their suitability in analog computing. We train the ANN on images of hand written digits from MNIST dataset[6]. Input voltages proportional to image pixels generate "read current"-s (Fig. 2b) at output nodes corresponding to digits ('0'-'9'), which pass through transistor based neuron circuit that perform tan-sigmoid function *(f)* and operational amplifier based back-propagation circuitry *(B)* (Fig. 1a, 2a) to generate "write current"-s (Fig. 2c) that in turn move DW/Sk at synaptic devices to adjust their weights. This process repeated over 100 epochs, with 100 samples repeated over each, trains the ANN. After that for each sample/image of digit "read current" at output node corresponding to that digit is positive and at all other output nodes it is negative (Fig. 2d) showing that ANN is trained.

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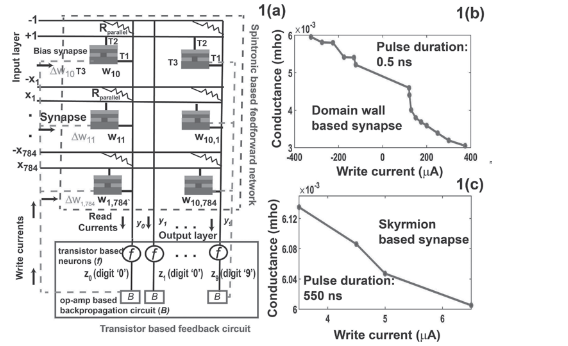

Fig 1.a) Simulated ANN- with domain wall (DW) or skyrmionic (Sk) synapses. b,c) synaptc characteristic of DW and Sk synapse

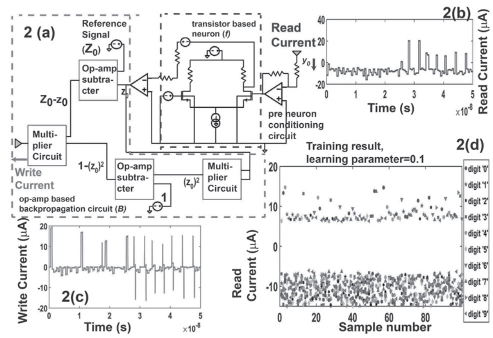

Fig 2. a) Neuron *(f)* and backpropagation *(B)* circuitry for each output node. b)Read current at output node for digit '0' for first epoch in DW synapse based ANN c) Write current going to bias synapse connected to same output node d) Read current at output nodes for 10 digits for the 100th epoch

9:18

CC-05. Neural-like computing with stochastic magnetic tunnel junctions. *A. Mizrahi*[1,2], T. Hirtzlin[3], A. Fukushima[4], H. Kubota[4], S. Yuasa[4], M. Stiles[5], J. Grollier[1] and D. Querlioz[3] *1. CNRS / Thales, Palaiseau, France; 2. NIST / University of Maryland, Gaithersburg, MD, United States; 3. Centre de Nanosciences et Nanotechnologies, Orsay, France; 4. National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan; 5. NIST, Gaithersburg, MD, United States*

Maintaining the stability of magnetic tunnel junctions at the nanometer scale is a challenge: junctions with low energy barrier switch stochastically between their two states driven by thermal noise. We draw inspiration from the brain for how to compute with stochastic devices because the brain operates at low power even though its neurons exhibit stochastic behavior. Sensory neurons emit voltage spikes of fixed amplitude but at time intervals that appear stochastic. One computing paradigm from neuroscience is population coding, in which information is carried by the spike rates of a population of neurons [1]. The non-linear relationship between the stimulus received by a neuron and its rate is called a tuning curve. The set of tuning curves for the population constitute a basis set of functions; simple linear combinations of them can construct non-linear transformations. We show that stochastic magnetic tunnel junctions can emulate spiking neurons [2]. Their stochastic transitions are reminiscent of the stochastic spikes of sensory neurons. Furthermore, their transition rate can be controlled by application of a dc current through the device giving a non-linear tuning curve. We experimentally show that linear combinations of the tuning curves of nine stochastic magnetic tunnel junctions can construct non-linear transformations. With simulations, we show how a network of two populations, interconnected by synaptic weights, can learn non-linear transformations with a simple learning rule. Equipping the system with continuous learning enables it to overcome the failure of neurons as well as the loss of synaptic