Hybrid Pass Transistor Logic With Ambipolar Transistors

Xuan Hu, *Graduate Student Member, IEEE*, Amy S. Abraham, Jean Anne C. Incorvia, *Member, IEEE*, and Joseph S. Friedman, *Senior Member, IEEE*

***Abstract*— The pass transistor logic (PTL) family enables compact circuits to reduce area and power consumption, but inter-stage inverters are required for signal integrity and complementary signals. Similarly, dual-gate ambipolar field-effect transistors are exceptionally logically expressive and provide a single-transistor XNOR operation, but numerous inverters are required to provide complementary signals. In both cases, these inverters and complementary signals significantly degrade overall system efficiency. Ambipolar field-effect transistors are a natural match for PTL, and we therefore propose a new hybrid ambipolar-PTL logic family that exploits the compact logic of PTL and the ambipolar capabilities of ambipolar field-effect transistors. This logic family is a hybrid between PTL and static CMOS-like logic that is made efficient by the use of ambipolar transistors. Novel hybrid ambipolar-PTL circuits were designed and simulated in SPICE, demonstrating strong signal integrity along with the efficiency advantages of using the required inverters to simultaneously satisfy the requirements of PTL and ambipolar circuits. In comparison to the ambipolar field-effect transistors in the conventional static CMOS logic structure, the proposed ambipolar-PTL family can reduce propagation delay by 33%, energy consumption by 88%, energy-delay product by a factor of 10, and area-energy-delay product by a factor greater than 20.**

***Index Terms*— Ambipolarity, transmission gate logic, pass transistor logic (PTL), carbon nanotube, ambipolar logic.**

I. Introduction

As TECHNOLOGY scaling becomes increasingly challenging and expensive, novel device switching phenomena have the potential to revolutionize computing beyond conventional unipolar field-effect transistors (FETs) with a fixed charge polarity [1]–[6]. In particular, dual-gate ambipolar FETs (DG-A-FETs) enable efficient computing through dynamic switching between *n*- and *p*-type [7]–[16]. Such DG-A-FETs can be implemented with a variety of materials that exhibit ambipolar transport, including carbon nanotubes (CNTs), silicon nanowires, graphene nanoribbons, and transition metal dichalcogenides [17]–[23]. Though this paper considers circuits designed with DG-A-FETs with CNTs (DG-A-CNTFETs) due to the existence of an effective SPICE-compatible device model, the general conclusions are expected to also apply to DG-A-FETs based on other ambipolar materials.

Manuscript received July 10, 2020; revised October 1, 2020; accepted October 23, 2020. Date of publication November 9, 2020; date of current version December 21, 2020. This article was recommended by Associate Editor J. Di. *(Corresponding author: Joseph S. Friedman.)*

Xuan Hu, Amy S. Abraham, and Joseph S. Friedman are with the Department of Electrical and Computer Engineering, The University of Texas at Dallas, Richardson, TX 75080 USA (e-mail: joseph.friedman@utdallas.edu).

Jean Anne C. Incorvia is with the Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712 USA.

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2020.3034042

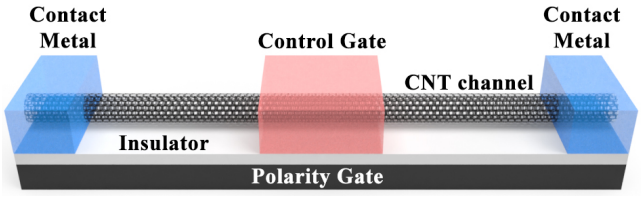

Fig. 1. Cross-section of a DG-A-FET with an ambipolar CNT channel.

In the device of Fig. 1, the polarity gate (PG) voltage in a DG-A-FET can be used to determine the dominant carrier polarity while the control gate (CG) voltage modulates the current. Ambipolar transistors have been used in circuits based on the conventional complementary pull-up and pull-down logic family (commonly referred to as the static CMOS logic family, which also connotes MOSFET devices), enabling increased logical expressivity in compact circuits [24], [25]. In particular, the conventional complementary pull-up and pull-down logic family enables XOR and XNOR gates with only four transistors. However, these gates require complementary input signals, necessitating the use of a two-transistor inverter for each input. These additional inverters significantly increase the area and energy consumption, thereby reducing the benefits of using ambipolar transistors. To fully leverage the ambipolar transport, it is critical to replace the complementary pull-up and pull-down circuit structure with an alternative structure better-suited to ambipolar transistors.

Pass transistor logic (PTL) is a well-established logic family that is designed to reduce the energy and area of logical computing systems by reducing the number of transistors required to perform logical functions [26]–[28]. However, the series resistance of the transistors degrades the signal integrity in cascaded pass transistor chains. Therefore, the broad application of PTL in large-scale circuits is limited by the need for inverters to provide the external power required for signal integrity [29]. Without inverters that restore the full output swing, the signal amplitude diminishes and eventually becomes insufficient to drive cascaded logic gates.

PTL-based logic gates using A-FETs have previously been considered, but a complete logic family using A-FETs in a PTL-based structure has never been proposed or evaluated. Examples of previous PTL-based A-FET logic gates include a transmission gate [24] and a 4:1 multiplexer [30]. While these logic gates are intriguing, it is unclear from these previous works how to efficiently scale to large circuits. Of particular interest, [31] proposes various three- and

five-input logic gates that enable efficient logic synthesis, but the lack of an electrical analysis and methodology for cascading and inverter insertion limits its utility. In this paper, we therefore propose and electrically evaluate multiple complete circuit design methodologies that provide a scalable and efficient approach for the design of large A-FET circuits and systems.

As both the PTL family and the DG-A-FET-based complementary pull-up and pull-down logic [24], [25] require additional inverters for proper operation, this paper proposes a hybrid ambipolar-PTL (hybrid A-PTL) family that simultaneously uses the inverters to satisfy the requirements for both PTL and DG-A-FET-based circuits. As the inverters provide both complementary signals and external power for signal integrity, their dual-purpose use makes PTL extremely well-suited for use with DG-A-FETs in compact and efficient logic circuits. This paper therefore describes the A-PTL family and explores the A-PTL design space to propose and analyze three A-PTL structures with distinct trade-offs in terms of area, speed, and energy. These A-PTL variants are shown to provide propagation delay reduction of up to 33% and energy savings of up to 88% in comparison to the conventional CMOS-like logic family with the same A-FETs, leading to a 10x reduction in EDP and greater than 20x reduction in area-energy-delay product (AEDP).

II. Background

In order to appreciate the potential benefits of using DG-A-FETs within the PTL family for large-scale computing systems, it is important to understand the potential and unique characteristics of these unconventional devices and of the PTL family.

A. Dual-Gate Ambipolar Carbon Nanotube Field-Effect Transistor

Although the high current density and tunable bandgap of low-dimensional materials such as CNTs have attracted significant attention, the presence of ambipolar transport has impeded attempts to use them to replace Si in unipolar FETs. Specifically, when using CNTs in implementing unipolar FETs, the ambipolarity of intrinsic CNT is generally considered as a drawback since the ambipolarity impedes the optimization of such unipolar CNTFETs [16]. Compared to doped CNTs, the ambipolarity of intrinsic CNTs results in higher leakage in the subthreshold region and therefore degrades the ON/OFF ratio. Furthermore, the band-to-band tunneling caused by the ambipolarity may lead to incorrect device functionality. However, this ambipolarity creates new opportunities for circuit design, as DG-A-FETs can be dynamically switched between *n*-type and *p*-type polarity.

In the device of Fig. 1, the PG voltage determines the channel polarity while the CG voltage modulates current flow through the channel. The A-FET has high conductivity when the voltages applied to the dual gates are both high or low. In particular, a low voltage applied to the polarity gate causes the device to act as *p*-type such that a low voltage applied to the control gate turns the device ON (CG = 0 & PG = 0); a high voltage at the polarity gate causes the device to act as *n*-type and the device is ON when the control gate voltage is also high (CG = 1 & PG = 1). In the two other cases (CG = 1 & PG = 0 or CG = 0 & PG = 1), the A-FET is in a high-resistivity OFF state.

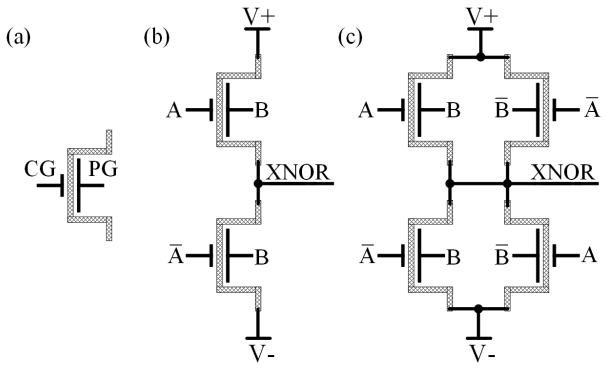

Fig. 2. Transistor-level schematic of XNOR gate with (a) single transistor, (b) two transistors, and (c) four transistors.

This ability to switch the transistor between electron and hole conduction by the dual independent gate control allows the transistor to have more expressive power, reducing the number of devices required to perform logical operations [24]. The four input combinations listed above enable a single A-FET to implement the XNOR function, where the voltage applied to the CG and PG are the two inputs and the resistance between source/drain contacts represents the output state of the signle-transistor XNOR gate. This native ability to provide a single-transistor XNOR operation enables high-efficiency logical and neuromorphic computing systems [24], [32].

B. Complementary Ambipolar Field-Effect Transistor Logic

When DG-A-FETs are used to implement logic circuits within a conventional complementary pull-up and pull-down logic structure, as in [24], transistor pairs with complementary inputs are used in the pull-up and pull-down networks to prevent V_T-drops [10]. For example, although a single DG-A-FET is able to implement the XNOR function [Fig. 2(a)], the output states are resistances rather than voltages. If two A-FETs are used as in Fig. 2(b), an XNOR gate can be realized with a voltage output [33]. However, in this case, both transistors will always be either *n*-type or *p*-type, and the output will have reduced voltage swing - between $|V_{thp}|$ and $V_{DD} - V_{thn}$ rather than V− and V+ due to the threshold voltage drops. To ensure signal integrity and fan-out, four DG-A-FETs are used as in Fig. 2(c).

The requirement of the complementary transistor pair significantly increases the device count and hence the area cost and power consumption. Furthermore, each transistor pair requires its input signal to be provided in a complementary form (both A, B, and their complements are needed for A XNOR B). Whereas this is the case for the XOR and XNOR functions with conventional CMOS, these complementary signals are required for all DG-A-FET logic functions with the complementary pull-up and pull-down structure. Therefore, the overhead circuits and interconnects required to generate the complementary signals further reduce the benefits derived from utilizing transistor ambipolarity.

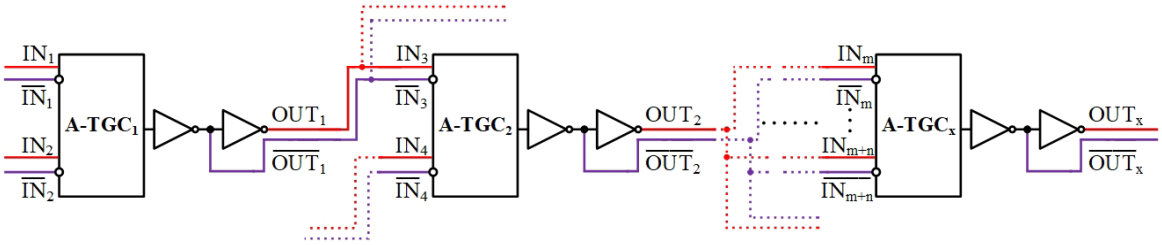

Fig. 3. Block diagram of the Type I hybrid A-PTL architecture illustrating the alternation between A-TGCs and buffering inverters.

Compared to conventional CMOS logic with unipolar transistors, DG-A-FETs within a conventional complementary pull-up and pull-down logic structure implement complex logic functions with higher logical expressivity. However, both the extra transistors used for ambipolar TG pairs and the inverters required for generating complementary signals decrease the efficiency of using A-FETs in the conventional CMOS logic architecture. It is therefore worthwhile to explore other logic styles that are well-suited to logic with DG-A-FETs.

C. Pass Transistor Logic

PTL is a logic family designed to minimize the number of transistors required to implement any given logic function, thereby reducing area and power consumption. Unlike the capacitive loads in conventional static CMOS logic that do not incur a voltage drop, PTL gates exhibit resistive loads that result in a voltage drop through each gate. Therefore, whereas conventional static CMOS logic gates can be cascaded indefinitely with energy supplied by built-in supply voltage rails, PTL requires the insertion of additional inverters to supply the energy necessary to maintain proper voltage levels within long chains of cascaded PTL logic gates [26], [34]. A large system based heavily on PTL must therefore be hybridized with the complementary pull-up and pull-down inverters of conventional static CMOS.

Furthermore, as traditional PTL uses only NMOS transistors, there is a threshold voltage drop whenever a high voltage signal is transmitted; an additional PMOS transistor is therefore frequently added to provide a full voltage swing using TGs in complementary PTL (CPL), which further necessitates inverters to provide each logical input signal in its complementary form. This heavy use of inverters and the need to use complementary transistors drastically increases the device count, delay, and energy consumption of PTL circuits, inhibiting the development of computing systems based entirely on PTL.

PTL and CPL are therefore often used for specific logic functions within systems based primarily on the conventional complementary pull-up and pull-down logic structure. For example, multiplexing is particularly efficient with PTL, and PTL multiplexers are therefore frequently found within an otherwise conventional CMOS logic architecture. In that vein, previous work has proposed PTL and CPL multiplexers with DG-A-CNTFETs [30] as well as a PTL full adder with ambipolar silicon nanowire FETs [35]. These logic circuits, however, face the same challenges that have plagued other A-FET based logic gates and PTL: complementary input signals are required for functionality, requiring the heavy use of additional inverters. The area and energy costs of these inverters drastically decrease the efficiency, limiting the use of such circuits to particular logic functions within systems based primarily on the conventional complementary pull-up and pull-down logic structure. While previous DG-A-FET and PTL/CPL circuits are efficient for particular individual functions, novel approaches are required to enable a scalable logic family.

III. Hybrid Ambipolar Pass Transistor Logic

The challenges facing both PTL and DG-A-FETs can be resolved by incorporating DG-A-FETs into a hybrid A-PTL family that can be scaled to large circuits and systems by linking PTL to the conventional complementary pull-up and pull-down logic structure. A-FETs need complementary transistor pairs for rail-to-rail voltage swing, necessitating the use of inverters to generate complementary signals, while both CPL and PTL need inverters to maintain signal integrity despite degradation through the resistive signal path. Therefore, in the proposed hybrid A-PTL family, the inverters required for complementary inputs and signal integrity simultaneously satisfy the needs of both DG-A-FETs and PTL, thereby amortizing the costs of these inverters across the benefits provided by both DG-A-FETs and PTL. Various hybrid A-PTL circuit styles are optimized for particular figures of merit, providing distinct advantages in large-scale circuits implemented entirely with hybrid A-PTL.

A. Basic Hybrid A-PTL Structure (Type I)

As illustrated in Fig. 3, the core concept of the proposed hybrid A-PTL family is the alternation between PTL-based computational circuits and buffering inverters, thus creating a hybrid between the PTL and conventional pull-up and pull-down logic families. The entire system is composed solely of DG-A-FETs, with CPL-based computations performed by ambipolar transmission gate cores (A-TGCs) followed by two CMOS-style DG-A-FET inverters. The A-TGC performs logical operations based on the input data, and is succeeded by two inverters that ensure signal integrity and provide the complementary output signals for cascading stages. These buffering inverters provide energy from the power supply (rather than from the input as in PTL), thereby boosting the fan-out and enabling large cascaded circuits without signal degradation. Furthermore, using DG-A-FETs to reduce the number of transistors in the PTL-style logic circuits reduces area, delay, and energy in comparison to PTL.

An example hybrid A-PTL circuit is illustrated in the schematic of Fig. 4, which will henceforth be referred to as the

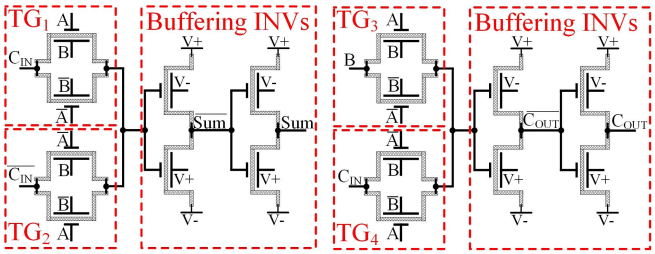

Fig. 4. Transistor-level schematic of the Type I hybrid-A-PTL one-bit full adder.

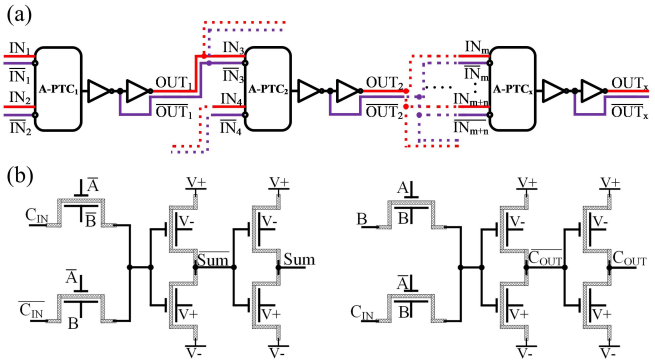

Fig. 5. (a) Block diagram of the Type II hybrid A-PTL style. (b) Transistor-level schematic of a Type II hybrid-A-PTL one-bit full adder, showing A-TGCs replaced by A-PTCs.

Type I cascading style. This one-bit requires eight transistors in the A-TGC and an additional eight transistors in the four inverters, for a total of 16. In comparison to the 28 DG-A-FETs required for a one-bit full adder in the conventional CMOS architecture [10], this represents a 43% reduction in area. Furthermore, as demonstrated in the simulations of section IV, this hybrid A-PTL full adder structure exhibits significant reductions in delay and energy consumption.

B. Alternative Hybrid A-PTL Structures (Types II & III)

Beyond the proposed Type I hybrid A-PTL style, the transistor count can be minimized further by reducing complementarity in either the A-TGC or buffering inverters. These two alternative logic styles make the following modifications:

- Type II: one transistor is removed from each TG pair within the A-TGC.
- Type III: one buffering inverter is removed following each A-TGC.

Each of these modifications directly causes a significant decrease in the circuit area, while also drastically impacting energy consumption and delay.

The Type II style is illustrated in Fig. 5, with each TG pair in the A-TGC replaced by an ambipolar pass transistor core (A-PTC) with a single pass transistor to reduce device count. As a single pass transistor cannot always provide a full voltage swing, the logical complexity of the Type II A-PTL is limited by the DG-A-FET threshold voltage drops from propagating a '1' ('0') when the DG-A-FET has an *n*-type (*p*-type) channel. As demonstrated in section IV, the area reduction in this Type II structure therefore comes at the cost of increased delay, limiting its overall efficiency.

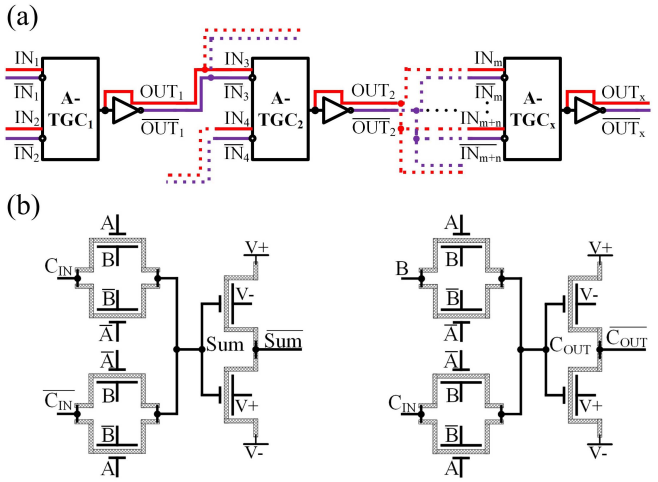

Fig. 6. (a) Block diagram of the Type III hybrid A-PTL architecture showing the direct cascading of the non-inverted output without a buffering inverter. (b) Transistor-level schematic of a Type III hybrid-A-PTL one-bit full adder with only one inverter following each A-TGC.

TABLE I
ONE-BIT FULL ADDER AREA COMPARISON WITH HYBRID A-PTL

Architecture	Device Count	Estimated Area Reduction
CMOS-like	28	baseline
Type I	16	43%
Type II	12	57%
Type III	12	57%

The Type III structure shown in Fig. 6 uses the same A-TGC structure as Type I, but one buffering inverter is removed. Therefore, the non-inverted output signals (*Sum* and C_{OUT} in the full adder) drive cascaded stages directly, without passing through a buffering inverter. Like conventional CPL, this may prevent long chains of cascaded circuits because the energy of the entire CPL block comes from the initial input signals. Whereas the Type II style compromises signal integrity by having an asymmetric signal swing at the output of the A-PTC, the Type III style has reduced signal integrity due to the lack of isolation/buffering inverters between the input and output. As demonstrated in section IV, the removal of an inverter from the critical path gives the Type III style the lowest delays for circuits without high fan-out.

Table I summarizes the transistor count of one-bit full adders in each of the three styles. Compared to the CMOS-like one-bit full adder baseline [10], the proposed Type I style reduces the area by 43%, while Types II and III reduce the area by 57%. The reduced circuit symmetry with both Types II and III decreases the output slew rate, increasing the delay. However, this is compensating to varying degrees by reductions in the parasitic capacitances and, for Type III, the removal of an inverter from the critical path.

IV. COMPUTATIONAL PERFORMANCE & EFFICIENCY

To evaluate the performance and efficiency of the proposed hybrid A-PTL styles, SPICE simulations have been performed to compare the various styles to the baseline conventional complementary pull-up and pull-down structure [10].

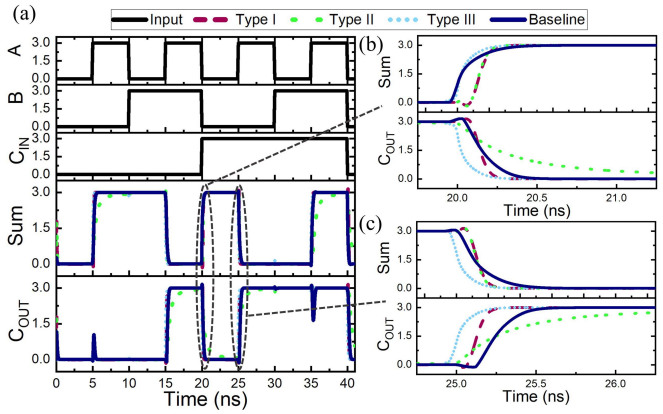

Fig. 7. Transient waveforms of the A-PTL one-bit full adders with CG cascading where (a) shows all input combinations while (b) and (c) show zoomed-in transitions of rising and falling edges.

While ambipolarity has been demonstrated in numerous materials including silicon nanowires, WSe_2, and graphene nanoribbons, the DG-A-CNTFET has been chosen for this analysis due its prior experimental demonstration and the availability of a SPICE-compatible device model [7]–[10]. In all of the simulations in this paper, the intrinsic gate-to-electrode parasitic capacitance ($C_{CG-S}, C_{CG-D}, C_{PG-S}, C_{PG-D}$) are 5 fF while the load capacitance C_{LOAD} at each output node is 10 fF. The SPICE simulations of one-bit and four-bit full adders demonstrate that the choice between CG and PG cascading engenders a trade-off between delay and energy consumption. Overall, the Type III style is shown to be superior, with delay reduced by up to 33%, energy reduced by a factor of eight, and AEDP reduced by a factor greater than 20.

A. Comparison of One-Bit Full Adders

Fig. 7 shows the transient simulation waveforms of one-bit full adder circuits in the three hybrid A-PTL styles. To provide a reference that enables apples-to-apples comparisons of the circuit structures, the conventional static CMOS-like 28-transistor one-bit full adder of [10] servers as a baseline. As shown in Figs. 4-6, the output of the A-TGC or A-PTC is fed to the CGs of the DG-A-FETs in the buffering inverters; the PGs of the DG-A-FETs in the inverters are connected to power supplies for DC biasing. Figs. 7(b) and (c) zoom in on transitions of both the *Sum* and C_{OUT} output signals. These simulations clearly reveal that the Type I and III styles provides the shortest delays, significantly faster than the baseline. The Type II styles has varying delays in each case, though the Type II style is clearly quite slow for computing C_{OUT}.

B. Control Gate Vs. Polarity Gate Cascading

In all of the circuits that have thus far been discussed, the output of the A-TGC or A-PTC has been fed to the CGs of the DG-A-FETs within the inverters. With this CG cascading, the polarity of each DG-A-FET within the inverters is constant. Alternatively, this signal could be used to drive the PGs within the inverter DG-A-FETs, as shown in Fig. 8, thus broadening the design space. In the case of PG cascading, the the polarity of the DG-A-FETs within the inverters is modulated by the outputs of the A-TGC or A-PTC while the CG input remains constant.

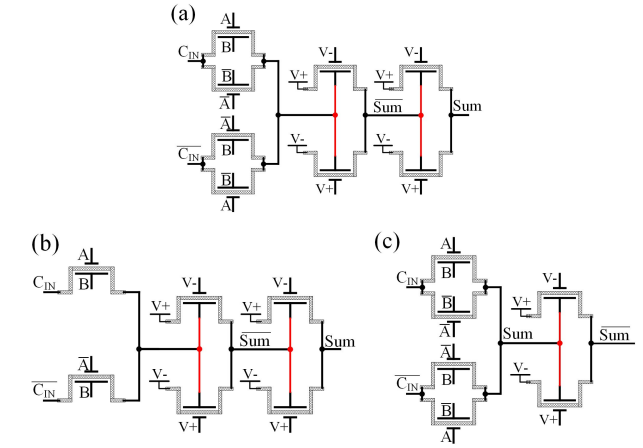

Fig. 8. *Sum* circuit schematic with PG cascading in (a) Type I, (b) Type II, and (c) Type III hybrid A-PTL styles.

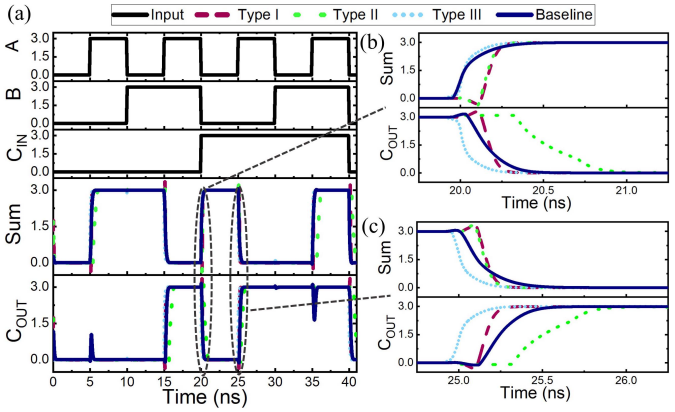

Fig. 9. Transient waveforms of the A-PTL one-bit full adders with PG cascading where (a) shows all input combinations while (b) and (c) show zoomed-in transitions of rising and falling edges.

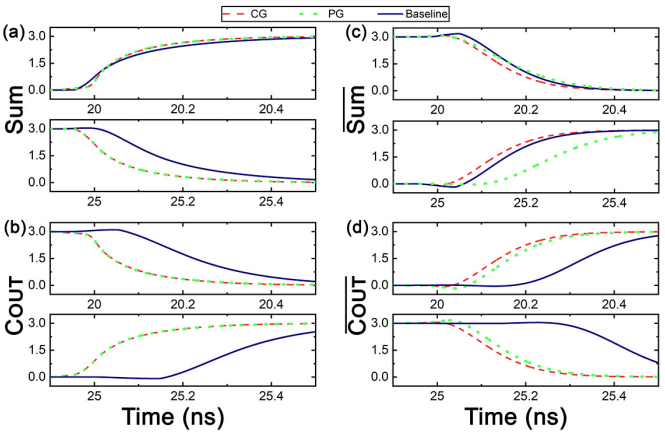

Fig. 10. Transient switching waveforms of the Type III hybrid A-PTL one-bit full adder with CG cascading (dashed lines) and PG cascading (dotted lines) for: (a) *Sum*; (b) C_{OUT}; (c) $\overline{Sum}$; (d) $\overline{C_{OUT}}$.

Fig. 9(a) shows the transient simulation waveforms of one-bit full adder circuits with PG cascading in the three hybrid A-PTL styles, with a focus on the switching at selected edges in Figs. 9(b) and (c). Similar to the simulations with CG cascading in Fig. 7, these simulations show that the Type III

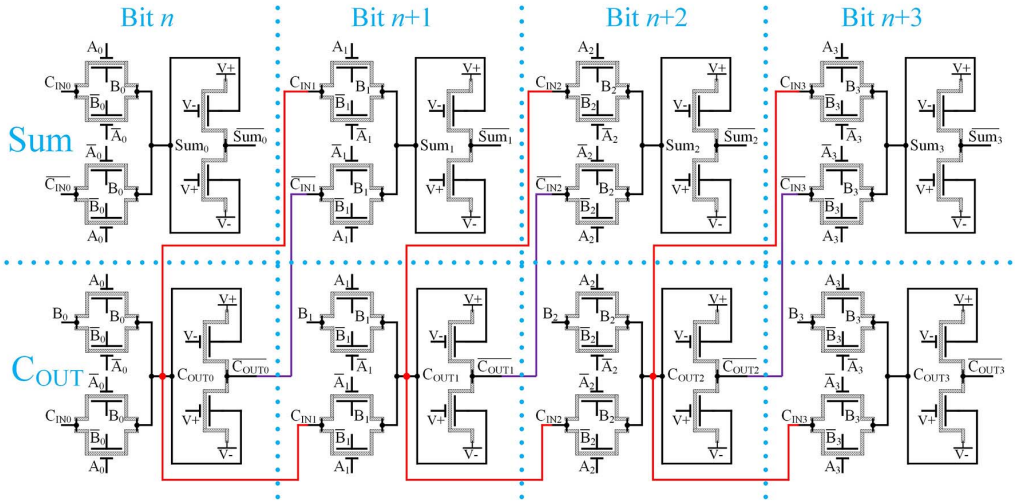

Fig. 11. Transistor-level schematic of the hybrid A-PTL four-bit ripple-carry adder using the Type III style and PG cascading.

style exhibits the shortest delay, while the relative delays of the Type I and II styles vary.

To directly compare CG and PG cascading, the transient waveforms with both CG and PG cascading are plotted together for the Type III hybrid A-PTL full adder in Fig. 10. As the non-inverted *Sum* and C_{OUT} signals have not passed through an inverter, there is no difference between CG and PG cascading. For the inverted output signals, this comparison clearly shows that CG cascading provides shorter delay than PG cascading due to an earlier transition. However, as can be seen in Fig. 10, the rise and fall times for CG cascading are longer than for PG cascading, even though the delay for CG cascading is lower for some input combinations. This longer rise time - that is, slower slew rate - for CG results in a longer time period with short-circuit current between the inverter supply rails, and therefore higher energy consumption. Therefore, the higher output slew rate of PG cascading results in a lower total energy consumption by reducing the cumulative short-circuit current in the inverters.

C. Medium-Scale Circuit Analysis

To enable analysis more predictive of a large-scale system, four-bit hybrid A-PTL ripple-carry adders have been simulated with all three styles and both cascading approaches, for a total of six distinct circuits. As an example, the four-bit hybrid A-PTL ripple-carry adder using the Type III style with PG cascading is shown in Fig. 11. Each one-bit full adder output signal $C_{OUT-(i)}$ is fed into the carry-in input port $C_{IN-(i+1)}$ of the next one-bit full adder through the drain/source of input A-FETs. This circuit thus includes various combinations of cascading to capacitive (CG & PG) and resistive (drain & source) input ports. To broadly characterize the behavior across input combinations, a sequence of 1,000 operations was randomly generated and used as input signals.

A selection of the transient simulation waveforms is shown in Fig. 12. This four-bit full adder circuit has an additional carry-in bit such that it is composed of four one-bit full adders rather than three one-bit full adders and a half adder. As can be seen in the figure, the missing inverter from the Type III style leads to a propagation delay dependent on the input combination.

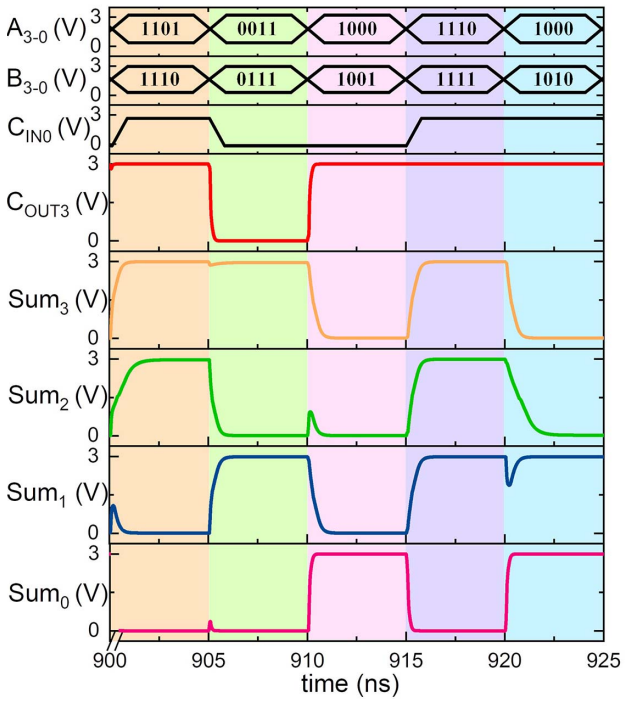

Fig. 12. Selected simulation waveforms of the Type III hybrid A-PTL four-bit ripple-carry adder with PG cascading.

D. Discussion

The performance and efficiency of all three hybrid A-PTL styles and both cascading approaches are analyzed in Fig. 13 based on the results for the four-bit full adder circuits. These results are compared to the conventional CMOS-style DG-A-FET circuit as a baseline in terms of maximum delay, average energy consumption, EDP, and AEDP across the 1,000 input combinations. As can clearly be observed in the figure, the Type III hybrid A-PTL style is superior to the conventional baseline structure for all metrics.

The asymmetry between the CG and PG of the DG-A-FET devices leads to a trade-off between speed and energy consumption. The minimum, average, and maximum delays for each of the six cascading approaches are shown in Fig. 14. For all three hybrid A-PTL styles, CG cascading is always faster

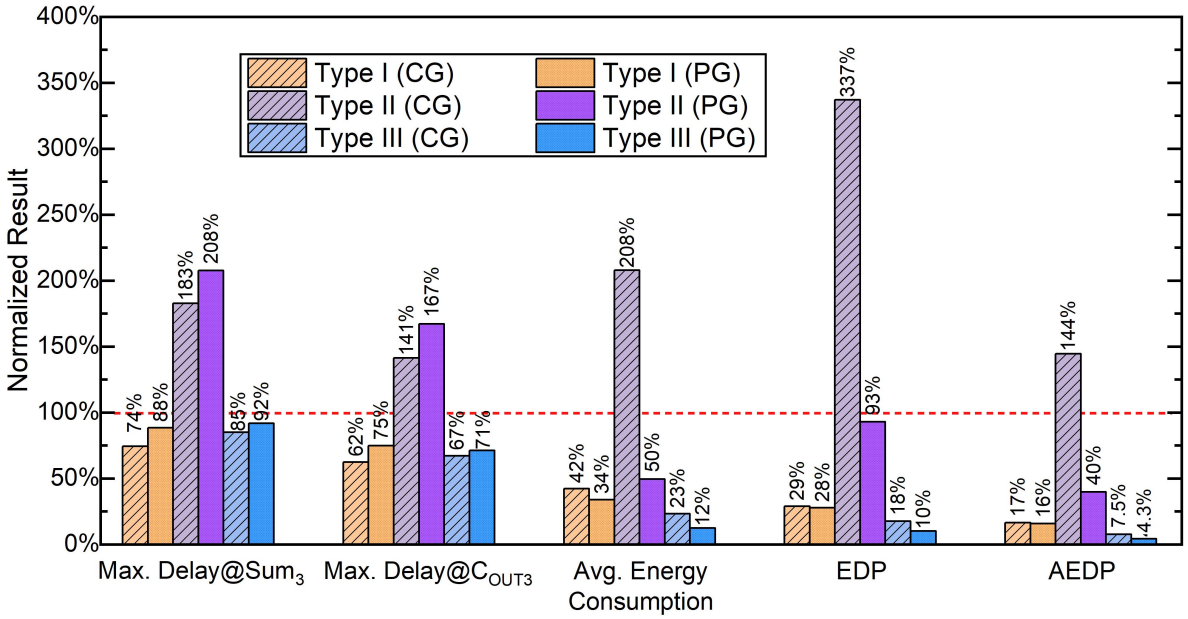

Fig. 13. Performance and efficiency comparison of the proposed hybrid A-PTL styles to the conventional CMOS-style baseline. These results are based on simulations of the four cascaded full adders.

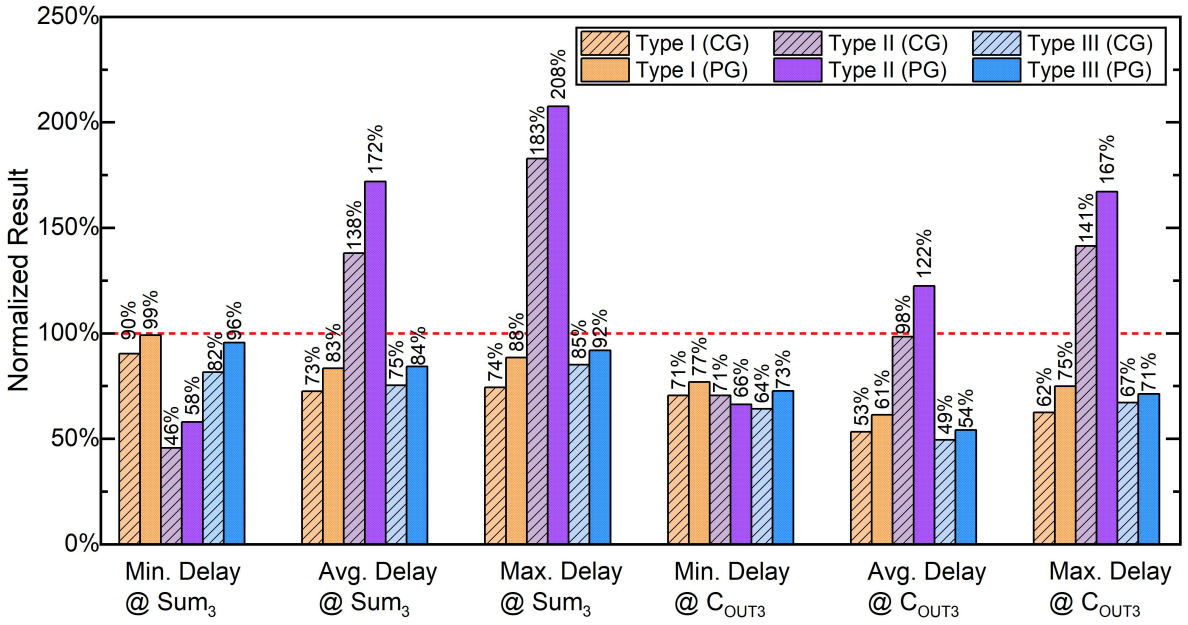

Fig. 14. Minimum, average, and maximum delay of each circuit structure normalized to the baseline of the conventional static CMOS-style simulation results.

than PG cascading; however, the circuits with PG cascading consume less energy and therefore result in a lower EDP and AEDP. Therefore, CG cascading is preferred when speed is critical, while PG cascading is more suitable to low-power system design.

While the delay of the Type I and III styles can be significantly less than the baseline, the type II style is significantly slower. The Type I and III styles also provide enormous reductions in energy consumption, with the Type III style providing an 8x reduction when using PG cascading. The energy consumption of the Type II style strongly depends on the cascading approach, with PG cascading producing an energy consumption 4x less than CG cascading. The lack of complementary transistors in the Type II A-PTC results in lower signal integrity than with the A-TGC used in Types I and III, leading to increased EDP and AEDP for Type II.

Hybrid A-PTL drastically improves the overall computing efficiency, with the Type III style with PG cascading providing a 9x improvement in EDP and a 20x improvement in AEDP. These figures of merit leverage the slightly improved delay and massively improved energy consumption, with the AEDP further incorporating the 57% reduction in area (Table I). While the Type I style is also promising, the reduced transistor count and simplified circuit structure provide the Type III style the greatest potential for compact and efficient circuits.

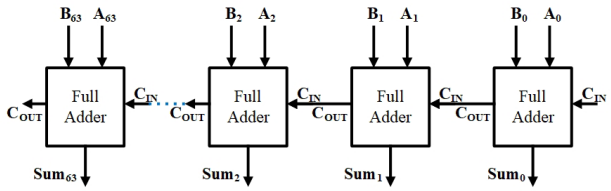

Fig. 15. Block diagram of 64 cascaded one-bit full adders.

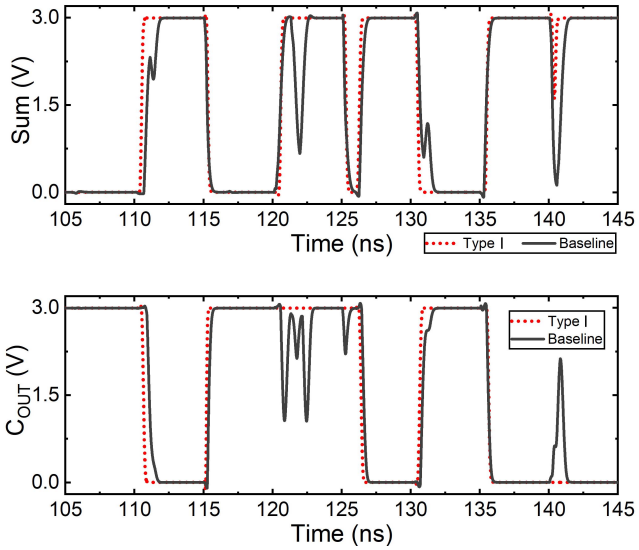

Fig. 16. Output waveform of the last stage of a 64-bit adder.

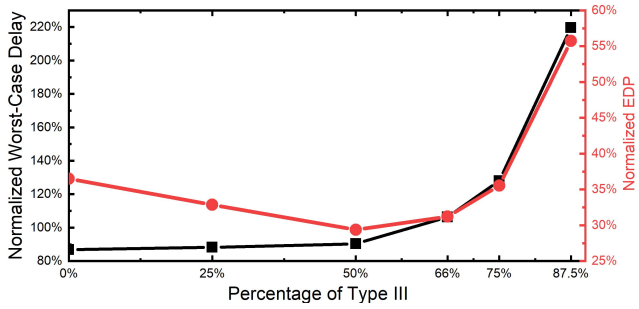

Fig. 17. Performance evaluation for the mixture of Type I and Type III structures.

In circuits with long cascaded chains of hybrid A-PTL gates, it is necessary to ensure that no signal has a path through too many transmission gates without an inverter. To investigate this concern, a 64-bit ripple-carry adder (Fig. 15) was simulated in the Type III style with CG cascading; the circuit fails to produce the correct output for some input combinations due to the presence of an inverter-free path across all 64 bits. In contrast, the Type I style, which has at least one inverter between each transmission gate, provides correct results with a delay smaller than the baseline. This is shown in Fig. 16, which also uses CG cascading. For both Type I and the baseline, the worst-case delay is found to be roughly 16x larger than the worst-case delay of a four-bit adder, suggesting a proportional relationship between delay and number of bits.

Given the superior energy efficiency of Type III over Type I, it is worthwhile to consider the optimal mixture of the Types I and III styles. As shown in Fig. 17, various mixtures were evaluated, from a fully-Type I system to a system that is 87.5% Type III and 12.5% Type I, all with CG cascading. (In other words, an 87.5% Type III system means that an additional inverter has been added after every eighth logic stage.) Given the proportional delay described above, the average energy is assumed to also scale proportionally with the number of bits. While the best delay is achieved with a fully Type I system, the EDP is optimized with a system that is roughly half Type III and half Type I.

The potential advantages and scaling limitations of the A-FETs are currently unknown. In order to avoid presenting misleading results, we have therefore focused only on apples-to-apples comparisons evaluating a single device type within varying logic families and circuit structures. Furthermore, while the results in this paper are specific to addition functions, the cascading trade-offs are also relevant to other functions. The application of this hybrid A-PTL logic family to future down-scaled devices or alternative ambipolar materials may impact the trade-offs among the six cascading styles.

V. Conclusion

DG-A-FETs are naturally compatible with PTL, and the proposed hybrid A-PTL family leverages the advantages of both DG-A-FETs and PTL by applying their required inverters in a manner that efficiently amortizes their costs. DG-A-FET logic requires inverters to generate complementary input signals to transistor pairs, while PTL requires inverters to restore voltage swing for signal integrity. By reusing the complementary signals generated by the inverters in a system implemented with DG-A-FETs, the PTL structure becomes more efficient than the conventional static CMOS structure. For the first time, we propose in this paper that DG-A-FETs can resolve the challenges of PTL, and demonstrate that a hybrid complementary/PTL circuit structure is highly effective with DG-A-FETs. This A-PTL family enables device count to be reduced by half, and increases energy-efficiency by an order of magnitude.

Comparisons among the three hybrid A-PTL styles proposed in this work indicate that the Type III style is superior, thanks to the complementarity of the A-TGC and the removal of the second inverter. Furthermore, CG cascading is shown to be faster than PG cascading, while PG cascading is shown to be more energy-efficient than CG cascading. By comparing a medium-scale hybrid A-PTL circuit to one realized with DG-A-FETs in the conventional CMOS-like logic style, the hybrid A-PTL system is shown to provide up to 47% decrease in delay, 57% reduction in area, 88% reduction in energy consumption, 9x reduction in EDP, and 20x reduction in AEDP. These results therefore greatly advance the already-promising prospects for efficient computing systems with ambipolar transistors.

References

[1] X. Chen, K. Ni, M. T. Niemier, Y. Han, S. Datta, and X. S. Hu, "Power and area efficient FPGA building blocks based on ferroelectric FETs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 5, pp. 1780–1793, May 2019.

[2] G. Wang *et al.*, "Ultra-dense ring-shaped racetrack memory cache design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 215–225, Jan. 2019.

[3] X. Wang, M. A. Zidan, and W. D. Lu, "A crossbar-based in-memory computing architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Jun. 18, 2020, doi: 10.1109/TCSI.2020.3000468.

[4] G. Papandroulidakis, A. Serb, A. Khiat, G. V. Merrett, and T. Prodromakis, "Practical implementation of memristor-based threshold logic gates," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3041–3051, Aug. 2019.

[5] R. Zand and R. F. DeMara, "MRAM-enhanced low power reconfigurable fabric with multi-level variation tolerance," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4662–4672, Dec. 2019.

[6] X. Hu, M. J. Schultis, M. Kramer, A. Bagla, A. Shetty, and J. S. Friedman, "Overhead requirements for stateful memristor logic," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 263–273, Jan. 2019.

[7] Y.-M. Lin, J. Appenzeller, and P. Avouris, "Novel carbon nanotube FET design with tunable polarity," in *IEDM Tech. Dig.*, Dec. 2004, pp. 687–690.

[8] Y.-M. Lin, J. Appenzeller, J. Knoch, and P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 481–489, Sep. 2005.

[9] X. Hu and J. S. Friedman, "Closed-form model for dual-gate ambipolar CNTFET circuit design," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.

[10] X. Hu and J. S. Friedman, "Transient model with interchangeability for dual-gate ambipolar CNTFET logic design," in *Proc. IEEE/ACM Int. Symp. Nanosc. Archit. (NANOARCH)*, Jul. 2017, pp. 61–66.

[11] C. Pan *et al.*, "Analog circuit applications based on ambipolar Graphene/MoTe2 vertical transistors," *Adv. Electron. Mater.*, vol. 4, no. 3, Mar. 2018, Art. no. 1700662.

[12] S. G. Bucella *et al.*, "Inkjet printed single-walled carbon nanotube based ambipolar and unipolar transistors for high-performance complementary logic circuits," *Adv. Electron. Mater.*, vol. 2, no. 6, Jun. 2016, Art. no. 1600094.

[13] J. Zhang, P.-E. Gaillardon, and G. De Micheli, "Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, pp. 2111–2114.

[14] J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-controllable silicon nanowire transistors with dual threshold voltages," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3654–3660, Nov. 2014.

[15] M. De Marchi *et al.*, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire fets," in *IEDM Tech. Dig.*, Dec. 2012, pp. 8.4.1–8.4.4.

[16] X. Hu, W. H. Brigner, and J. S. Friedman, "CNT and SiNW modeling for dual-gate ambipolar logic circuit design," in *Functionality-Enhanced Devices An alternative to Moore's Law*, P.-E. Gaillardon, Ed. London, U.K.: Institution of Engineering and Technology, Nov. 2018, ch. 8, pp. 151–188.

[17] L. Yin *et al.*, "Ferroelectric-induced carrier modulation for ambipolar transition metal dichalcogenide transistors," *Appl. Phys. Lett.*, vol. 110, no. 12, Mar. 2017, Art. no. 123106.

[18] Y. Zhang, J. Ye, Y. Matsuhashi, and Y. Iwasa, "Ambipolar MoS2 thin flake transistors," *Nano Lett.*, vol. 12, no. 3, pp. 1136–1140, Mar. 2012.

[19] B. Kim, M. L. Geier, M. C. Hersam, and A. Dodabalapur, "Inkjet printed circuits based on ambipolar and p-type carbon nanotube thin-film transistors," *Sci. Rep.*, vol. 7, no. 1, May 2017, Art. no. 39627.

[20] D. N. Ortiz, I. Ramos, N. J. Pinto, M.-Q. Zhao, V. Kumar, and A. T. C. Johnson, "Ambipolar transport in CVD grown $MoSe_2$ monolayer using an ionic liquid gel gate dielectric," *AIP Adv.*, vol. 8, no. 3, Mar. 2018, Art. no. 035014.

[21] J. F. Tian, L. A. Jauregui, G. Lopez, H. Cao, and Y. P. Chen, "Ambipolar graphene field effect transistors by local metal side gates," *Appl. Phys. Lett.*, vol. 96, no. 26, pp. 94–97, 2010.

[22] M. Yu, H. Wan, L. Cai, J. Miao, S. Zhang, and C. Wang, "Fully printed flexible dual-gate carbon nanotube thin-film transistors with tunable ambipolar characteristics for complementary logic circuits," *ACS Nano*, vol. 12, no. 11, pp. 11572–11578, Nov. 2018.

[23] K.-J. Baeg, H. J. Jeong, S. Y. Jeong, J. T. Han, and G.-W. Lee, "Enhanced ambipolar charge transport in staggered carbon nanotube field-effect transistors for printed complementary-like circuits," *Current Appl. Phys.*, vol. 17, no. 4, pp. 541–547, Apr. 2017.

[24] M. H. Ben-Jamaa, K. Mohanram, and G. De Micheli, "An efficient gate library for ambipolar CNTFET logic," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 2, pp. 242–255, Feb. 2011.

[25] G. V. Resta *et al.*, "Polarity control in WSe2 double-gate transistors," *Sci. Rep.*, vol. 6, no. 1, Sep. 2016, Art. no. 29448.

[26] K. Yano, Y. Sasaki, K. Rikino, and K. Seki, "Top-down pass-transistor logic design," *IEEE J. Solid-State Circuits*, vol. 31, no. 6, pp. 792–803, Jun. 1996.

[27] D. Radhakrishnan, S. R. Whitaker, and G. K. Maki, "Formal design procedures for pass transistor switching circuits," *IEEE J. Solid-State Circuits*, vol. 20, no. 2, pp. 531–536, Apr. 1985.

[28] K. Yano, A. Shimizu, T. Nishida, M. Saito, and K. Shimohigashi, "A 3.8-ns CMOS 16×16-b multiplier using complementary pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 388–395, 1990.

[29] J. von Neumann, "First draft of a report on the EDVAC," Moore School Elect. Eng., Univ. Pennsylvania, Philadelphia, PA, USA, Tech. Rep., 1945.

[30] K. Jabeur, I. O'Connor, N. Yakymets, and S. Le Beux, "High performance 4:1 multiplexer with ambipolar double-gate FETs," in *Proc. 18th IEEE Int. Conf. Electron., Circuits, Syst.*, Dec. 2011, pp. 677–680.

[31] A. Zukoski, X. Yang, and K. Mohanram, "Universal logic modules based on double-gate carbon nanotube transistors," in *Proc. 48th Design Autom. Conf. DAC*, Jun. 2011, pp. 884–889.

[32] F. Kenarangi, X. Hu, Y. Liu, J. A. C. Incorvia, J. S. Friedman, and I. Partin-Vaisband, "Exploiting dual-gate ambipolar CNFETs for scalable machine learning classification," *Sci. Rep.*, vol. 10, no. 1, p. 5735, Dec. 2020.

[33] J. S. Friedman, M. L. Geier, M. C. Hersam, and A. V. Sahakian, "System and method for complimentary VT-drop ambipolar carbon nanotube logic," U.S. Patent 10 594 319, Mar. 17, 2020.

[34] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[35] J. Zhang, X. Tang, P.-E. Gaillardon, and G. De Micheli, "Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2851–2861, Oct. 2014.

Xuan Hu (Graduate Student Member, IEEE) received the B.S. degree in electrical and information engineering from Huaqiao University, Xiamen, China, in 2013, and the M.S. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2015. He is currently pursuing the Ph.D. degree in electrical engineering with the Erik Jonsson School of Engineering and Computer Science, The University of Texas at Dallas, Richardson, TX, USA.

His current research interests include circuit design and modeling of efficient logic and neuromorphic circuits composed of ambipolar carbon nanotubes, skyrmions, magnetic domain-wall devices, memristors, and multi-gate transistors.

Amy S. Abraham is currently a Junior with the Erik Jonsson School of Engineering and Computer Science, The University of Texas at Dallas, majoring in Electrical Engineering and Computer Engineering. Her current research interests include circuit design and modeling of efficient logic circuits composed of ambipolar carbon nanotubes.

Jean Anne C. Incorvia (Member, IEEE) received the B.A. degree in physics from the University of California, Berkeley, Berkeley, CA, USA, in 2008, and the A.M. and Ph.D. degrees in physics from Harvard University, Cambridge, MA, USA, in 2012 and 2015, respectively.

She was a Post-Doctoral Research Associate with Stanford University, Stanford, CA, USA, from 2015 to 2017, and joined the Department of Electrical and Computer Engineering, The University of Texas at Austin, as an Assistant Professor, in 2017. Her technical contributions include the development of magnetic compute-in-memory and neuromorphic devices and circuits, and device and materials research in novel materials, including low dimensional materials and emerging memories. She received the 2020 National Science Foundation CAREER award and the 2020 IEEE Magnetics Society Early Career Award. She holds the 2020–2021 Fellow of the AMD Chair with UT Austin.

Joseph S. Friedman (Senior Member, IEEE) received the A.B. and B.E. degrees from Dartmouth College, Hanover, NH, USA, in 2009, and the M.S. and Ph.D. degrees in electrical and computer engineering from Northwestern University, Evanston, IL, USA, in 2010 and 2014, respectively.

He joined The University of Texas at Dallas, Richardson, TX, USA, in 2016, where he is currently an Assistant Professor of electrical and computer engineering and the Director of the NeuroSpinCompute Laboratory. From 2014 to 2016, he was the Centre National de la Recherche Scientifique Research Associate with the Institut d'Electronique Fondamentale, Université Paris-Sud, Orsay, France. He has also been a Summer Faculty Fellow with the U.S. Air Force Research Laboratory, Rome, NY, USA, a Visiting Professor with the Politecnico di Torino, Turin, Italy, a Guest Scientist with RWTH Aachen University, Aachen, Germany, and worked on logic design automation as an Intern with Intel Corporation, Santa Clara, CA, USA.

Dr. Friedman is a member of the Editorial Board of *Microelectronics Journal*, the technical program committees of DAC, DATE, SPIE Spintronics, NANOARCH, GLSVSI, ICECS, and VLSI-SoC, the review committee of ISCAS, and the IEEE Circuits and Systems Society Nanoelectronics and Gigascale Systems Technical Committee. He has been a member of the organizing committee of VLSI-SoC 2020, NANOARCH 2019, and DCAS 2018. He has also been awarded a Fulbright Postdoctoral Fellowship. His research interests include the invention and design of novel logical and neuromorphic computing paradigms based on nanoscale and quantum mechanical phenomena, with particular emphasis on spintronics.