SPICE-Only Model for Spin-Transfer Torque Domain Wall MTJ Logic

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Abstract — The spin-transfer torque domain wall (DW) magnetic tunnel junction (MTJ) enables spintronic logic circuits that can be directly cascaded without deleterious signal conversion circuitry and is one of the only spintronic devices for which cascading has been demonstrated experimentally. However, experimental progress has been impeded by a cumbersome modeling technique that requires a combination of micromagnetic and SPICE simulations. This paper, therefore, presents a SPICE-only device model that efficiently determines the DW motion resulting from spin accumulation and calculates the corresponding MTJ resistance. This model has been validated through comparison to the authoritative micromagnetic-based model, enabling reliable prediction of circuit behavior as a function of device parameters with a $10^4$ reduction in the simulation time. This model thus enables deeper device and circuit investigation, advancing the prospects for nonvolatile spintronic computing systems that overcome the von Neumann bottleneck.

Index Terms — Device model, magnetic domain wall (DW), magnetic tunnel junction (MTJ), spintronic logic.

I. INTRODUCTION

Spintronics could revolutionize the next generation of computing due to the possibility of high density, low power consumption, and nonvolatility. Spintronics can be employed in a wide variety of circuit applications, such as memory structures [1]–[7], sensors [8]–[11], neural networks [12]–[16], and logical computing [17]–[27]. For the proposed concepts of beyond-CMOS computing, cascading is a critical challenge that limits the integration of some spintronic devices into logical computing systems. In many spintronic logic proposals, signal conversion or level shifting is required between each logic gate, resulting in undesirable power, delay, and area costs. Some ideas [21]–[27] have been proposed to enable directly cascaded spintronic logic circuits, but experimental progress has been quite limited.

The domain wall (DW) magnetic tunnel junction (DW-MTJ) [23] shown in Fig. 1 is one of only two spintronic logic structures for which cascaded logic gates have been experimentally demonstrated (alongside nanomagnetic logic [28]). This DW-MTJ device permits logic cascading without any extra buffers or level shifters, while also storing the device state in a nonvolatile manner as part of the logic functionality. Beyond its potential use in conventional computing structures, the nonvolatile information storage permits logic-in-memory architectures that may overcome the von Neumann bottleneck.

Preliminary efforts to experimentally demonstrate the proposed computing system beyond a few logic gates [25], [26] have been hampered by the poor scalability of the available circuit simulation techniques. Although circuit simulations have previously been performed with a hybrid technique that combines micromagnetic simulation (OOMMF) [29] of the DW-MTJ magnetization with SPICE analysis of the currents and voltages, the complexity of the approach prevents a thorough exploration of device parameters within a reasonable timeframe. To enable the experimental demonstration of DW-MTJ circuits with optimized device parameters, it is therefore critical to efficiently simulate cascaded circuits through a technique that permits the facile modification and exploration of device parameters. While models have been developed for some magnetic devices and logic structures [12], [30]–[32], no closed-form models are available for the DW inertia that plays a critical role in DW-MTJ logic. This paper, therefore, includes DW inertia in a SPICE-only model of the DW-MTJ device that enables efficient analysis of DW-MTJ circuits. This novel closed-form Verilog-A model accelerates circuit simulation by a factor of $10^4$ while maintaining the accuracy provided by the hybrid micromagnetics-SPICE technique in [23].

II. BACKGROUND

The DW-MTJ device leverages MTJ magnetoresistance in concert with spin-transfer torque (STT)-driven DW motion to perform nonvolatile logical operations. Similar to a memristor controlled by the history of applied voltages, the DW-MTJ output resistance is determined by the cumulative current flow. In addition, the circuit structure proposed in [23] permits...
direct cascading without additional signal conversion circuitry and is one of the only spintronic logic devices for which this direct cascading has been experimentally demonstrated.

A. Magnetic Domain Wall Motion

In the soft ferromagnetic free layer shown in Fig. 1, the local magnetization direction beneath the left terminal (IN) is pinned upward, whereas the magnetization direction on the right (CLK) is fixed downward; there is, therefore, a DW at the transition region. This DW can be moved by applying an electrical current through STT [33]. Experimental evidence and physical simulations both demonstrate that a DW moves only if the current flowing through a ferromagnetic track exceeds a particular threshold [2], [34]. For the materials used in this device, the DW motion is in the direction of electron flow; the current magnitude is below the Walker breakdown threshold to ensure that the DW velocity is linearly proportional to the current magnitude. It should be noted that the electrical resistance of a ferromagnetic nanowire is almost completely unrelated to the presence and position of DWs within the nanowire.

B. MTJ Magnetoresistance

Conventional MTJs are composed of a fixed (hard) and a free (soft) ferromagnetic layer separated by a barrier. In the DW-MTJ device, the free layer is replaced by a ferromagnetic nanowire track as shown in Fig. 1. An MTJ is thus formed where the resistance is dependent on the relationship between the fixed layer magnetization and the local magnetization within the nanowire track directly beneath the fixed layer. When the DW is to the left of the MTJ, as shown in Fig. 1, the MTJ exhibits the parallel low resistance \( R_p \). When the DW is to the right of the MTJ, the MTJ exhibits the antiparallel high-resistance \( R_{AP} \). These two discrete states can be used for digital logic, while the nonvolatility of the DW position has exciting implications for memory applications.

C. DW-MTJ Logical Operation

The DW-MTJ device [25], [26] is formed by combining an MTJ with a ferromagnetic nanowire track through which a DW can propagate, as shown in Fig. 1. It consists of a patterned ferromagnetic wire with an MTJ in the center and can be initialized using a current to have a single DW. The ferromagnetic track is 180 nm long, 5 nm wide, and 2.5 nm thick, and the fixed layer and tunnel barrier are 20 nm long and 5 nm wide. Logical operation consists of two steps: in the Write step, a voltage is applied between the IN and CLK terminals, and the DW propagates along the wire via STT [35]. During the Read step, a voltage is applied between the CLK and OUT terminals, reading out the resistance state of the device. For a device initialized as shown in Fig. 1, with the DW on the left and the MTJ in the parallel magnetization state, the device can switch from a high OUT current to a low current only if the input current from the previous device(s) is above the switching current threshold of the DW. With careful selection of the switching current threshold, a single DW-MTJ device can perform either the OR, AND, NOR, or NAND function based on the outputs of other DW-MTJ devices [23].

The cascading of DW-MTJ devices is shown in the shift register-based ring oscillator shown in Fig. 2. The OUT terminals of each device are connected to an IN terminal of another device, such that the voltages applied to the clock terminals cause current to flow through the devices. As shown in the figure, a high voltage on CLK2 reads the state of device 2, with the same current also writing device 3 and resetting the DW of device 2 to the left of the device. Experimental prototypes have shown that one DW-MTJ can drive two devices on its output and that a circuit of three inverters in series inverts the bit at each stage of the circuit [25], [26].

D. Hybrid OOMMF-SPICE DW-MTJ Model

Previous studies of the DW-MTJ device produced a model for DW-MTJs [23] that combines micromagnetic simulation [29] with SPICE to accurately capture both the magnetic and electronic behavior of the circuit as shown in the flowchart of Fig. 3(a). With this hybrid simulation technique, an external Python script alternates between calculations of the DW position via micromagnetic simulation and calculations of the currents and voltages via SPICE. Compared to SPICE-only simulation techniques, this hybrid approach requires enormous computational time and resources due to the complexity of the micromagnetic simulations.

This inability to efficiently simulate large-scale DW-MTJ circuits impedes the further development of this technology. In particular, recent experimental results have demonstrated proper cascaded logic functionality for four clock cycles, after which the DW-MTJ circuit ceases to perform the desired function [25], [26]. The development of a scalable SPICE-only simulation technique would, therefore, be greatly beneficial for large-scale circuit design.

III. DW-MTJ SPICE MODEL

The SPICE-only DW-MTJ model presented here [36] enables efficient and scalable circuit simulation and analysis. This model is inspired by recent models for memristors [37]–[40], which also exhibit a device resistance determined by the electrical history. The DW-MTJ is modeled as the resistor network shown in Fig. 4, where \( R_{MTJ} \) is continually updated as the DW moves through the track due to current flow through the fixed resistances \( R_L \) and \( R_G \).

The model procedure is illustrated in Fig. 3(b), with the DW spin accumulation, DW position, and MTJ resistance continually updated within a simple SPICE framework. While not perfectly representative of the underlying physics, this simplified model reduces the simulation time by 10000× while providing exceptional matching to the authoritative micromagnetic simulation results [23].

A. Domain Wall Propagation Velocity

When the current flows through the soft ferromagnetic nanowire, energy accumulates at the DW through the STT effect and eventually moves the DW along the nanowire track. If the current magnitude \( I \) is greater than a threshold \( I_{th} \),
the DW propagates along the electron flow direction with velocity \( v \) given by [35], [41]

\[
v_0 = \frac{J g P \mu_B}{2 e M_{\text{sat}}},
\]

(1)

where \( J \) is the current density flowing through the DW track, \( g \) is the Landé factor [42]–[44], \( \mu_B \) is the Bohr magneton, \( P \) is the spin polarization of conduction electrons, \( e \) is the electron charge, and \( M_{\text{sat}} \) [23] is the saturation magnetization. Any current below this threshold is considered insufficient to introduce DW motion. After the current is removed, DW inertia can cause a DW to continue to move until its accumulated energy is exhausted. As calculated by [45], the DW drift distance \( X_{\text{drift}} \) resulting from inertia is

\[
X_{\text{drift}} = \frac{\delta_{\text{DDW}}}{2 \alpha}
\]

(2)

where \( \delta_{\text{DDW}} \) is the width of the DW.

### B. Domain Wall Edge Repulsion

In the absence of applied current, a DW moving as a result of inertia can be reflected when it reaches the end of the track. In this case, the DW begins drifting in the opposite direction along the track. A portion of the DW inertia is lost when this reflection occurs, and the DW moves a distance \( X_{\text{repel}} \) in the opposite direction

\[
X_{\text{repel}} = K_{\text{repel}} \cdot X_{\text{drift}},
\]

(3)

where \( K_{\text{repel}} \) is the portion of the drift inertia that is reflected. As the DW drift distance varies significantly among devices and the underlying physics of the DW motion has not yet been fully explored, this model is designed to represent the behavior of the particular DW-MTJ proposed in [23]. Greater physical intuition can be integrated into this simplified model when it is available.

### C. Domain Wall Position Calculation

As described above, current flows through the nanowire track with magnitude greater than a threshold \( I_{th} \) causes the DW to propagate along the track. As a result of the DW inertia, the DW continues to propagate a distance \( X_{\text{drift}} \) after the input current is removed. Based on the previous results [23] that show a characteristic velocity \( v_0 \) as calculated in (1), the DW velocity \( v \) can be approximated as

\[
\begin{align*}
v &= \begin{cases} -v_0 & I > I_{th} \\ -v_0 & 0 < I < I_{th} \land X_{\text{inertia}} > 0 \\ 0 & \text{when } I_{th} < I < I_{th} \land X_{\text{inertia}} < 0 \\ +v_0 & \text{when } I < -I_{th},
\end{cases}
\end{align*}
\]

(4)

where \( I_{th} \) is the current threshold and \( X_{\text{inertia}} \) is the remaining distance that the DW can move as a result of the DW inertia. When the current pulse is below the threshold, the DW is driven by the inertia a distance of either \( X_{\text{drift}} \) or \( X_{\text{repel}} \), depending on whether the DW has been repelled by the edge. The DW velocity remains constant until the inertia is fully dissipated, at which point the velocity is set to zero. This \( X_{\text{inertia}} \) can, therefore, be expressed as

\[
X_{\text{inertia}} = \begin{cases} X_{\text{drift}} - v \cdot t_{\text{drift}} & \text{Drift State} \\ X_{\text{repel}} - v \cdot t_{\text{repel}} & \text{Repel State},
\end{cases}
\]

(5)

where \( t_{\text{drift}} \) and \( t_{\text{repel}} \) are the length of time length that the DW has been in the drift or repel state, respectively. The DW position is then calculated with

\[
X = X_0 + v \cdot \Delta t,
\]

(6)

where \( \Delta t \) is the simulation time-step and \( X_0 \) is the prior position.

### D. MTJ Resistance Calculation

The DW position determines the magnetization within the soft ferromagnetic track directly below the hard ferromagnetic fixed layer, thus governing the state of the MTJ formed by the fixed layer and the portion of the free layer directly below the fixed layer (see Fig. 1). When the DW is to the left of the left edge of the fixed layer \( X_{\text{MTJL}} \), the MTJ is in the parallel state; when the DW is to the right of the right edge of the fixed layer \( X_{\text{MTJR}} \), the MTJ is in the antiparallel state. The MTJ resistance is thus calculated as

\[
R_{\text{MTJ}} = \begin{cases} R_P & X < X_{\text{MTJL}} \\ R_{\text{AP}} & X > X_{\text{MTJR}} \\ R_{\text{IM}} & X_{\text{MTJL}} < X < X_{\text{MTJR}},
\end{cases}
\]

(7)

where the intermediate resistance \( R_{\text{IM}} \) resulting from a DW directly below the fixed layer is

\[
R_{\text{IM}} = \frac{X_{\text{MTJR}} - X}{X_{\text{MTJR}} - X_{\text{MTJL}}} \cdot R_P + \frac{X - X_{\text{MTJL}}}{X_{\text{MTJR}} - X_{\text{MTJL}}} \cdot R_{\text{AP}}.
\]

(8)

This model also includes an option to incorporate the dependence of the MTJ resistance on the bias voltage [6], [46], but this capability is not used in the simulations in this paper.

### IV. MODEL VALIDATION

To validate the model, SPICE-only simulations of both the ring oscillator shown in Fig. 2 and the full adder shown in Fig. 6(a) are compared to the hybrid OOMMF-SPICE results in [23]. The SPICE-only simulation results reliably reproduce the authoritative simulation results from the hybrid
Fig. 5. DW-MTJ ring oscillator simulated in response to a three-phase pulsed clock, showing close matching between the OOMMF-SPICE simulation technique (solid lines) in [23] and the SPICE-only model proposed here (dashed lines).

TABLE I

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Name</th>
<th>Value</th>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{	ext{MTJ}}$</td>
<td>800 kA/m²</td>
<td>$R_{	ext{MTJ}}$</td>
<td>55 kΩ</td>
<td>$I_{	ext{th}}$</td>
<td>3.5 μA</td>
</tr>
<tr>
<td>$R_{	ext{p}}$</td>
<td>100 Ω</td>
<td>$R_{	ext{p}}$</td>
<td>100 Ω</td>
<td>$W_{	ext{MTJ}}$</td>
<td>1.5 μm</td>
</tr>
<tr>
<td>$R_{	ext{m}}$</td>
<td>10 Ω</td>
<td>$W_{	ext{MTJ}}$</td>
<td>10 Ω</td>
<td>$W_{	ext{MTJ}}$</td>
<td>1.5 μm</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>0.01</td>
<td>$L_{	ext{MTJ}}$</td>
<td>20 nm</td>
<td>$\Delta t$</td>
<td>1 μs</td>
</tr>
<tr>
<td>$x_{	ext{MTJ}}$</td>
<td>2.5 nm</td>
<td>$R_{\text{track}}$</td>
<td>2.5 kΩ</td>
<td>$R_{\text{track}}$</td>
<td>1.8 kΩ</td>
</tr>
</tbody>
</table>

OOMMF-SPICE model; it is expected that this conclusion also applies to other circuits, though the prohibitive micromagnetic simulation time leads such further validation to be reserved for the future work. This SPICE-only model is, thus, shown to provide a 10000× improvement in the simulation time without significantly compromising accuracy.

A. Ring Oscillator

Clocked rectangular pulses are used to trigger the oscillations in the ring oscillator simulation. For the pulsed-clock scheme, the pulse height is $-120$ mV with a clock period of 5.2 ns and pulsewidth of 2 ns. As shown in Fig. 5 for the parameters given in Table I and the circuit shown in Fig. 2, the first clock pulse applied to Device 1 propagates to Device 2 through MTJ1; as Device 1 is in the parallel state, the output current is sufficient to move the Device 2 DW toward the right side of the track and switch MTJ2 to the antiparallel state. The clock pulse applied to Device 2 resets Device 2 by moving the DW to the left side of the track, but the output current through the antiparallel MTJ2 is below the threshold current and unable to move the DW of Device 3. Periodically applying these three clock pulses causes the data to shift among the devices arranged as an inverter ring, resulting in oscillation of the output current of Device 3. Fig. 5 validates the SPICE-only model by faithfully replicating the waveforms produced by the authoritative hybrid OOMMF-SPICE technique.

B. Full Adder

To further validate the accuracy of the proposed SPICE-only DW-MTJ model, the one-bit full adder from [23] is simulated as shown in Fig. 6. In this circuit, three-phase clocks with 2-ns pulse duration and $-125$-mV peak voltage at 65.79-MHz frequency are used to propagate the signal through the full adder circuit. In order to maintain signal synchronization, clocked buffers are used as delay stages. As described in [23] and listed in Table I, various values of $R_p$, $R_{\text{track}}$, and $I_{\text{th}}$ are used throughout the circuit.

Given the simplicity of this SPICE-only model, there is exceptional matching to the authoritative hybrid technique of micromagnetic and SPICE simulations [23]. These results demonstrate that the DWs continue to propagate after the current pulses are removed and that the SPICE-only approach thus accurately models the DW inertia. This SPICE-only model provides sufficient accuracy for reliable results, while also enabling the analysis of large-scale circuits and the optimization of device parameters.

V. CONCLUSION

The inadequacy of the available simulation techniques has impeded further development of cascaded DW-MTJ circuits. This paper, therefore, presents a SPICE-only model of the DW-MTJ that reduces the simulation time by a factor of 10000, thereby providing the ability to efficiently simulate large-scale circuits and to optimize device parameters to ensure proper functionality of these circuits. The model presented here is shown to accurately predict the device behavior and can be adapted to similar devices that exploit alternative physical phenomena. It is therefore hoped that this model can enable significant advances in the design of spintronic logic circuits, and the eventual replacement of CMOS with a highly efficient nonvolatile alternative.

REFERENCES


