# An SRAM Based on the MSET Device

Assaf Peled, Xuan Hu, Ofer Amrani, Joseph S. Friedman, and Yossi Rosenwaks

***Abstract*— From its conceptual inception in 2015, the combined capabilities of the multiple-state electrostatically formed nanowire transistor (MSET) have given way to a unique set of logic structures—in the example of NAND and NOR gates—which utilize fewer transistors as compared to conventional technologies. In this paper, we expand the recently published framework of MSET logic functions and present a static random access memory (SRAM) memory structure that consists entirely of MSET devices. Using TCAD simulations, we demonstrate the MSET-SRAM functionality in several phases of operation, while analyzing its performance in terms of speed, stability, and power consumption.**

***Index Terms*— Device simulations, multigate transistors, multiple-state electrostatically formed nanowire transistor (MSET) transistor, static random access memory (SRAM).**

## I. Introduction

TO PERFORM low-noise functions with minimal subthreshold noise, electrostatically formed nanowires (EFNs) [1], [2] have been demonstrated as the basis of highly precise biosensors [3]. The EFN has subsequently prompted the development of the multiple-state EFN transistor (MSET) [4], [5] and laid a theoretical groundwork for logic structures based solely on the MSET [6], [7].

The MSET is closely related to a double-gate JFET [8], [9] but differs from the latter by comprising two or more drains per single device. The double-drain MSET, based on Silicon-On-Insulator (SOI) technology [12], is schematically depicted in Fig. 1, together with the characteristic dimensions of its elements. The bulk substrate and the junction gates (JGs) are doped to form back-to-back one-sided p-n junction surrounding the bulk, with $N_{JG} = 10^{19}$ cm$^{-3}$ and $N_{bulk} = 5 \cdot 10^{17}$ cm$^{-3}$. The drains are separated by an oxide barrier, extending 70 nm in the $y$-direction and all the way down to the SOI buried oxide in the $z$-direction. The barrier has an indispensable role in obstructing leakage between drains and, moreover, bounding and shaping the depletion regions within the bulk.

Shallow trench isolation around the gates suppresses leakage between adjacent terminals and the surrounding devices.

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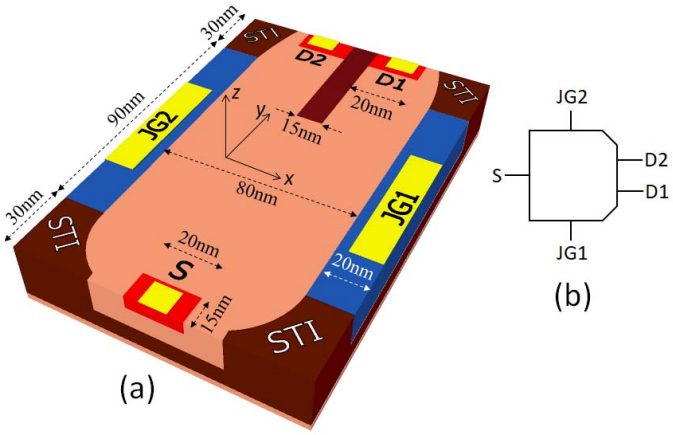


Fig. 1. (a) MSET Transistor. The EFN within the bulk has its size and position modulated by JG1, 2, while its strength is set by all five terminals. (b) MSET schematic symbol.

To prevent excess forward current between the JG and bulk, the MSET dynamic voltage range is limited to ±0.25 V. This range enables multiple MSETs to concatenate, thereby allowing the realization of MSET-based logical functions.

The MSET conduction channel is modulated by the presence or absence of a "nanowirelike" channel. Unlike conventional nanowire transistors [10], [11] where the conducting channel is formed by chemical doping during fabrication, the MSET channel is formed by the voltage applied to the device across its five terminals (see Fig. 1). When a differential bias is applied to the JGs (denoted JG1, JG2), the depletion region around the respective gate's p-n junction either expands into the bulk or recedes. Consequently, the conduction channel in between these depletion regions is *shifted laterally between drains* (denoted D1, D2).

Due to the MSET's nanodimensions, some degree of coupling exists between the drains. Providing a quantitative analysis of this coupling involves an exhaustive set of equations that underlie the MSET physics, down to energy band analysis. Prospective work on the MSET modeling should address these physical aspects. Compared to conventional transistors, this double-drain structure allows complex logic functions to be realized with fewer devices by integrating multiple drain contacts with a single semiconductor structure [6]. In addition, both n- and p-type MSETs are available (determined by the bulk doping), permitting complementary logic functions. As the fabrication technology of the MSET is compatible with other EFN devices, it is, therefore, possible to integrate MSETs with other logic families such as compact Boolean logic [13] and threshold logic [14].

Although various MSET logic structures have been proposed and demonstrated theoretically, it is not possible to realize MSET ecosystem without sequential synchronization

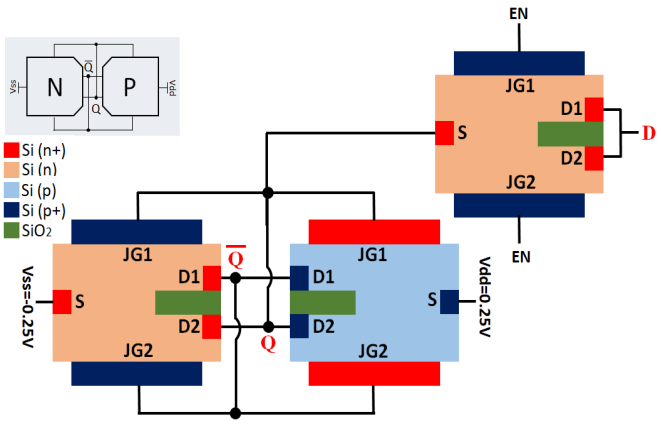


Fig. 2. MSET-SRAM cell illustration. On the top left corner is a schematic representation of the basic cross-coupling inverter cell.

blocks. Moreover, it is desirable to have memory cells with the same fabrication technology in an integrated MSET chip. In light of the need for synchronization and storage elements, this paper, therefore, proposes an MSET-based static random access memory (SRAM) cell to complete the MSET system. The framework also includes a sense amplifier (SA) [15], introduced as a peripheral component to accomplish read/write operations. These MSET memory elements, thus, promote a complete low-power computing system based entirely on MSET devices.

## II. Single Gate SRAM Cell

Fig. 2 shows three-MSET, or 3T SRAM cell, constituting the building block of the SRAM array [16]. The cell has the well-known cross-coupling inverters configuration with an additional data-enabling MSET that buffers between the cell and input $D$. To verify proper functioning, consider one polar case in which the cell holds a logic "0" at $Q$ (namely, $V_Q = -0.25$ V). $Q$ is then fed into JG1 of the n- and p-MSETs, pulling the output $\bar{Q}$ to logic "1" by virtue of their complementary structure (namely, $V_Q = +0.25$ V). $\bar{Q}$, in turn, is fed into JG2, ensuring that the cell retains its value. Depending on the cell's input signal, the cell quickly moves to one of its stable states by means of its regenerative action.

Stability during *Hold* is measured by its static noise margins (HSNMs), corresponding to the maximum value of voltage disturbance before changing logic states. In keeping with the well-known *butterfly curves* [17], [18], the SNM metric used is the maximum size square nested into the cross-coupled inverters voltage transfer characteristics. Graphical estimation of the SNM during standby operation is plotted in Fig. 3, where the butterfly curve of the feed-forward and feedback MSET-inverters is illustrated [19]. HSNM amounts to 0.124 V.

To reduce net area, each cell along with its respective SA consists of a single rather than two complementary bit lines. The SA's bistable operation during read is therefore preceded by precharging the bitline (BL) to 0 V before the word-line (WL) is enabled. To tackle issues related to majority carriers mobility, the cell's N-MSET height is set to 60 nm, whereas the P-MSET is twice as high to ensure proper symmetry of their conduction strength.

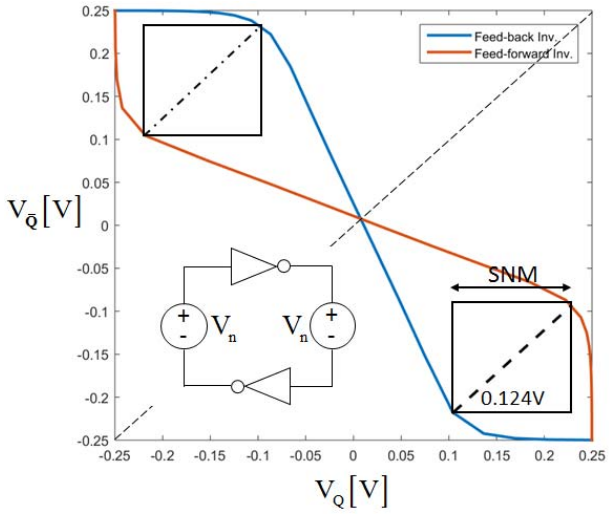


Fig. 3. HSNM analysis for the MSET cell.

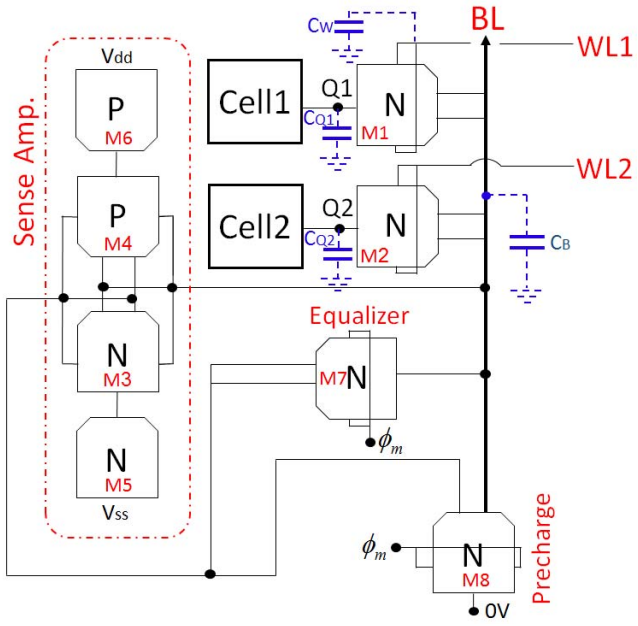


Fig. 4. Simulated setup of a $2 \times 1$ SRAM array and a SA. The capacitive elements in blue denote the equivalent array capacitance in different key nodes of the setup.

In the following sections, we demonstrate a simple MSET-SRAM array consisting of two cells, an SA and two peripheral MSET devices, as depicted in Fig. 4. M1 and M2 are the access transistors to cells #1 and #2, respectively, asserted by the WLs WL1 and WL2. MSETs M3 and M4 comprise the SA, which essentially features a bistable latch structure as shown in Fig. 3. The following operations are performed to examine the setup in Fig. 4; We start with a WRITE phase wherein cell #1 and cell #2 are assigned "0" and "1" logic, respectively. In the READ phase that follows, the SA responds sequentially to the stored bits in cells #1 and #2. Using 3-D modeling, MSETs M1–M7 are simulated in TCAD-Sentaurus, incorporating drift-diffusion carrier transport model, combined with Fermi–Dirac statistics with incomplete ionization.

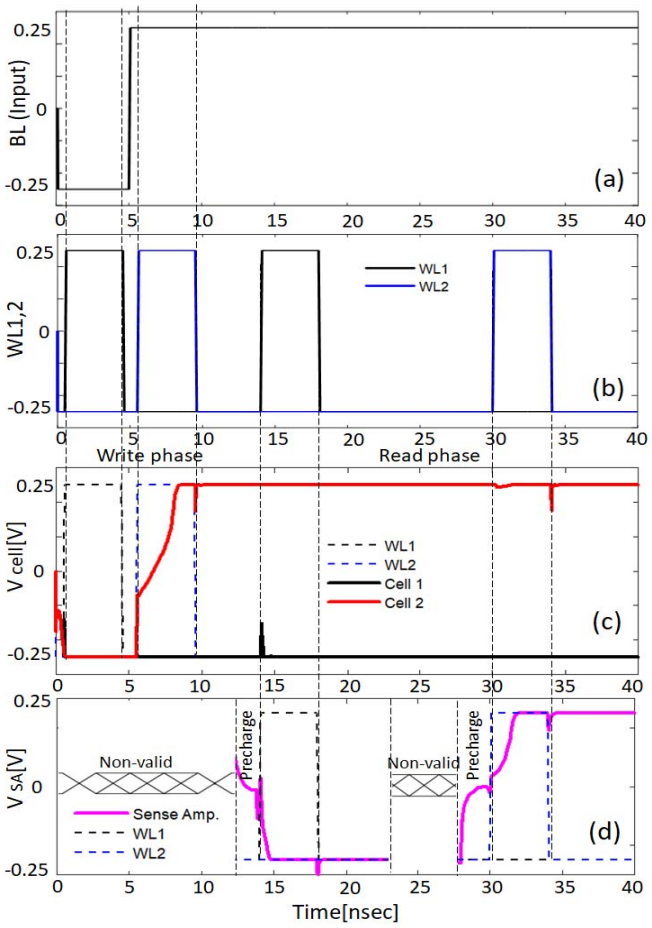


Fig. 5. Transient simulation results for the setup in Fig. 4. (a) BL voltage signal at the input. (b) WL1, WL2 voltage signals. (c) Voltage in cells 1 and 2. (d) Voltage signal in SA (top to bottom).

## III. WRITE Operation Analysis

As aforementioned, we begin with a successive storing of logic "0" and logic "1" in cells #1 and #2, respectively. As seen in Fig. 5, we reserve 10 ns for the entire WRITE phase, wherein the WL signals enabling MSETs M1 and M2 assume a semirectangular profile with a 0.1-ns rise and fall time. During WRITE, BL is charged −0.25 V ("0" logic) and M1 access N-MSET is asserted between 0.5 and 4.5 ns. Cell #1 output quickly stabilizes to logic "0" and retains its value. M2 is asserted through WL2 between 5.5 and 9.5 ns, pulling up cell #2 output to 0.25 V (logic "1"). During the first part of the WRITE cycle, cell #2 is pulled down to logic "0" prior to clocking, suggesting that the cell's feedback loop is predisposed to pull-down output Q2.

The intersection of BL and WL with the cell, together with the lines' own capacitance to ground, set limitations on the MSETs operational speed. If we regard BL as a simple metal line, its parasitic capacitance to ground (substrate) per unit area [20] is $100[aF/\mu m^2]$. Considering the BL effective area relative to the MSETs sizing, we obtain an overall capacitance to ground in the order of $0.1[fF]$. While this may not seem very significant, one must also bear in mind the BL coupling with each access MSET along the column, together with the capacitive coupling of WL with the access MSET. In order for the MSET cell to toggle between states during writing, the WRITE process can be envisioned as involving the charging of the setup's lumped capacitive elements.

Let us observe, for instance, the WRITE "1" phase at 5.5–9.5 ns. The BL capacitance denoted $C_B$ in Fig. 4 accounts for the line own capacitance to ground, plus the capacitance between the line and both drains of access MSET M2, at which point $C_B$ is charged from −0.25 to 0.25 V. The assertion of WL2 in addition charges the lumped element $C_W$, representing the equivalent capacitance of WL to both JGs of M2. For cell#2 to change states, $C_{Q2}$ has to charge cell node $V_Q$ beyond the feed-forward inverter's threshold voltage, so as to initiate the cell's regenerative action. However, when writing logic "1" into cell #2, 0.25 V is applied to both JGs of access MSET M2. MSET M2 charges internal node $Q$ to 0.25 V all the while, gradually reverse-biasing [21] the access MSET's bulk-to-JG p-n junction and consequently decreasing the drive-in current through M2. The transition from "0" logic to "1" during writing, as seen in Fig. 5, is therefore significantly slower than the vice versa ("1" to "0").

The average power consumption per cell depends on the frequency at which it is accessed. The average dynamic power is dissipated by the current required to charge the setup's internal nodes, as illustrated in Fig. 4. Summing the power dissipated in all MSETs activated during a particular operation, we have

$$\sum_j \frac{1}{t_r} \int_{t_r} I_j(t) \cdot V_j(t) dt. \tag{1}$$

Equation (1) sums the $I$–$V$ products of the $j$th MSET either during the transient phase of READ/WRITE or in the intermediate intervals between successive operations where the setup is idle. $t_r$ denotes the time interval for the respective operation, over which (1) is evaluated. Static power consumption is equally present in the SRAM setup throughout all MSETs, mainly due to reverse-bias leakages between JGs and substrate. The average static power dissipated is evaluated as

$$\sum_j \frac{1}{t_s} \int_{t_s} I_j(t) \cdot V_j(t) dt \tag{2}$$

again, with $j$ denoting the $j$th MSET in the setup and $t_s$ is the intervals where none of the MSETs involved is actively conducting.

The dynamic power consumption during WRITE operation is summarized in Table I. The column labeled "Time" addresses the intervals where the MSETs change states, namely, from the time, the WL in question is asserted, until the cell output completes its excursion from "0" to "1," or vice versa. The energy per bit access during WRITE (in [fJ] units) is tabulated in the last column. Shown in Table I, the energy per bit access dissipated during WRITE "1" in access MSET M2 is appreciably large. This can be accounted for by the gradual narrowing of the conduction channel inside M2 as $C_{Q2}$ is being charged. To illustrate this, Fig. 6 captures four TCAD simulation images of the access-MSET M2 during WRITE "1" operation into cell #2.

The two pairs of images on the top and bottom of Fig. 6 depict the current density and charge carrier concentration at

TABLE I
SINGLE BL-SRAM DYNAMIC POWER CONSUMPTION WRITE OPERATION

| Operation | Time[ns] | MSETs involved | Mean dynamic power consumption[nW] | Energy per Bit access [fJ] |
|---|---|---|---|---|
| Write '0' | 0.5-0.71 | Cell#1 | 16.1 | 0.005 |
| Write '0' | 0.5-0.71 | M1 | 129.11 | 0.03 |
| Write '1' | 5.5-8.62 | Cell#2 | 26.49 | 0.082 |
| Write '1' | 5.5-8.62 | M2 | 37.40 | 0.12 |

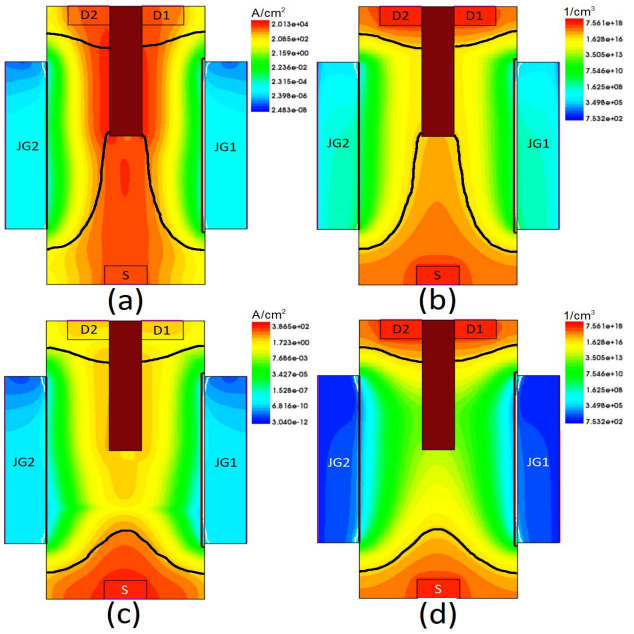


Fig. 6. TCAD simulations of WL MSET M2 (see Fig. 4) during WRITE "1" operation. (a) Current density (A/cm2) at 5.8 ns, when output $Q$ of cell2 is start charging toward logic "1." (b) Free carriers distribution in M2 at 5.8 ns. (c) Current density in M2 at 8 ns, when cell2 $Q$ is nearly fully charged. (d) Free carriers distribution in M2 at 8 ns.

the start and end of the writing process, respectively. The solid black lines within the MSETs denote the effective depletion borders inside the bulk volume, which expand accordingly as D1-to-JG1, D2-to-JG2, and S-to-JG1, 2 junctions become progressively reverse-biased. This process gradually narrows the conduction channel's cross section within M2, therefore increasing its effective impedance and inflicts energy losses. With that in mind, however, it is sufficient during WRITE "1" operation to hold WL2 high until $Q$ surpasses the 0-V metastable point, at which time the cell's regenerative action inherently pulls up $Q$ to logic "1" and $\bar{Q}$ to logic "0."

Fig. 6 implies that for a feasible WRITE operation, it is crucial to consider the delay incurred by the capacitive elements associated with BL and assess the proper ratio of the access MSET which drives the cell, to the cell's pull-up MSET. Put differently, the access MSET should overpower the cell's MSETs and drive the cell beyond its metastable point within the time frame reserved for WL clocking. To this end, we set the cross-sectional height of the access MSET M1, M2 to 150 nm, namely, 2.5 times that of the cell's MSET. We define the transition time between states as the cell's output signal delay on its excursion from 10% to 90% of the valid logic values. Based on Fig. 5, the delay time for writing "0" is roughly 200 ps, whereas for writing "1" it is 3.137 ns.

TABLE II
COMPLEMENTARY BL-SRAM DYNAMIC POWER CONSUMPTION WRITE OPERATION

| Operation | Time[ns] | MSETs involved | Mean dynamic power consumption[nW] | Energy per Bit access [fJ] |
|---|---|---|---|---|
| Write '0' | 0.5-0.606 | Cell#1 | 92.25 | 0.01 |
| Write '0' | 0.5-0.606 | M1a, M1b | 325.88 | 0.035 |
| Write '1' | 5.5-6.06 | Cell#2 | 16.47 | 0.009 |
| Write '1' | 5.5-6.06 | M2a, M2b | 92.29 | 0.051 |

Moderating the adverse effects of parasitic capacitance can be achieved with a complementary BL. This entails the adding of one access MSET to each cell, resulting in area penalty. Considering the surplus area reserved for interconnections, a single MSET covers an area of 180 nm × 120 nm, indicating that a four-MSETs cell (of a complementary BL setup) would cover $0.9[\mu m^2]$, leading to an overhead area of about $0.3[\mu m^2]$ with respect to the SRAM cell in the single BL setup. Adding one access MSET to cells #1 and #2 in Fig. 4, we have simulated the complementary-BL setup with a similar timeline as shown in Fig. 5. The access MSETs for cells #1 and #2 are denoted {M1a, M1b} and {M2a, M2b}, respectively.

Simulation results for the WRITE operation of the complementary setup are shown in Table II. The complementary setup exhibits a significant improvement in the switching time of both WRITE "0" and "1" operations, owing to the two access MSETs driving the cell. Also, apparent is the overall reduction of energy per bit access in WRITE "1," as the combining driving force of the two access MSETs moderates their effective impedance with regard to the detrimental effect discussed in Fig. 6.

It would be difficult to conform to the conventional procedure for establishing a butterfly curve to derive the WRITE SNMs (WSNMs) of the MSET-SRAM, as two access transistors are required for the foregoing analysis. We turn instead to a simple procedure that essentially follows the very definition of noise margins. SNM metric assumes a dc voltage noise applied in opposite polarities to the two internal nodes of the feedback and feed-forward components of the SRAM cell. An illustration of the two "noisy" voltage sources with magnitude $V_n$ is given in the inset of Fig. 3. During WRITE operation, it is assumed that the three-MSET cell circuit can withstand only a finite amount of noise before becoming monostable, irrespective of the logic value being written. Another concern is to have the WRITE access time too short to flip the cell into the opposite stable state. To derive WSNM of the 3-MSET cell, we perform multiple WRITE simulation, each of which is introduced with varying dc noise (induced by sources $V_n$) with respect to the cell's metastable point, thus determining the maximum noise allowed before WRITE operation fails. Noise simulation results show that the WSNM of the three-MSET cell amounts to 0.121 V, namely, 24.4% of the total dynamic range [−0.25 V, 0.25 V].

## IV. READ OPERATION ANALYSIS

During READ operation, the SA's cross-coupled inverters reinforce the data present in the SA as long as power is supplied to the SA via MSETs M5-M6, and the SA, in turn,

TABLE III
SINGLE BL-SRAM DYNAMIC POWER CONSUMPTION READ OPERATION

| Operation | Time [ns] | MSETs involved | Mean dynamic power consumption[nW] | Energy per Bit access [fJ] |
|---|---|---|---|---|
| Read '0' | 12-14.9 | Cell#1 | 5.01 | 0.014 |
| Read '0' | 12-14.9 | M1 | 7.55 | 0.021 |
| Read '0' | 12-14.9 | M3-M8 | 44.8 | 0.13 |
| Read '1' | 28-31.9 | Cell#2 | 0.79 | 0.003 |
| Read '1' | 28-31.9 | M2 | 0.98 | 0.004 |
| Read '1' | 28-31.9 | M3-M8 | 19.95 | 0.11 |

TABLE IV
COMPLEMENTARY BL-SRAM DYNAMIC POWER CONSUMPTION READ OPERATION

| Operation | Time [ns] | MSETs involved | Mean dynamic power consumption[nW] | Energy per Bit access [fJ] |
|---|---|---|---|---|
| Read '0' | 12-14.7 | Cell#1 | 2.59 | 0.018 |
| Read '0' | 12-14.7 | M1a,M1b | 0.91 | 0.008 |
| Read '0' | 12-14.7 | M3-M8 | 15.32 | 0.10 |
| Read '1' | 28-30.8 | Cell#2 | 3.01 | 0.002 |
| Read '1' | 28-30.8 | M2a,M2b | 1.16 | 0.008 |
| Read '1' | 28-30.8 | M3-M8 | 16.16 | 0.10 |

provides a full-swing signal at its outputs. Thus, M5 and M6 eliminate leakage currents and static power losses by disabling $V_{dd}$ and $V_{ss}$ when the SA is off use. READ operation is preceded by a precharging phase, whereby $\phi_m$ goes high, setting the SA at its 0-V unstable equilibrium point through M8. MSET M7 speeds up the process by equalizing both SA inputs *and then* $\phi_m$ *goes low*. The WL of the read cell then exposes M1 to BL for a very short interval, pulling BL slightly toward the accessed cell's stored logic value. The last step causes an initial small voltage increment at the SA input, sufficient to initiate the regeneration mechanism of the SA.

The SA readout is nonvalid up to 12 ns, as M5 and M6 disconnect the SA from the supply rails. At 12.1 ns, M5 and M6 connect the SA to $V_{dd}-V_{ss}$ and $\phi_m$ turns high, precharging BL and both SA ends to 0 during the following 1.5 ns. WL1 subsequently opens M1 to allow reading access to cell #1, and the SA to stabilize at "0" logic almost immediately. Similar procedure takes place at 28 ns, after roughly 3 ns when the SA is disconnected again from the supply rails (thus, showing a nonvalid data). BL is once again precharged to 0 and WL2 turns high to enable access to cell #2. The SA output is pulled up to logic "1" in keeping with the value in cell #2.

The foremost concern during READ operation is to allow the SA to reach a stable state within the WL access time frame, without causing a failure in the read cell. During READ, $C_B$ also assumes an additional role in charging the SA internal node (connected to BL), as well as the SA's JG capacitance. As seen in Fig. 5, the single BL capacitance controls the READ operation delay, with an undesired effects on the overall READ "1" time that originate from similar internal dynamics of the SA-MSET to those depicted in Fig. 6. To ensure its proper operation with regard to the said limitations, we set the SA MSETs height to 300 nm. However, there exists an apparent tradeoff between READ delay and the SA MSETs height, as the latter may ensure the overpowering of the SA with respect to the read cell, but it equally increases the SA MSETs JG capacitance, thus incurring unwanted delays.

Tables III and IV show the READ time, average power and energy consumption of the MSET engaged in the READ process. READ time is determined from $\phi_m$ clocking until the SA output stabilizes on a valid logic value. Appreciable reduction in READ time with respect to the single-BL setup is observed when complementary setup is employed. The read static noise-margins (RSNMs) are obtained in a similar fashion to the WSNM and is also validated by setting the butterfly curves during READ, i.e., by setting the BL to 0 V and sweeping the cell voltage across the dynamic range. RSNM is found to be around 10.5% of the dynamic range or 0.052 V. The mean static power consumption in all MSETs is calculated by (2) and summarized in Table V.

TABLE V
SINGLE BL-SRAM STATIC POWER CONSUMPTION BY MSET

| MSET | Mean static power consumption[nW] |
|---|---|
| Cell#1 | 0.20 |
| Cell#2 | 0.36 |
| M1 | 0.33 |
| M2 | 0.09 |
| M3 | 0.55 |
| M4 | 0.32 |
| M5 | 0.007 |
| M6 | 0.007 |
| M7 | 0.01 |
| M8 | 0.005 |

Finally, for a fair analysis, we have also used Cadence simulator to simulate a setup similar to Fig. 4, this time within a 90-nm 6T SRAM-CMOS. In CMOS, the areas on-chip designated for SRAM are acknowledged as limiting the system's supply voltage scaling, seldom enabling operation below 1 V. Our simulation employs a 1.2-V cell, with a layout area of 0.1072 $\mu m^2$. The average WRITE delay is measured 94.85 ps, with an energy per bit access of 0.81 fJ, whereas the average READ delay is 71.2 ps, with 2.88-fJ energy per bit access. The HSNM, WSNM, and RSNM are 30.6%, 13.7%, and 10.2% of the total dynamic voltage, respectively.

## V. CONCLUSION

The study proposes and demonstrates a single BL SRAM device consisting entirely of MSET transistors and expands the recently published paradigm for MSET-based logic components. We show through TCAD simulations that the MSET-SRAM fulfills the basic operations required by a synchronized storage element. Simulation analysis demonstrates that the MSET-SRAM is well suitable for low-power, low-voltage applications. The study also addresses technical issues related to the operational speed of the memory device, arising due to the internal capacitive effects and other in-built physical limitations of the device. Future work should focus on enhancing the MSET capabilities as a preliminary step toward improving the MSET-SRAM performance.

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