Sequential Circuit Design with Bilayer Avalanche Spin Diode Logic

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ABSTRACT
Novel computing paradigms like the fully cascadable InSb bilayer avalanche spin-diode logic (BASDL) are capable of performing complex logic operations. Although the original work provides a comprehensive explanation for the device structure, the fundamental logic set and basic combinational circuits, it lacks the inclusion of sequential circuit design. This paper addresses the void by demonstrating the structural design of SR and D-type latches with BASDL. Novel latch topologies are proposed that take full advantage of the BASDL-based logic set while maintaining conventional latch functionality. The effective operation of these latches is verified through a complete logic-level analysis and a brief insight into their physical implementation.

CCS CONCEPTS
• Hardware → Spintronics and magnetic technologies:

KEYWORDS
Spin-Diodes, Flip-Flops, Spintronics

ACM Reference Format:

1 INTRODUCTION
Emerging device technologies like spintronics promise to serve as the foundation for the next generation of computing paradigms [1–6]. Ref. [4] improves on the proposal by Joo et al. [3] by devising a fully cascadable bilayer avalanche spin-diode logic (BASDL) structure. On one hand, the efficient cascading scheme enables the design of more compact circuits, while on the other, faster switching speeds are attainable due to their dependence on electromagnetic wave propagation delay rather than RLC delay [4, 6].

Both combinational and sequential circuits are required in a computing system. As opposed to combinational logic circuits whose state depends on the instantaneous values of the inputs, sequential circuits use the state of the previous inputs as additional data to determine the current output. This results in a memory element, which can be used to store information. Sequential circuits are essential in digital systems as they allow for the processing of data and control signals in a temporal manner.

2 BILAYER AVALANCHE SPIN-DIODE LOGIC
A spin-diode is a device with a negative magnetoresistance whose resistance state (and hence the output current) is modulated by the application of an external magnetic field. In the case of BASDL, this magnetic field is a result of the additive and counteractive interaction between the individual magnetic fields created by two current carrying wires $A$ and $B$ (Fig. 1) [4]. The magnitude and direction of the resultant magnetic field with respect to a threshold determines the resistance state of the spin-diode. Here, a logic ‘1’ is a large current, whereas a small current is the equivalent of logic ‘0’.

Since the output currents can be used to feed the control wires of subsequent BASDL devices, this scheme allows for a fully cascading logic design without the use of any amplification or control overhead. Further, depending on the relative direction of the two currents, the device performs either an inverted-input AND (IAND $= A \land \overline{B}$) or the conventional OR ($A \lor B$) operation. Together, these operations form a complete basis logic set.

3 BASDL SR LATCH DESIGN
The most fundamental latch constructed using basic CMOS logic gates is the ‘set-reset’ (SR) latch. IAND gates can be used to devise...
Table 1: Truth table for cross-coupled IAND SR Latch

<table>
<thead>
<tr>
<th>Characteristic Table</th>
<th>Excitation Table</th>
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<tbody>
<tr>
<td>$S$</td>
<td>$R$</td>
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<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
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where $Q$ and $Q_{next}$ are the present and next states of the latch, respectively. It can be noted that the hold and forbidden states are interchanged relative to a conventional CMOS SR latch.

An alternate, yet simpler structure consists of a cross-coupled IAND-OR loop (Fig. 2b) and behaves as a regular SR latch having the characteristic equation given by (2); the standard truth table is not shown here. This structure is particular to the basis logic set provided by BASDL, and is described by (2). Fig. 3 shows the physical implementation of the cross-coupled IAND-OR SR latch [4].

$$Q_{next} = S\overline{R} + \overline{Q}\overline{R}.$$  (2)

4 BASDL D LATCH DESIGN

The forbidden state of the SR latch can be eliminated by disallowing simultaneous identical inputs such that the reset input is replaced by $\overline{D}$ as the complement of set input $D$. A gated D latch with an active-low enable signal ($E_n$) can be designed using either of the two SR latch structures described in the previous section (Fig. 4). Fig. 4a shows a D latch constructed using the cross-coupled IAND SR latch. An IAND gate with a fixed high non-inverted input acts as an inverter and prevents the latch from entering the forbidden state. When the enable signal is low, the latch is set or reset in accordance with the $D$ input; otherwise the latch retains its previous state (Table 2). Hence, the characteristic equation of this latch is given by (3):

$$Q_{next} = \begin{cases} Q, & \text{when } E_n = 0 \\ D, & \text{when } E_n = 1. \end{cases}$$  (3)

The above structure requires the use of additional IAND gates as inverters prior to the SR latch stage for proper latch operation. This extra inversion stage can be eliminated by exploiting the cross-coupled IAND-OR SR latch described in the previous section. The characteristic equation and truth table of the resultant structure (Fig. 4b) is identical to a conventional D latch and is not shown here. This results in a significant reduction in the gate count and total gate delay, in concert with the lower switching times of bilayer avalanche spin-diodes [6].

5 CONCLUSIONS

The fully cascadable design and faster switching speeds enable BASDL to provide for a promising pathway towards efficient alternatives to conventional computing methods. This paper describes the design of fundamental latch topologies tailored to the BASDL logic set, making sequential computing possible for the first time. The proposed design can be extended, with relative ease, to other computing methods with asymmetric logic operations (similar to IANDs) as part of their fundamental logic set.

REFERENCES