Kanad Basu

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Education

PhD and MS in Computer Engineering, **University of Florida, USA** 2007 - 2012
Thesis: Efficient Techniques for Observability Enhancement during Post-Silicon Validation

B.E. in Electronics and Tele-Communication Engineering, **Jadavpur University, India** 2003 - 2007
Bachelor's project**:** Simulation of radiotherapy treatment for brain tumors on MRI images.

Employment History

Assistant Professor, Electrical and Computer Engineering, UT Dallas	2019 - present
Assistant Research Professor, Electrical and Computer Engineering, New York university	2017 - 2019
Senior R&D Engineer, Synopsys India Private Limited	2013 - 2017
Staff R&D Engineer, IBM India Software Labs (System Technology Group)	2012 - 2013
Graduate Technical Intern, Intel Corporation, Hillsboro, OR, USA	Summer 2011
Graduate Technical Intern, Intel Corporation, Folsom, CA, USA	Summer 2008

Honors and Awards

- Erik Jonsson School of Engineering **Outstanding Assistant Professor Award,** 2024.
- IEEE **Top Picks in Test and Reliability**, 2023, 2024.
- 3rd Prize at **Hack@DAC**, 2024, 2022.
- **Honorable Mention Award** at the International Conference on VLSI Design, 2021.
- 2nd Prize at **New York University Cyber Security Awareness Week** Logic Locking Competition, 2021.
- 3rd Prize at **New York University Cyber Security Awareness Week** Logic Locking Competition, 2020.
- Nominated for **Blavatnik Awards for Young Scientists, 2019** Regional Postdoctoral competition.
- **Quarterly Achievement Award, 2015** fourth quarter, Synopsys Inc.
- **Best Paper Award** at the International Conference on VLSI Design 2011.
- **College of Engineering Travel grant** for attending IEEE VLSI Test Symposium, 2011.
- **CISE Departmental Travel grant** for attending IEEE International Test Conference, 2011.
- **Outstanding Student Achievement Award 2008 and 2010** from University of Florida Internal Center.
- **CISE Departmental Travel grant** for attending ACM Great Lakes Symposium on VLSI, 2008.
- **Scholarship from National Brain Research Center (NBRC), India** for summer internship at NBRC, 2006 (14 students across India were selected for the scholarship)**.**
- **Ranked 23rd (engineering stream)** in the West Bengal Joint Entrance Examination (among 170,000 examinees) in 2003.

Summary of Research Grant(s)

Total grants awarded --- $8.15M, My portion -- $2.9M, as **Single PI** -- $1.4M.

Summary of Publications

1 book, **2** book chapters, **46** journal articles, **92** referred conference papers and workshop proceedings, **2** patents, **1** tutorial, **7** thesis dissertations.

Summary of Students Mentored

Graduated Students**:** 5 (**PhD),** 10 **(MS)**.
Current Students in Lab**:** 11 **(PhD),** 1 **(MS)**, 4 **(BS).**

Summary of Professional Services

- **Associate Editor,** IEEE Design and Test Journal (2022 – present)
- **Associate Editor**, IET Computer and Digital Technology (2018 – present)
- **Guest Editor,** IEEE Journal on Emerging and Selected Topics in Circuits and Systems (July 2021)
- **Guest Editor,** Springer Journal of Electronic Testing (December 2019)
- **Track Chair,** IEEE Design Automation Conference, 2022
- **Track Co-chair,** IEEE Design Automation Conference, 2021
- **Finance Chair,** IEEE VLSI Test Symposium, 2024.
- **Finance Co-chair,** IEEE Computer Society International Symposium on VLSI, 2021
- **Publication Chair,** IEEE International Symposium on LLM-aided Design, 2024.
- **Publication Co-chair,** IEEE VLSI Test Symposium, 2021, 2022
- **Technical Program Committee** (IEEE Design Automation Conference, 2020, 2021, 2022; IEEE Computer Society International Symposium on VLSI, 2020; IEEE International Conference on VLSI Design, 2015, 2018, 2019, 2020, 2021, 2023; IEEE High-Level Design, Verification and Trust Workshop, 2018; IEEE Rapid System Prototyping Workshop, 2016; IEEE International Symposium on Smart Electronics, 2018)
- **Organizing committee chair** (IEEE International Symposium on Rapid System Prototyping, 2014)

Press Release(s)

- SRC
- University of Texas at Dallas News (2024)
- University of Texas at Dallas News (2022)
- University of Texas at Dallas News (2020)
- ScienceDaily
- KXAN
- ABP News (Bengali)

Research Interests

Hardware Security, Functional Safety, Deep Learning Hardware Reliability and Security, Quantum Computing, EDA CAD tools, Embedded Security, Post-Quantum Cryptography.

Research Grant(s) (Awarded)

[1] K. Basu (Single PI), $249K, Secure and Robust Low Quantization AI Hardware, *Semiconductor Research Corporation*, Jan 2024 - Dec 2026.

[2] K. Basu (PI), $600K (My Portion: $291K), Collaborative Research: SaTC: CORE: Small: SOCIAL: System-on-Chip Information Flow Validation under Asynchronous Events, *National Science Foundation*, Oct 2022 – Sep 2025.

[3] K. Basu (Senior Personal, due to NSF restrictions on number of PIs), $5M (My Portion: $450K), ExpandQISE: Track 2: Neutral Atom Based Quantum Information Processing, *National Science Foundation*, Oct 2022 – Sep 2025.

[4] K. Basu (Lead PI), $400K (My Portion: $186K), Collaborative Research: SaTC: EDU: A Socially-Distant Cloud-Based Hardware Security Educational Platform, National Science Foundation, 08/2024 – 07/2027

[4] K. Basu (Lead PI), $220K (My Portion: $110K), Collaborative Research: EAGER: CSR: Full-stack defense of vision-based autonomous driving systems, National Science Foundation, 07/2024 – 06/2026

[5] K. Basu (Single PI), $150K, Improving System-on-Chip (SoC) Validation using Large Language Models, *Intel,* Oct 2023 – Sep 2026.

[6] K. Basu (Single PI), $393K, Securing System-on-Chip in a Zero-Trust Environment, *Technology Innovation Institute (Abu Dhabi, UAE)*, Dec 2022 – Dec 2025.

[7] K. Basu (Single PI), $249K, Machine Learning-based Functional Safety Improvement of AMS components in Automotive SoCs, *Semiconductor Research Corporation*, Jan 2022 - Dec 2024.

[8] K. Basu (Single PI), $247K, Improving Fault Injection-based Functional Safety Evaluation using Machine Learning, Semiconductor Research Corporation, Jan 2023 - Dec 2025.

[9] K. Basu (Single PI), $225K, Effective In-field Testing and Diagnosis for improvement of Functional Safety, *Semiconductor Research Corporation*, Jan 2020 - Dec 2022.

[10] K. Basu (Lead PI), $160K (My Portion: $130K), Scalable Security Verification Framework for Digital and Analog/Mixed-Signal System-on-Chips, *NSF CHEST I/UCRC*, 06/01/2021-05/31/2024.

[11] K. Basu (co-PI), $270K (My Portion: $85K), Machine Learning-based efficient Atomic Layer Deposition, *Semiconductor Research Corporation*, Jan 2021 - Dec 2023.

[12] K. Basu (co-PI), $20K (My Portion: $5K), Vaccinating Integrated Circuits Interconnected with Attack-Immune Architecture, *Defense Advanced Research Projects Agency*, May 2020 – Nov 2020.

[13] K. Basu (co-PI), $150K (My Portion: $100K), MIDAS TOUCH: Malware Identification in Driver Assistance Systems by Tracking On-chip Unhackable Counter Hardware, *Ford Motors*, Aug 2019 - Jul 2022.

[14] K. Basu (co-PI), $25K (My Portion: $10K), Real-Time Analysis Infrastructure for Attack-Resilient Robotic Vehicle Controllers, *UTD New Faculty Research Symposium*, 04/01/2021-03/31/2022.

Research Experiences

University of Texas at Dallas — **Assistant Professor**
Department: Electrical and Computer Engineering — 2019 - Present
Research Group: Trustworthy and Intelligent Embedded Systems (TIES) Lab
PhD students graduated: Dr. Abraham Kuruvila, Dr. Ayush Arunachalam, Dr. Xingyu Meng, Dr. Shamik Kundu, Dr. Chao Lu.
Current PhD students: Ms. Amisha Srivastava, Mr. Sanjay Das, Mr. Samit Miftah, Mr. Navnil Choudhury, Mr. Anand Menon, Mr. Swastik Bhattacharya, Mr. Daksith Chandrasekhara, Mr. Ameya Bhave, Ms. Haimabati Dey, Mr. Dismas Ezechukwu and Mr. Pandy Kalimuthu.

- Hardware Security
- Functional Safety
- Deep Learning Hardware Reliability and Security
- Quantum Computing
- Post-Quantum Cryptography

New York University — **Assistant Research Professor**
Department: Electrical and Computer Engineering — 2017 – 2019
Research Group: Center for Cybersecurity — New York

- Malware Detection using Embedded Trace Buffer.
- Developing an Attack Vector into Electronics Supply Chain using EDA CAD tools.
- A theoretical framework for HPC-based malware detection techniques.
- Realization of a black-hat HLS tool.
- HLS-based IP protection mechanism.
- Security analysis of superconducting electronics.
- Planned Obsolescence on an IC using 3D NoCs.
- Designing a fault-tolerant TPU.

Synopsys India Private Limited — **Senior R & D Engineer**
Group: DFTMAX-Ultra R&D team. — 2013 – 2017
Research projects: — Bangalore, India

- Developing a low-power, low-pin DFT solution.
- Improving post-silicon debug methodologies. (In collaboration with IIT Bombay, India).
- Efficient post-silicon debug techniques for wireless NoCs. (In collaboration with IIIT Delhi, India).

IBM India Private Limited — **Staff R & D Engineer**
Group: System Technology Group of IBM India Software Labs. — 2012 – 2013

Research projects: Bangalore, India

- Crosstalk-aware ATPG algorithm.
- DFT for IBM Power and Z supercomputers.

University of Florida **Graduate Student**
Department: Computer and Information Science and Engineering 2007 – 2012
Research Group: Embedded Systems Lab Gainesville, Fl

- Efficient Trace Signal Selection for Post-Silicon Debug
- Static Dictionary based Trace Data Compression for Post-Silicon Debug
- Efficient techniques to combine Trace and Scan signals for Post-Silicon Debug
- Partition based signal selection for Error Detection in Post-Silicon Debug
- Bitmask based Test Data Compression
- Bitmask aware NISC Control Word Compression

National Brain Research Center **Undergraduate intern**
Research Group: Computational Neuroscience 2006

- Simulation of Radiotherapy on MRI images of brain. Gurgaon, India

Jadavpur University **Undergraduate Student**
Department: Electronics and Telecommunication Engineering Kolkata, India
Research Group: Mobile Networking and AI

- Car number plate detection using discrete Hopfield Neural Networks.
- Connectivity Maintenance in Mobile Ad-hoc Network.

Industry Experiences

Synopsys India Private Limited **Senior R & D Engineer**
Team: TEST team of Synopsys 2013 – 2017
Project: *Development of DFTMAX Ultra, the state-of-the-art low pin test compression solution from Synopsys.* Bangalore, India

IBM India Private Limited **Staff R & D Engineer**
Group: IBM System and Technology Group 2012 – 2013
Project: *DFT (Design for Test) for Power and Z Processors* Bangalore, India

Intel Corp. **Graduate Technical Intern**
Group: PVE Group May 2011 – Aug 2011
Project: *Developed a tool to automate signal selection for post-silicon debug in actual industrial designs: taking care of latches, multiple clock domains and large number of gates in each design.* Hillsboro, OR, USA

Intel Corp. **Graduate Technical Intern**
Group: SEG group May 2008 – Aug 2008
Project: *Developed a tool to automate the translation of TLM tests to RTL tests.* Folsom, CA, USA

Teaching Experience

University of Texas at Dallas **Assistant Professor**
Department of Electrical and Computer Engineering 2019 – Present
Graduate course: *Hardware Security (Fall 2019, Spring 2021, Fall 2022), Computer Architecture (Spring 2023), Applied Data Structures and Algorithms (Fall 2023, Fall 2024)* (Richardson, TX)

Undergraduate course: *Digital Circuits (Spring 2020, Fall 2020, Fall 2021, Fall 2022, Spring 2024)*

New York University — **Guest lecturer**
Department of Electrical and Computer Engineering — Fall 2018
Graduate course (Guest lecturer): *Advanced Hardware Design* — (New York, NY)

University of Florida — **Teaching Assistant**
Department of Computer and Information Science and Engineering — 2007 – 2012
Graduate courses TA: *Computer Architecture, Computer Networks, Embedded Systems, Operating Systems*. — (Gainesville, FL)
Undergraduate course: *Computer Organization, Problem solving using Computer Software*

Publications

Google Scholar profile: https://scholar.google.com/citations?user=q0PDoH8AAAAJ&hl=en

Book:

[1] Deepraj Soni, **Kanad Basu**, Mohammed Nabeel, Najwa Aaraj, Marc Manzano and Ramesh Karri. Hardware Architectures for Post-Quantum Digital Signature Schemes. Springer, 2020.

Book Chapters:

[2] Kanad Basu. Structural Signal Selection for Post-Silicon Validation, In: Post-Silicon Validation and Debug, Springer, 2018.

[3] Nirmalya Bandyopadhyay**, Kanad Basu** and Prabhat Mishra**.** HMDES, ISDL and Other Contemporary ADLs, In: Processor Description Languages: Applications and Methodologies, Morgan Kaufmann Publishers, 2008.

Journal Articles:

[4] Navnil Choudhury, Chao Lu, **Kanad Basu**. "Quantum Assertion Scheme for Assuring Qudit Robustness", *IEEE Computer Architecture Letters (CAL), 2024.*

[5] Shamik Kundu, Sanjay Das, Arnab Raha, Souvikk Kundu, Sayar Karmakar, Yiorgos Makris, **Kanad Basu**. "Bit-by-Bit: Investigating the Vulnerabilities of Binary Neural Networks to Adversarial Bit Flipping", *Transactions on Machine Learning Research (TMLR), 2024*.

[6] Chao Lu, Christian Pilato, **Kanad Basu**. "QHLS: An HLS Framework to Convert High-Level Descriptions to Quantum Circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024.*

[7] Amisha Srivastava, Sanjay Das, Navnil Choudhury, Rafail Psiakis, Pedro Silva, Debjit Pal, **Kanad Basu**. "SCAR: Power Side-Channel Analysis at RTL-Level", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, 2024.

[8] Samit S. Miftah, Kshitij Raj, Xingyu Meng, Sandip Ray, **Kanad Basu.** "System-On-Chip Information Flow Validation Under Asynchronous Resets", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2024.

[9] Chao Lu, Navnil Choudhury, Utsav Banerjee, Abdullah Saki, **Kanad Basu.** "QuBEC: Boosting Equivalence Checking for Quantum Circuits with QEC Embedding", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2024.

[10] Udit Kumar, Ayush Arunachalam, Corbein Feit, S Novia Berriel, **Kanad Basu,** Parag Banerjee, Sudipta Seal "Real-time artificial intelligence enhanced defect engineering in CeO2 nanostructures", *Journal of Vacuum Science & Technology*, 2023.

[11] Shamik Kundu, Suvadeep Banerjee, Arnab Raha, Fei Su, Suriyaprakash Natarajan, **Kanad Basu.** "DiagNNose: Towards Error Localization in Deep Learning Hardware based on VTA-TVM Stack". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2023.

[12] Abhijitt Dhavlle, N Meraj Ahmed, Naseef Mansoor, **Kanad Basu**, Amlan Ganguly, Sai Manoj PD. "Defense against On-Chip Trojans Enabling Traffic Analysis Attacks based on Machine Learning and Data Augmentation". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2023.

[13] Shamik Kundu, Suvadeep Banerjee, Arnab Raha, Fei Su, Suriyaprakash Natarajan, **Kanad Basu**. "Troubleshooting at GAN Point: Improving Functional Safety in Deep Learning Accelerators". *IEEE Transactions on Computers (TC)*, 2023.

[14] Rakibul Hassan, Xingyu Meng, **Kanad Basu**, Sai Manoj PD. "Circuit Topology-aware Vaccination-based Hardware Trojan Detection". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 2023.

[15] Ioannis Zografopoulos, Abraham Peedikayil Kuruvila, Charalambos Konstantinou, **Kanad Basu**. "Time Series-based Detection and Impact Analysis of Firmware Attacks in Microgrids". *Elsevier Energy Reports*, 2022.

[16] Shakya Chakrabarti, Akshay Wali, Harikrishnan Ravichandran, Shamik Kundu, Thomas Schranghamer, **Kanad Basu**, Saptarshi Das. "Logic Locking of Integrated Circuits Enabled by Nanoscale MoS2 Based Memtransistors". *ACS Applied Nano Materials*, 2022.

[17] Rajesh Datta, Guangwei Zhao, **Kanad Basu**, Kaveh Shamsi. "A Security Analysis of Circuit Clock Obfuscation". *MDPI Cryptography*, 2022.

[18] Ayush Arunachalam, Shamik Kundu, Arnab Raha, Suvadeep Banerjee, Suriyaprakash Natarajan, **Kanad Basu**. "A Novel Low-power Compression Scheme for Systolic Array-based Deep Learning Accelerators". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.

[19] Seetal Potluri, Shamik Kundu, **Kanad Basu**, Aydin Aysu. "SeqL+: Secure Scan-Obfuscation with Theoretical and Empirical Validation". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.

[20] Shamik Kundu, Arnab Raha, Suvadeep Banerjee, Suriyaprakash Natarajan, **Kanad Basu**. "Analysis and Mitigation of DRAM Faults in Sparse-DNN Accelerators". *IEEE Design and Test Journal (D&T)*, 2022.

[21] Xingyu Meng, Kshitij Raj, Sandip Ray, **Kanad Basu**. "SEVNOC: Security Validation of System-on-Chip Designs with NoC Fabrics", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.

[22] Debjani Sihi, Biswanath Dari, Abraham Peedikayil Kuruvila, Gaurav Jha, **Kanad Basu**. "Explainable Machine Learning Approach Quantified the Long-term (1981-2015) Impact of Climate and Soil Properties on Yields of Major Agricultural Crops across CONUS", *Frontiers in Sustainable Food Systems Journal*, 2022.

[23] Abraham Kuruvila, Xingyu Meng, Shamik Kundu, Gaurav Pandey, **Kanad Basu**. Explainable Machine Learning for Intrusion Detection via Hardware Performance Counters. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.

[24] Abraham Kuruvila, Anushree Mahapatra, Ramesh Karri, **Kanad Basu**. Hardware Performance Counters: Ready-Made vs Tailor-Made. *ACM Journal on Emerging Technologies in Computing Systems (JETC),* 2021.

[25] Nimisha Limaye, Nikhil Rangarajan, Satwik Patnaik, Ozgur Sinanoglu, **Kanad Basu**. PolyWorm: Leveraging Polymorphic Behavior to Implant Hardware Trojans. *IEEE Transactions on Emerging Topics in Computing (TETC)*, 2022.

[26] Sanjeev Tannirkulam Chandrasekaran, Abraham Kuruvila, **Kanad Basu** and Arindam Sanyal. Real-Time Hardware Based Malware and Micro-architectural Attack Detection Utilizing CMOS Reservoir Computing. *IEEE Transactions on Circuits and Systems II: Express Briefs (TCASII)*, 2022.

[27] Abraham Peedikayil Kuruvila, Ioannis Zografopoulos, **Kanad Basu**, Charalambos Konstantinou. Hardware-Assisted Detection of Firmware Attacks in Inverter-Based Cyberphysical Microgrids. *Elsevier International Journal of Electrical Power and Energy Systems (JEPE)*, 2021.

[28] Wenye Liu, Chip-Hong Chang, Xueyang Wang, Chen Liu, Jason Fung, Mohammad Ebrahimabadi, Naghmeh Karimi, Xingyu Meng, **Kanad Basu**. Two Sides of the Same Coin: Boons and Banes of Machine Learning in Hardware Security. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, 2021.

[29] Xingyu Meng, Shamik Kundu, Arun Kanuparthi, **Kanad Basu**. RTL-ConTest: Concolic Testing on RTL for Detecting Security Vulnerabilities. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.

[30] Ayush Arunachalam, Udit Kumar, Corbin Feit, S. Novia Berriel, Parag Banerjee, Sudipta Seal, **Kanad Basu**. A machine learning approach to thickness prediction from in situ spectroscopic ellipsometry data for atomic layer deposition processes. *AVS Journal of Vacuum Science and Technology A,* 2022.

[31] Udit Kumar, Corbin Feit, S. Novia Berriel, Ayush Arunachalam, **Kanad Basu**, Parag Banerjee, Sudipta Seal. In situ Ellipsometry aided Rapid ALD Process Development and Parameter Space Visualization of Cerium Oxide Nano-films. *AVS Journal of Vacuum Science and Technology A,* 2021.

[32] Akshay Wali, Shamik Kundu, Andrew Arnold, Guangwei Zhao, **Kanad Basu**, and Saptarshi Das. Satisfiability Attack Resistant Camouflaged Two-Dimensional Heterostructure Devices. *ACS Nano*, 2021.

[33] Rana Elnaggar, **Kanad Basu**, Krishnendu Chakrabarty, and Ramesh Karri. Run-time Malware Detection Using Embedded Trace Buffers. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021.

[34] Shamik Kundu, Suvadeep Banerjee, Arnab Raha, Suriyaprakash Natarajan and **Kanad Basu**, Towards Functional Safety of Systolic Array-based Deep Learning Hardware Accelerators. *IEEE Transactions on VLSI Systems (TVLSI)*, 2021.

[35] Siddhartha Sankar Rout, Sujay Deb and **Kanad Basu**, WiND: An Efficient Post-Silicon Debug Strategy for Network-on-Chip. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021.

[36] Abraham Kuruvila, Shamik Kundu and **Kanad Basu**, Defending Hardware-based Malware Detectors against Adversarial Attacks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021.

[37] Virinchi Roy Surabhi, Prashanth Krishnamurthy, Hussam Amrouch, **Kanad Basu**, Jorg Henkel, Ramesh Karri and Farshad Khorrami, Hardware Trojan Detection Using Controlled Circuit Aging. *IEEE Access*, 2020.

[38] **Kanad Basu**, Suha Hussain, Ujjwal Gupta and Ramesh Karri. COPPTCHA: COPPA Tracking by Checking Hardware-level Activity. *IEEE Transactions on Information Forensics and Security (TIFS),* 2020.

[39] Binod Kumar, Jay Adhaduk, **Kanad Basu**, Masahiro Fujita and Virendra Singh. A Methodology to Capture Fine-grained Internal Visibility during Multi-session Silicon Debug. *IEEE Transactions on VLSI Systems (TVLSI)*, 2020.

[40] **Kanad Basu,** Prashanth Krishnamurthy, Farshad Khorrami and Ramesh Karri. A Theoretical Study of Hardware Performance Counters-based Malware Detection. *IEEE Transactions on Information Forensics and Security (TIFS),* 2020.

[41] Harshit Kumar, Tahereh Jabberi, Gleb Krylov, **Kanad Basu**, Eby Friedman, and Ramesh Karri. Toward Increasing the Difficulty of Reverse Engineering of RSFQ Circuits. *IEEE Transactions on Applied Superconductivity,* 2020.

[42] **Kanad Basu,** Samah Saeed, Christian Pilato, Mohammad Ashraf, Mohammad Nabeel, Krishnendu Chakraborty and Ramesh Karri. CAD-Base: An Attack Vector into the Electronics Supply Chain. *ACM Transactions on Design Automation of Embedded Systems (TODAES),* 2019.

[43] Jeff Zhang, **Kanad Basu** and Siddharth Garg. Fault-tolerant Systolic Array Based Accelerators for Deep Neural Network Execution. *IEEE Design and Test of Computer (DNT),* 2019.

[44] Christian Pilato, **Kanad Basu** and Ramesh Karri. Black-Hat High-Level Synthesis: Myth or Reality? *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI),* 2019.

[45] Mohammad Shayan, **Kanad Basu** and Ramesh Karri. Hardware Trojans Inspired IP Watermarks. *IEEE Design and Test of Computer (DNT),* 2019.

[46] Binod Kumar, **Kanad Basu**, Masahiro Fujita and Virendra Singh. Post-Silicon Gate-Level Error Localization with Effective & Combined Trace Signal Selection. *Accepted for publication in IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

[47] **Kanad Basu,** Chetan Murthy and Prabhat Mishra. Bitmask aware compression of NISC Control Words. *Integration, the VLSI Journal* (Elsevier), 2013.

[48] **Kanad Basu** and Prabhat Mishra. Restoration Aware Trace Signal Selection for Post-silicon Validation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI),* 2013.

[49] **Kanad Basu** and Prabhat Mishra. Test Data Compression using Efficient Bitmask and Dictionary Selection Methods. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, 2009.

Peer-Reviewed Conference and Workshop Proceedings

[50] Navnil Choudhury, Chaithanya Naik Mude, Sanjay Das, Preetham Chandra Tikkireddi, Swamit Tannu, **Kanad Basu.** "Crosstalk-induced Side Channel Threats in Multi-Tenant NISQ Computers", *At Network and Distributed System Security Symposium (NDSS), 2025.*

[51] Sanjay Das, Anand Menon, Ayush Arunachalam, Rubin Parekhji, Prasanth Viswanath, Pooja Viswanath, **Kanad Basu.** "Enhancing AMS Circuit Reliability: A Benchmark for ML-Driven Fault Detection in Automotive SoCs", *At IEEE International Symposium on Circuits and Systems (ISCAS), 2025.*

[52] Sakib Reza, Sanjay Das, Shamik Kundu, **Kanad Basu**, Ifana Mahbub. "Efficient Explainable Boosting Machine for RF Active Metasurface Array Synthesis", *At IEEE Radio Wireless Week (RWW), 2025.*

[53] Chao Lu, Navnil Choudhury, **Kanad Basu.** "QuaSi: A Scalable and Reliable Quantum Simulation-based Equivalence Checking Framework", *At IEEE International Conference on Quantum Computing and Engineering (QCE), 2024.*

[54] Sanjay Das, Shamik Kundu, **Kanad Basu**. "Explainability to the Rescue: A Pattern-Based Approach for Detecting Adversarial Attacks". *At IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2024.*

[55] Samit Miftah, Amisha Srivastava, Hynmin Kim, **Kanad Basu**. "Assert-O: Context-based Assertion Optimization using LLMs". *At ACM Great Lakes Symposium on VLSI (GLSVLSI), 2024.*

[56] Navnil Choudhury, **Kanad Basu**. "A Survey of Side-Channel Attacks in Superconducting Quantum Computers". *At IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024.*

[57] Sakib Reza, Sanjay Das, Shamik Kundu, **Kanad Basu**, Ifana Mahbub. "Machine Learning Intervened RIS-based RF Interference Management For IoT". *At IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024.*

[58] Zhepeng Wang, Yi Sheng, Niranjan Koirala, **Kanad Basu**, Taeho Jung, Cheng-Chang Lu, Weiwen Jiang. "PristiQ: A Co-Design Framework for Preserving Data Security of Quantum Learning in the Cloud". *At IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024.*

[59] Xingyu Meng, Amisha Srivastava, Ayush Arunachalam, Avik Ray, Pedro Henrique Silva, Rafail Psiakis, Yiorgos Makris, **Kanad Basu**. "NSPG: Natural language Processing-based Security Property Generator for Hardware Security Assurance"*, AT ACM/IEEE Design Automation Conference (DAC), 2024.*

[60] Sanjay Das, Shamik Kundu, Pooja Madhusoodhanan, Prasanth Viswanathan Pillai, Rubin Parekhji, Arnab Raha, Suvadeep Banerjee, Suriya Natarajan, **Kanad Basu**. *"*Graph Learning-based Fault Criticality Analysis for Enhancing Functional Safety of E/E Systems"*, AT ACM/IEEE Design Automation Conference (DAC), 2024.*

[61] Shamik Kundu, Mirazul Haque, Sanjay Das, Wei Yang, **Kanad Basu**. "MENDNet: Just-in-time Fault Detection and Mitigation in AI Systems with Uncertainty Quantification and Multi-Exit Networks", *At ACM/IEEE Design Automation Conference (DAC), 2024.*

[62] Sanjay Das, Shamik Kundu, **Kanad Basu.** "Explainability to the Rescue: A Pattern-Based Approach for Detecting Adversarial Attacks", *At IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2024.*

[63] Shamik Kundu, Navnil Choudhury, **Kanad Basu**. "QuEST: Quantum Circuit Output Estimation using Gaussian Distribution Analysis", *At IEEE Symposium on Quality of Electronic Design (ISQED), 2024.*

[64] Shamik Kundu, Arnab Raha, Deepak A. Mathaikutty, **Kanad Basu**. "RASH: Reliable Deep Learning Acceleration using Sparsity-based Hardware", *At IEEE Symposium on Quality of Electronic Design (ISQED), 2024.*

[65] Xingyu Meng, Abhrajit Sengupta, **Kanad Basu**. "A Needle in the Haystack: Inspecting Circuit Layout to Identify Hardware Trojans", *At IEEE Symposium on Quality of Electronic Design (ISQED), 2024.*

[66] Sanjay Das, Shamik Kundu, Anand Menon, Yihui Ren, Shubha Kharel, **Kanad Basu.** "Analyzing and Mitigating Circuit Aging Effects in Deep Learning Accelerators", *At IEEE VLSI Testing Symposium (VTS), 2024.*

[67] Samit Miftah, Shamik Kundu, Austin Mordahl, Shiyi Wei, **Kanad Basu.** "RTL-Spec: RTL Spectrum Analysis for Security Bug Localization", *At IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2024.*

[68] Shamik Kundu, Navnil Choudhury, Sanjay Das, Arnab Raha, **Kanad Basu.** "QNAD: Quantum Noise Injection for Adversarial Defense in Deep Neural Networks", *At IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2024.*

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[70] Ayush Arunachalam, Sanjay Das, Monikka Rajan, Fei Su, Xiankun Jin, Suvadeep Banerjee, Arnab Raha, Suriyaprakash Natarajan, **Kanad Basu**. "Enhanced ML-based Approach for Functional Safety Improvement in Automotive AMS Circuits". *At International Test Conference (ITC)*, 2023.

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[72] Shamik Kundu, **Kanad Basu**. "Improving Fault Injection-based Functional Safety Evaluation using Machine Learning". *At SRC TECHCON*, 2023.

[73] Sanjay Das, Shamik Kundu, **Kanad Basu**. "Bottlenecks in Secure Adoption of Deep Neural Networks in Safety-Critical Applications". *At IEEE Midwest Symposium on Circuits and Systems (MWSCAS),* 2023.

[74] Anand Menon, Amisha Srivastava, Shamik Kundu, **Kanad Basu**. "Application Profiling Using Register-Instruction Hardware Performance Counters". *At IEEE Computer Society Annual Symposium on VLSI (ISVLSI),* 2023.

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[76] Chao Lu, Christian Pilato, **Kanad Basu**. "Towards High-Level Synthesis of Quantum Circuits". At *Design, Automation and Test in Europe Conference (DATE)*, 2023.

[77] Chao Lu, Amisha Srivastava, **Kanad Basu**. "Designing Complex Mathematical Functions using Quantum Hardware". At *GoMacTech* 2023.

[78] Xingyu Meng, **Kanad Basu**. "Scalable Semi-formal SoC Security Validation". At *GoMacTech* 2023.

[79] Shamik Kundu, **Kanad Basu**. "Towards Radiation-aware Functional Safety in Online AI Accelerators". At *GoMacTech* 2023.

[80] Ayush Arunachalam, **Kanad Basu**. "Detecting Radiation-aware Functional Safety Violation via Early Anomaly Detection". At *GoMacTech* 2023.

[81] Chao Lu, Utsav Banerjee, **Kanad Basu**. "Design and Analysis of a Scalable and Efficient Quantum Circuit for LWE Matrix Arithmetic". *At IEEE International Conference on Computer Design (ICCD)*, 2022.

[82] Shamik Kundu, **Kanad Basu**. "Detecting Functional Safety Violation in Online AI Accelerators". *At IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)*, 2022.

[83] Ayush Arunachalam, Shamik Kundu, Fei Su, Suvadeep Banerjee, Robert Jin, Arnab Raha, Suriyaprakash Natarajan, **Kanad Basu**. Unsupervised Learning-based Early Anomaly Detection in AMS Circuits of Automotive SoCs. *At International Test Conference (ITC)*, 2022.

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[85] Chao Lu, Shamik Kundu, Abraham Peedikayil Kuruvila, Supriya Margabandhu Ravichandran, **Kanad Basu**. Design and Logic Synthesis of a Scalable, Efficient Quantum Number Theoretic Transform. *At ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, 2022.

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[90] S. Kundu, S. Banerjee, A. Raha, **Kanad Basu**. Special Session: Effective In-field Testing of Deep Neural Network Hardware Accelerators. At *VLSI Test Symposium (VTS)*, 2022.

[91] Ayush Arunachalam, S. Novia Berriel, Parag Banerjee, **Kanad Basu**. Machine Learning-enhanced Efficient Spectroscopic Ellipsometry Modeling. *At AAAI Workshop on AI to Accelerate Science and Engineering (AI2ASE)*, 2022.

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[100] Ayush Arunachalam, Shamik Kundu, Arnab Raha, Suvadeep Banerjee, Suriya Natarajan and **Kanad Basu**. HardCompress: A Novel Hardware-based Low Power Compression Scheme for DNN Accelerators. At *International Symposium on Quality Electronic Design (ISQED)*, 2021.

[101] Ayesha Siddique, **Kanad Basu** and Khaza Anuarul Hoque. Exploring Fault-Energy Trade-offs in Approximate DNN Hardware Accelerators. *At International Symposium on Quality Electronic Design (ISQED)*, 2021.

[102] Shamik Kundu, Xingyu Meng and **Kanad Basu**. Application of Machine Learning in Hardware Trojan Detection. At *International Symposium on Quality Electronic Design (ISQED)*, 2021.

[103] Pandy Kalimathy, **Kanad Basu** and Benjamin Carrion Schaefer. Efficient Hierarchical Post-Silicon Validation and Debug. At *International Conference on VLSI Design (VLSID),* 2021. **(Honorable Mention Award)**

[104] Yug Pratap Singh, Abraham Kuruvila and **Kanad Basu**. Hardware-assisted Detection of Malware in Automotive-Based Systems. At Design, Automation and Test in Europe Conference (DATE), 2021.

[105] Abraham Kuruvila, Ayush Arunachalam and **Kanad Basu**. Benefits and Challenges of Utilizing Hardware Performance Counters for COPPA Violation Detection. At *IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE)*, 2020.

[106] M Meraj Ahmed, Abhijitt Dhavlle, Naseef Mansoor, Purab Sutradhar, Sai Manoj Pudukotai Dinakarrao, **Kanad Basu** and Amlan Ganguly. Defense against On-Chip Trojans Enabling Traffic Analysis Attacks. At *ACM Asian Hardware Oriented Security and Trust Symposium (AsianHOST),* 2020.

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[111] B.Kumar, S. Thakur, **K. Basu**, M. Fujita, V. Singh. A Low Overhead Methodology for Validating Memory Consistency Models in Chip Multiprocessors. At International Conference on VLSI Design (VLSID), 2020.

[112] Deepraj Soni, Mohammed Nabeel, **Kanad Basu**, and Ramesh Karri. Power, Area, Speed, and Security (PASS) Trade-offs of NIST PQC Signature Candidates Using a C to ASIC Design Flow. *IEEE International Conference on Computer Design (ICCD),* 2019.

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[114] **Kanad Basu,** Rana Elnaggar, Krishnendu Chakrabarty, and Ramesh Karri. Preempt: PReempting malware by Examining Embedded Processor Traces. *ACM/IEEE Design Automation Conference (DAC)*, 2019.

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[117] Sidhartha Sankar Rout, **Kanad Basu** and Sujay Deb. Efficient Post-Silicon Validation of Network-on-Chip using Wireless Links. *IEEE International Conference on VLSI Design (VLSID),* 2019.

[118] Jeff Zhang, Tianyu Gu, **Kanad Basu** and Siddharth Garg. Analyzing and mitigating the impact of permanent faults on a systolic array based neural network accelerator. *IEEE VLSI Test Symposium (VTS)*, 2018.

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[121] **Kanad Basu** and Shreyas Sen. Intelligent Sensor Nodes. *IEEE VLSI Test Symposium (VTS), 2018.*

[122] Ankit Jindal, Binod Kumar, **Kanad Basu**, and Masahiro Fujita. ELURA: A Methodology for Post-silicon Gate-level Error Localization using Regression Analysis. *IEEE International Conference on VLSI Design (VLSID)*, 2018.

[123] Binod Kumar, **Kanad Basu**, Masahiro Fujita and Virendra Singh. RTL Level Trace Signal Selection and Coverage Estimation During Post-Silicon Validation. *IEEE International High Level Design Validation and Test Workshop (HLDVT),* 2017.

[124] Binod Kumar, **Kanad Basu**, Ankit Jindal, Masahiro Fujita, and Virendra Singh. Improving post-silicon error detection with topological selection of trace signals. *IEEE/IFIP International Conference on Very Large Scale Integration (VLSI-SoC),* 2017.

[125] **Kanad Basu**, Rishi Kumar, Santosh Kulkarni and Rohit Kapoor. Deterministic Shift Power Reduction in Test Compression. *IEEE International Symopsium on VLSI Design and Test (VDAT)*, 2017.

[126] Binod Kumar**, Kanad Basu,** Ankit Jindal, Brajesh Pandey and Masahiro Fujita. A Formal Perspective on Effective Post-Silicon Debug and Trace Signal Selection**.** *IEEE International Symopsium on VLSI Design and Test (VDAT)*, 2017.

[127] Subhadip Kundu, **Kanad Basu** and Rohit Kapur. Observation-Point identification based on Signal Selection Methods for improving Diagnostic Resolution. *International Test Conference – India (ITC-India)*, 2017.

[128] **Kanad Basu,** Prabhat Mishra, Priyadarsan Patra, Amir Nahir, Allon Adir. Dynamic Selection of Trace Signals for Post-Silicon Debug. *International Workshop on Microprocessor Test and Verification (MTV),* 2013.

[129] **Kanad Basu,** Prabhat Mishra and Priyadarsan Patra. Observability-aware Directed Test Generation for Soft Errors and Crosstalk Faults. *IEEE International Conference on VLSI Design (VLSID),* 2013.

[130] **Kanad Basu**, Prabhat Mishra and Priyadarsan Patra. Constrained Signal Selection for Post Silicon Validation. *IEEE International High Level Design, Validation and Test Workshop (HLDVT),* 2012.

[131] **Kanad Basu,** Prabhat Mishra and Priyadarsan Patra. Efficient Combination of Trace and Scan Signals for Post-Silicon Validation and Debug. *IEEE International Test Conference (ITC),* 2011.

[132] **Kanad Basu** and Prabhat Mishra. Efficient Trace Data Compression using Statically Selected Dictionary**.** *IEEE VLSI Test Symposium (VTS),* 2011.

[133] **Kanad Basu** and Prabhat Mishra. Efficient Trace Signal Selection for Post Silicon Validation and Debug. *International Conference on VLSI Design (VLSID),* 2011 **(Best Paper Award).**

[134] **Kanad Basu** and Prabhat Mishra. A Novel Test-Data Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods. *ACM Great Lakes Symposium on VLSI (GLSVLSI),* 2008.

[135] **Kanad Basu,** Subhadip Paul and Prasun Roy. MRI-image based radiotherapy treatment optimization for brain tumors using stochastic approach. *3rd National Brain Research Center International Conference (NBRC),* 2007.

[136] Jishan Mehedi, **Kanad Basu,** Surendra Dalu and M. K. Naskar. A Novel Distributed Algorithm to maintain Connectivity with Fault-tolerant scheme in Mobile Ad-hoc Networks. *International Conference on Intelligent Systems and Networking (ICISN),* 2007.

[137] Ayan Banerjee, **Kanad Basu** and Aruna Chakraborty. Prediction of EEG Signals by Digital Filtering. *International Conference on Intelligent Systems and Networking (ICISN),* 2007.

[138] Samir Biswas, **Kanad Basu,** Avik Ray and M. K. Naskar. A Novel Distributed Algorithm to maintain Connectivity in Mobile Ad-hoc Networks. *Asian Mobile Computing Conference (AMCC),* 2007.

[139] Ayan Banerjee, **Kanad Basu** and Amit Konar. Designing a Real Time System for Car Number Detection using Discrete Hopfield Networks. *National Conference on Recent Trends in Information Systems (RETIS),* 2006.

[140] Avik Ray, **Kanad Basu,** Samir Biswas and M. K. Naskar. A Novel Distributed Algorithm for topology management in Mobile Ad-hoc Networks. *International Conference on Computers and Devices for Communication (CODEC),* 2006.

[141] S. Sen, A. Chatterjee, P. Bhattacharya, S. Das, **K. Basu** and A. Pal. Nanocrystalline MEMS Metal Oxide Gas Sensors for Underground Coal Mines. *International Conference on Resource Utilization and Intelligent Systems (INCRUIS),* 2006.

Patents:

[142] **Kanad Basu**, Raghu Gaurav Gopalakrishnasetty and Hari Krishnan Rajeev. Automatic test pattern generation (ATPG) considering crosstalk effects, US9218447B2, 2013.

[143] Prabhat Mishra, Seok-won Seong, **Kanad Basu**, Weixun Wang, Xiaoke Qin. Bitmaksk-based Code Compression Technique and Decompression Mechanism. Provisional Patent UF 12654, 2007.

Tutorial(s):

[144] **Kanad Basu** and Subhadip Kundu. Post-Silicon Validation and Diagnosis. *IEEE International Conference on VLSI Design*, 2016.

Thesis:

[145] **Chao Lu.** Enhancing the Power of Quantum Electronic Design Automation, 2024.

[146] **Shamik Kundu.** Towards Functional Safety in Deep Learning Hardware Accelerators. Doctoral Dissertation, University of Texas at Dallas, 2024.

[147] **Xingyu Meng.** Ensuring Hardware Robustness via Security Verification. Doctoral Dissertation, University of Texas at Dallas, 2023.

[148] **Ayush Arunachalam.** Towards synergizing AI and Hardware. Doctoral Dissertation, University of Texas at Dallas, 2023.

[149] Abraham Kuruvila. Hardware-assisted Malware Detection for Securing Embedded Systems. Doctoral Dissertation, University of Texas at Dallas, 2021.

[150] Kanad Basu. Efficient Techniques for Observability Enhancement during Post-Silicon Validation. Doctoral Dissertation, University of Florida, 2012.

[151] Kanad Basu. Simulation of radiotherapy treatment for brain tumors on MRI images. Bachelor's project, Jadavpur University, 2006.

Invited Talks and Presentations

Security: The Next Grand Challenge for Hardware Design 2020 - 2023
Invited talks at Army Research Lab Working Group Meeting, Iowa State University, IEEE Computer And Systems, Bangalore Chapter, India, University of California – Irvine, North Carolina State University, Purdue University, Southwest Research Institute, University of Illinois - Chicago, University of Buffalo, Indian Statistical Institute, Indian Institute of Science and Rochester Institute of Technology.

Fault-tolerant Hardware for ML 2023
Invited talk at International Functional Safety Conference, Rutgers University

Fault-tolerant Hardware for ML 2019
Invited talk at IEEE International Test Conference

Can Monitoring System State + Instruction Sequences aid Malware Detection? 2019
Presented at IEEE Asian Test Symposium

PREEMPT: PReempting Malware by Examining Embedded Processor Traces 2019
Presented at ACM/IEEE Design Automation Conference

High Level Synthesis (HLS) using Xilinx Vivado HLS tool. 2018
Guest lectures for the course: Advanced VHDL Design

Application of Hardware Performance Counters for malware detection. 2018
Seminar talk at NYU Center for Cybersecurity

A Technique for Electrical Error Localization with Learning Methods During Post-Silicon Debugging. 2018
Presented at IEEE International Conference on Green and Sustainable Computing.

Post-silicon validation: opportunities and challenges. 2017
Seminar talk at NYU Center for Cybersecurity.

RTL Level Trace Signal Selection and Coverage Estimation During Post-Silicon Validation. 2017
Presented at IEEE International High-Level Design Validation and Test Workshop.

Deterministic Shift Power Reduction in Test Compression. 2017
Presented at IEEE International Symposium on VLSI Design and Test.

A Formal Perspective on Effective Post-Silicon Debug and Trace Signal Selection. 2017
Presented at IEEE International Symposium on VLSI Design and Test.

Post-Silicon Validation and Diagnosis 2016
Tutorial talk at IEEE International Conference on VLSI Design.

Observability-aware Directed Test Generation for Soft Errors and Crosstalk Faults. 2013

Presented at IEEE International Conference on VLSI Design.

Efficient Combination of Trace and Scan Signals for Post-Silicon Validation and Debug. 2011
Presented at IEEE International Test Conference.

Efficient Trace Data Compression using Statically Selected Dictionary. 2011
Presented at IEEE VLSI Test Symposium.

A Novel Test-Data Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods. 2008
Presented at ACM Great Lakes Symposium on VLSI.

A Novel Distributed Algorithm to maintain Connectivity in Mobile Ad-hoc Networks. 2007
Presented at Asian Mobile Computing Conference.

Designing a Real Time System for Car Number Detection using Discrete Hopfield Networks.
Presented at National Conference on Recent Trends in Information Systems. 2006

A Novel Distributed Algorithm for topology management in Mobile Ad-hoc Networks 2006
Presented at 3rd International Conference on Computers and Devices for Communication.

Academic Services

Journal Editor	Associate Editor of IET Computer and Digital Technology (2018 – present). Associate Editor of IEEE Design and Test Journal (2022 – present). Guest Editor for Springer Journal of Electronic Testing (December 2019). Guest Editor for IEEE Journal on Emerging and Selected Topics in Circuits and Systems (July 2021).
PhD Committee Member	Jianqi Chen, Yunjie Zhang, Masoud Shahshahani, Sneha Thakur, Xuan Hu, Pratyay Chowdhury, Ria Ghosh, Qilin Si, Arian Azizi, Roshni Anna Jacob, Vineeth Amritur Niranjan (UT Dallas)
MS Committee Member	Sumanth Kumar Reddy Kotareddy, Md Shakil (UT Dallas)
PhD Examiner	External examiner of Dr. Hemanta Kumar Mondal, IIIT Delhi, India, 2017.
Departmental Committee	TA Committee (2019-2020); Graduate Admission Committee (CE) (2020-2021, 2023, 2024); PhD Committee (2022—2023); Faculty Hiring Committee (2024).
Track Chair	IEEE Design Automation Conference 2021, 2022
Program Co-Chair	IEEE Asian Test Symposium, 2024.
Finance Chair	IEEE VLSI Testing Symposium, 2024
Finance Co-chair	IEEE Computer Society Annual Symposium on VLSI 2021
Publication Chair	IEEE VLSI Testing Symposium 2021, 2022; International Symposium on LLM-aided Design, 2024.

Poster Chair	IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE) 2022, 2023 SRC TxACE Symposium 2022, 2023
Special Session Chair	IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems 2022. IEEE International Conference on Physical Assurance and Inspection of Electronics 2022. ACM Great Lakes Symposium on VLSI, 2024.
Technical Program Committee	IEEE Conference on Computer Design 2022, 2024. IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2024. IEEE International Conference on Computer Aided-Design, 2024. International Reliability Physics Symposium 2022, 2023, 2024. IEEE International Conference on Networking, Architecture, and Storage 2022. IEEE Design Automation Conference 2020, 2024. IEEE International Symposium on Quality of Electronic Design, 2024. IEEE Computer Society Annual Symposium on VLSI 2020. IEEE International Conference on VLSI Design 2015, 2018, 2019, 2020, 2021, 2023, 2024. IEEE High-Level Design, Verification and Trust Workshop 2018. IEEE Rapid System Prototyping Workshop 2016. IEEE International Symposium on Smart Electronics, 2018.
Organizing Committee Chair	IEEE International Symposium on Rapid System Prototyping, 2014.
Reviewer – Journal	IEEE Transactions on VLSI Systems, IEEE Design and Test of Computers, IEEE Transactions on Computer Aided Design, Journal of Circuit, Systems and Computers, IEEE Transactions on Dependable and Secure Computing, IEEE Transactions on Multi-Scale Computing.
Reviewer – Conference	ACM Design Automation Conference, IEEE International Conference on Computer-Aided Design, IEEE Design and Test in Europe Conference, Hardware Oriented Security and Trust Conference, IEEE International Test Conference, IEEE VLSI Test Symposium, IEEE Asian Test Symposium, IEEE European Test Symposium, IEEE International Conference on VLSI Design and ACM Great Lakes Symposium on VLSI, Asia and South Pacific Design Automation Conference.
Organizer	NYU Cybersecurity Awareness Week (CSAW) Applied Research Track, 2018. TxACE Symposium, 2022-2023.