LAB VIII. LOW FREQUENCY CHARACTERISTICS OF JUNCTION FIELD EFFECT TRANSISTORS

1. OBJECTIVE
In this lab, you will study the I-V characteristics and small-signal model of Junction Field Effect Transistors (JFET).

2. OVERVIEW
In this lab, we will study the I-V characteristics of JFET and we will investigate some techniques for developing equivalent circuit parameters in order to make a small-signal model of our JFET. You will compare the experimental results with the theoretical results of the equations found in the lab manual.

Information essential to your understanding of this lab:
1. Theoretical background of the JFET (Streetman 6.2)

Materials necessary for this Experiment:
1. Standard testing station
2. One JFET (Part: 2N5485)
3. 1kΩ resistor

3. BACKGROUND INFORMATION

3.1 CHART OF SYMBOLS
Here is a chart of symbols used in this lab manual. This list is not all inclusive; however, it does contain the most common symbols and their units.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Symbol Name</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{DS}$</td>
<td>total drain to source current</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DS}$</td>
<td>DC drain to source current</td>
<td>mA</td>
</tr>
<tr>
<td>$i_{ds}$</td>
<td>AC drain to source current</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>saturation current w/ $V_G = 0$</td>
<td>mA</td>
</tr>
<tr>
<td>$V_P$</td>
<td>pinch off Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>total drain to source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>DC drain to source Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$v_{ds}$</td>
<td>AC drain to source Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$v_{GS}$</td>
<td>total gate to source Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>DC gate to source Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$v'_{gs}$</td>
<td>AC gate to source Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$g_m$</td>
<td>transconductance</td>
<td>A/V</td>
</tr>
</tbody>
</table>

3.2 CHART OF EQUATIONS
All of the equations from the background portion of the manual are shown in the table below.
Table 2. Chart of the equations used in this lab.

<table>
<thead>
<tr>
<th>Equation</th>
<th>Name</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Saturation Drain to Source</td>
<td>$I_{D(Sat)} = I_{DSS} \left( 1 + \frac{V_{GS}}{V_p} \right)^2$ for negative $V_{GS}$</td>
</tr>
<tr>
<td>2</td>
<td>Transconductance at the</td>
<td>$g_m = \left( \frac{\partial i_D}{\partial V_{GS}} \right)<em>{V</em>{GS}=const} \left( \frac{\Delta I_D}{\Delta V_{GS}} \right)<em>{V</em>{GS}=const}$</td>
</tr>
<tr>
<td>3</td>
<td>Equation for Transconductance</td>
<td>$g_m = \left( -\frac{2I_{DSS}}{V_p} \right) \left( 1 + \frac{V_{GS}}{V_p} \right)$</td>
</tr>
<tr>
<td>4</td>
<td>Total Drain to Source</td>
<td>$i_{DSAT}(t) = I_{DS(0)} + I_{DSS} \left( \frac{v_{gs}}{V_p} \right)^2$ $- 2I_{DSS} \left( 1 + \frac{v_{gs}}{V_p} \right) \frac{v_{gs}}{V_p} \cos(wt) + \frac{I_{DSS}}{2} \left( \frac{v_{gs}}{V_p} \right)^2 \cos(2wt)$</td>
</tr>
<tr>
<td>5</td>
<td>Shift in DC operating point</td>
<td>$\Delta I_D = \frac{I_{DSS}}{2} \left( \frac{v_{gs}}{V_p} \right)^2$</td>
</tr>
</tbody>
</table>

3.3 THE I-V CHARACTERISTICS OF A JFET

In the JFET the transistor action is determined by the flow of majority carriers between the source and the drain. In the low drain-source bias region the current flow is controlled by a voltage applied to the gate terminal that consists of a reversed biased pn junction. The gate voltage modulates the width of the reverse biased pn junction depletion layer. The change in the cross-sectional area of the current path under the gate modulates the current flow. For a fixed source-drain voltage and with increasing gate bias the width of the depletion layer at the drain end of the channel decreases. The most important operating region of the JFET occurs at larger drain-source bias levels. There the combination of the applied gate voltage and the drain to source voltages are sufficiently large so the depletion width extends fully across the channel, pinching it off at the drain end of the channel. The current flow is now limited by the current flow in the non-pinched off region of the channel, and when the carriers reach the pinched off end they are rapidly collected by the reverse bias of the pinched off region. Analysis of the device geometry shows that in the pinched off region the current flow is determined by the value of the gate voltage, and is relatively independent of the drain-source voltage. This is the practical region for operating the JFET as an amplifier.

The DC behavior of a JFET is specified most completely by the output characteristics, $i_D$ versus $v_{DS}$, with $v_{GS}$ as a parameter, as shown in Figure 1, and the input-output characteristic, $i_{D(Sat)}$ versus $v_{GS}$, as shown in Figure 2. However, such detailed information is not always supplied by the device manufacturer, as is the case for the 2N5485 N-channel JFET used in this lab. In such circumstances the circuit designer must measure the device.
characteristics or use the limited information supplied by the manufacturer, consisting usually of the approximate values of $I_{DSS}$ and $V_P$.

2N 5485 n-channel JFET I-V characteristic

![Figure 1. 2N5485 JFET $I_{DS} - V_{DS}$ characteristics.](image1)

![Figure 2. Input-output characteristic ($i_{D(Sat.)}$ vs. $v_{GS}$) of a JFET.](image2)
When used as a small signal amplifier the JFET will be operating in the pinched-off mode, \( V_{DS} > |V_{GS} - V_p| > 0 \), and its DC behavior can be approximately described by the following equation

\[
I_{D(Sat)} = I_{DSS} \left( 1 + \frac{V_{GS}}{V_p} \right)^2 \quad \text{for negative } V_{GS}
\]  

(1)

Hence once you can extract information such as \( I_{DSS} \) and \( V_p \), you can use the JFET in a circuit. Often the values of \( I_{DSS} \) and \( V_p \) for a given type of transistor vary over wide ranges and the values supplied by the device manufacturer represent only the average and extreme values of these parameters. Moreover the device may not closely obey the relationship given by Eq. (1). In this experiment the DC characteristics of the transistor are measured in order to obtain sufficient information to use the device in an amplifier circuit and also to determine how closely Eq. (1) represents the actual device behavior.

### 3.4 SMALL SIGNAL MODELS

The small signal equivalent circuit of a JFET operating in the pinched-off mode is shown in Figure 3. The transconductance is \( g_m \) and is equal to the slope of the transfer curve in Figure 2 which is given by:

\[
g_m = \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{v_{ds}=\text{const}} = \left( \frac{\Delta I_D}{\Delta V_{GS}} \right)_{v_{ds}=\text{const}}
\]  

(2)

The Equation (2) can be rearranged as:

\[
g_m = \left( -\frac{2I_{DSS}}{V_p} \right) \left( 1 + \frac{V_{GS}}{V_p} \right)
\]  

(3)

\[\text{Figure 3. The small signal model of a JFET in the pinched off mode of operation.}\]

Equation (3) is evaluated at a fixed value \( V_{GS}=V_{GS} \). The input terminals from the gate to the source appear as a reversed biased diode and are an effective open circuit. The numerical value of \( g_m \) can be estimated from either Eq. (3) or from Figure 1. The latter approach will be used in this experiment. To find \( g_m \) from the characteristic curves of Figure 1, find the desired operating point \((i_D, v_{DS})\) that is determined by the load resistor and the drain supply voltage \( v_{DD} \). Then, draw a vertical line through the \( v_{DS} \) operating point. On this line find the voltage difference between the two nearby characteristic curves, \( \Delta V_{GS} \). Extrapolate the two intersection points to the y-axis and find \( \Delta i_{DS} \). Then use Eq. (2) to find \( g_m \).

The output resistance \( r_d \) shunting the \( g_m V_{GS} \) current generator is included in the model to account for changes in the drain current due to changes in \( v_{DS} \). The numerical value of \( r_d \)
can be obtained from the slope of the $I_D, V_{DS}$ curve above saturation in Fig. 1 or from a small signal AC measurement at the desired DC operating point. The value of $r_d$ is inversely proportional to the change in the DC value of the drain current. Use the following graphical analysis to obtain $r_d$. Find the characteristic curve closest to the operating point and draw a straight line superimposed on the saturation part of the curve. Select two convenient values of $v_{DS}$ and draw two vertical lines through these points to where they intersect the straight curve. Circle the intersection points. The $x$-axis separation gives the value $\Delta v_{DS}$. Next draw horizontal lines through the circles to the $y$-axis. The $y$-axis separation gives the value of $\Delta i_D$. The value of $r_d = (\Delta v_{DS}/\Delta i_D)$.

4. PRE-LAB REPORT

1. Study Figures 6-4 and 6-5 in Streetman and describe the I-V characteristics of a JFET.
   - Manually re-plot Figure 6-4 (do not scan it or copy it) and describe in your own words the variation of depletion regions and channel as voltage changes. Describe what pinch-off is. Identify the $V_p$ in the plot.
   - Manually re-plot Figure 6-5 (b) and identify $I_{DSS}$. In this plot, describe how to calculate $g_m$ in your own words.

5. PROCEDURE

Take special note of the absolute maximum ratings (operating range) of the JFET. These can be found on the first page of the data sheets appended to the end of this manual.

Construct the circuit shown in Figure 4.

![Circuit diagram](image)

**Figure 4.** Circuit diagram for the $I_{DS}$ vs. $V_{DS}$ characteristics measurement for the 2N5485 JFET.

Once the circuit has been built, open and execute the program “FETIVcurve.vi” using LabView to obtain a plot of the $I_{DS}$ vs. $V_{DS}$ characteristic similar to the one shown in Figure 1. This program allows you to set a start voltage for $V_{DS}$ and $V_{GS}$. It also allows you to set a step size for each of them. FETIVcurve.vi will start at the initial $V_{DS}$ and $V_{GS}$ voltages and then will step the $V_{DS}$ value from its initial value to its final value. After the computer reaches the final value of $V_{DS}$ at a fixed $V_{GS}$ then it will increment $V_{GS}$. This process will continue until the final values of both $V_{DS}$ and $V_{GS}$ are reached.
Set $V_{DS}$ to vary from 0.0 V to 20 V in 0.25 V steps. Let $V_{GS}$ vary from 0.0 V to -2.5 V in -0.25 V incremental steps. **If you accidentally put positive incremental values, you will blow up the transistor!** If your transistor fails, you must get another JFET and re-characterize another transistor. Save the JFET characteristics in your key memory.

Examine the graph that you now have displayed in the LabView window. Now examine Figure 1. Take note of the pinch off locus (dotted red line) on the left part of the graph. The locus passes through the point where the current flattens out at every value of $V_{GS}$. After you have visualized the pinch off locus for your graph, estimate the values for $V_{DS(Sat.)}$ and $I_{D(Sat.)}$ at the different gate voltages and determine $I_{DSS}$ and $V_{P}$ at $V_{GS} = 0.0$ V. Next, use Eq. (1) to calculate $I_{D(Sat.)}$ for $V_{GS} = 0$. Fill out the table below.

**Table 3.** Experimental values of $V_{DS(Sat.)}$, $I_{D(Sat.)}$, $g_m$, and $r_d$ and theoretical values of $I_{D(Sat.)}$.

<table>
<thead>
<tr>
<th>$V_{GS}$</th>
<th>$V_{DS(Sat.)}$(experimental)</th>
<th>$I_{D(Sat.)}$(experimental)</th>
<th>$I_{D(Sat.)}$(equation)</th>
<th>$g_m$</th>
<th>$r_d$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0 V</td>
<td>N/A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-0.5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-1.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>-1.5 V</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>-2.0 V</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>-2.5 V</td>
<td></td>
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</tr>
</tbody>
</table>

Now, plot $I_{D(Sat.)}$ vs. $V_{GS}$ curve in Excel using the experimental values in the table above. This plot should look similar to the Figure 2 and it shows JFET amplifier’s input-output ($v_{GS}$ - $i_D$) characteristic.

Suppose you use 2N5485 in an amplifier and assume that your operating point is at $v_{DS} = 8$ V. Find transconductance $g_m$ and fill out the table above. Read 3.4 in this manual to find out how to find $g_m$. You can also find $r_d$ in the small signal model using the I-V characteristics data. Find $r_d$ based on the method described in the 3.4 in this manual and fill out the table above.

6. **LAB REPORT**

- Write a summary of the summary of the experiment.
- **JFET output characteristics ($I_{DS}$ – $V_{DS}$)**
  - Plot the $I_{DS}$ vs. $V_{DS}$ characteristic. Show the pinch-off locus in the plot. Make sure both axes are labeled and the graph is appropriately titled.
  - Put the table 3 with experimental and theoretical data in it.
- **JFET input-output characteristics ($I_{D}$ – $V_{GS}$)**
  - Plot the $I_{D(Sat.)}$ vs. $V_{GS}$ curve. Plot both experimental and theoretical $I_{D(Sat.)}$ in the plot. Make sure both axes are labeled and the graph is appropriately titled.
  - Plot the $I_{DS}$ vs. $V_{DS}$ characteristic again and show how you use this plot to find $g_m$ and $r_d$ at a $v_{DS}$ equal to 8 V at the specified gate voltages.