Self-Aligned Gate Technology
Relevant References

4. “Self-Aligned Gate Process,” https://books.google.com/books?id=72Mkl80d-FMC&pg=PA15&lpg=PA15&dq=aluminum+gate+mos+process+bower&source=bl&ots=htRTQyCWq0&sig=pn8WMix8gnWk4-vQaiAunJyDMsc&hl=en&sa=X&ei=JXDIUZf7Jc_J0AHiiYGgBA&ved=0CE0Q6AEdwBA#v=onepage&q=aluminum%20gate%20mos%20process%20bower&f=false
• Aluminum Used to Generate Original MOSFET Gates
  ➢ Prevented Development of Self-Aligned Gates
  ➢ Aluminum Melts at 660 °C
  ➢ Diffusions and Anneals of Silicon Typically Require Around 1000 °C
    Causing Any Aluminum Present During Processing to Melt
  ➢ Therefore Must Form Source and Drain Prior to Forming the Gate
    Causing Misalignment of the Gate to the Source and Drain
  ➢ Must Increase Size of the Gate to Assure Overlap of the Gate to the
    Source and Drain
  ➢ This Gate Misalignment Also Caused Substantial Variability
• Using Highly Doped Polysilicon Permits Use of Self-Aligned Gates
  ➢ Heavy Doping of Polysilicon Generates Highly Conductive Gates Required to Form the Device
  ➢ Silicon Also Melts at 1414 °C
  ➢ Permits Gates to Be Generated Prior to Formation of Source and Drain
    - Permitted Source and Drain to Be Self-Aligned by Diffusion in Earlier Devices
    - Later Permitted Source and Drain to Be Self-Aligned by Ion Implantation Followed by the Requisite High Temperature Anneal to Activate Dopant and Remove Implant Damage in Later Devices
    - This Permitted the Gate to Be Self-Aligned to the Source and the Drain
Standard Aluminum Gate Process (Top) and Polysilicon Self-Aligned Gate (Bottom).
Generates Substantial Performance Benefits

- Substantially Reduced the Overlap Capacitance
- Further Reduced the Variability of the Overlap Capacitance Further Improving the Performance of the Device
- Also Reduced the Threshold Voltage of the PMOS Transistors Primarily Being Used in MOSFETs at That Time by 1.1 V
  - Workfunction Difference Between P-Doped Polysilicon Gate and the Substrate 1.1V Lower Than for Aluminum
  - Lowered Threshold Voltage by 1.1 V or 30%
  - Substantially Improved Performance of the Device
• **Performance Benefits**
  - Generated 3 to 5 Times Increase in Speed at Same Power Dissipation
  - Reduced Power by 3 to 5 Times at Same Speed
  - Substantially Reduced Variability in Device Performance
• Reduced Silicon Area and Cost by Approximately One Half
  - Gate Area Substantially Reduced by Smaller Gate
  - Polysilicon Used as Local Interconnect Increasing Routability and Reducing Area
  - Buried Contacts Whereby Polysilicon Could Make Direct Contact to Silicon Also Reduced the Area Although Ultimately Could Not Be Applied to CMOS
Self-Aligned Gate Also Substantially Improved Reliability

- Enabled Use of Phosphosilicate Glass, or PSG, Which Requires Higher Temperature Processing
- PSG Deposited After Devices Formed in Silicon Using Self-Aligned Gate
- Phosphorus Getters Alkali Ions at 1000 to 1100 °C Improving Reliability
- PSG Can Also Be Reflowed at 1000 to 1100 °C Smoothing Surface and Improving Step Coverage and Reducing Tendency of Al to Crack Improving Yield and Reliability
- Reduced Voltages Allowed by a Lower $V_T$ Also Reduced the Field Oxide Thickness Reducing Oxide Step Height and Improving Al Reliability
- Reliability Increased to Level of Bipolar Devices Then Dominant IC Technology
PSG Reflow Used to Both Getter Alkali Ions and Planarize the Oxide Deposited Over the Transistor at Contact Level
PSG Reflow Generated Across an Abrupt Step by Annealing at 1100 °C for 20 Minutes at a Phosphorus Concentration of (a) 0.0 wt% P; (b) 2.2 wt% P; (c) 4.6 wt% P; and (d) 7.2 wt% P.
Reflow of a Borophosphosilicate Glass, Improved Variant of PSG, Containing 5% B and 5% P for 30 Minutes in N₂ (a) Before Reflow; (b) After Reflow.
Actual Image of a Crack Generated in Al Deposited Across an Abrupt Step (Top) and Computer Simulation of Al Deposited Across a Similar Abrupt Step (Bottom)
• Drove Shift to MOSFET Devices by the Late 1970s
  - Bipolar Only Continued to Be Used in the Highest Speed Applications
  - Intel Continued to Use BiCMOS and IBM Pure Bipolar Until the Middle of the 1990s