"Converting MATLAB Algorithms to FPGA or ASIC Designs"

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In the DSP domain, MATLAB is the DSL of choice with 97% of DSP design implemented on dedicated DSP processors. MATLAB provides both an efficient system-level verification environment and an efficient path to implementation. Unfortunately, the process of converting MATLAB to "C" code to run on the processor is reaching its limits. A DSP processor's inherent limitation of serial operation is becoming a bottleneck for advanced high-performance algorithms. To solve this problem, a new methodology must be in place to convert algorithmic MATLAB to a register-transfer language (RTL) that can be used by industry-standard synthesis and verification tools. Companies that use the new methodology will benefit from greater productivity, both in terms of the domain-specific language and from the new breed of best-inclass tools they will enable.

This presentation will show the process of taking a MATLAB algorithm down to a silicon representation. It will demonstrate a design style and methodology for implementing this algorithm in either an FPGA or an ASIC.

As CTO and VP of Engineering, Michael Bohm oversees all product and technology development for AccelChip Inc. Bohm was most recently chief scientist and Technology Fellow for Mentor Graphics. Prior to this, he ran IC/ASIC development at Harris Semiconductor, where he worked closely with the founders of Synopsys. Bohm worked onsite at Synopsys/Cadence/Cross Creek as a Harris semiconductor employee from 1989 - 1991, where he contributed to the development of their Design Compiler technology. Bohm joined Mentor Graphics in 1991 and led the development of AutoLogic II. He later became VP and chief scientist at Exemplar. When Mentor Graphics folded Exemplar into the company, Bohm oversaw the technical development and direction of their HDL tool set for FPGA design.

More information on the Dallas Chapter of the IEEE Signal Processing Society available at http://www.utdallas.edu/~kehtar/ieee-sp-index.htm.