Electrical Engineering Colloquium
Dallas Chapter of IEEE Signal Processing Society Presents

Benchmarking Processors for DSP Applications

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Today, a growing range of applications - from telecom infrastructure equipment to PDAs - includes signal-processing tasks. The rapid growth of signal processing applications has motivated DSP processor vendors to introduce a slew of new processors. The expansion of signal-processing applications has also motivated vendors of general-purpose processors, FPGAs, and other types of processors to introduce processors with impressive signal-processing capabilities. These new options provide unprecedented freedom in selecting processors for signal-processing applications.

Choosing the right processor can make the difference between a product's success and failure. For example, signal-processing applications make heavy demands on processor performance, so system developers must be careful to choose a processor with adequate horsepower. Unfortunately, it can be difficult to assess which processor provides the best solution in terms of speed, cost, energy efficiency, and other considerations. And while the expanding array of architecture choices offers welcome freedom in choosing a processor, it also complicates the decision-making process. Sorting through the options can be a full-time job.

Performance evaluation can be particularly difficult for heterogeneous multiprocessors - that is, chips that contain two or more dissimilar processor cores. Evaluating this emerging class of processors requires an understanding of how the target application will be partitioned across the processor.

In this presentation, we examine and address the challenges of predicting processor performance for signal processing applications. We present several benchmarking approaches and highlight key strengths and weaknesses of each. We examine three approaches - algorithm kernel benchmarks, synthetic task benchmarks, and standards-based benchmarking - in detail. Next, we explain the limitations of benchmarking and the careful analysis required to apply results to a specific application. Finally, we explore ways to avoid common benchmarking pitfalls.

Jeff Bier is co-founder and President of Berkeley Design Technology, Inc. (BDTI). Mr. Bier oversees BDTI's benchmarking and competitive analysis of chips, tools, and other technology. He is a recognized industry expert, frequently presenting seminars on signal processing applications and technologies. He is also the editor of BDTI's respected technology analysis reports, including "Buyer's Guide to DSP Processors," now in its sixth edition, and the Editor-in-Chief of the "Inside DSP" series of quarterly supplements to EE Times. Mr. Bier earned B.S. and M.S. degrees from Princeton University and U.C. Berkeley.

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