C-based VLSI Design and Verification

2 Days Hands-on High-Level Synthesis Course

C-Based design has many advantages compared to traditional RTL design. Some of the advantages include the increase in design productivity, which allows design teams to meet the increasingly stringent time-to-market requirements. Second, the ability to create smaller designs compared to hand-coded RTL due to its ability to maximize resource sharing. Lastly the possibility of generating a set of micro-architectures with different area vs. performance trade-offs without having to modify the original behavioral description, also called Design Space Exploration (DSE) are some of them.

The University of Texas at Dallas, Department of Electrical and Computer Engineering (ECE) DARClab (Design Automation and Reconfigurable Computing) organizes this course.

This lab specializes in C-Based VLSI design for ASICs and FPGAs and has among other things released a SystemC Synthesizable Benchmark suite called S2CBench.

The main course instructor is Dr. Benjamin Carrion Schafer, who prior to joining PolyU worked at NEC Corporation as an R&D engineer for their commercial HLS tool CyberWorkBench and who was also responsible for the international training program. This course includes multiple topics covered at the training program.

Course Objectives

This course focuses on C-based design based on High-Level Synthesis, including how to verify these designs and co-verify legacy RTL blocks with newly developed C-based design processes. By the end of the course, the participants should be able to:

- Synthesize ANSI-C descriptions using state of the art commercial High-Level Synthesis tools;
- Convert behavioral Software (SW) descriptions (e.g. ANSI C) into synthesizable ANSI C descriptions, understanding the limitations;
- Differentiate between different scheduling modes (automatic, manual and pipeline mode) in order to be able to synthesize different types of applications i.e. data dominant, control dominant or controller circuits;

- Understand the different design techniques available to improve latency, area and delay in C-based VLSI designs;
- Verify C-based designs including: behavioral simulations, cycle-accurate simulations and RTL simulations using the golden inputs from the untimed behavioral description as inputs;
- Co-verify legacy RTL descriptions and new C-based behavioral descriptions;
- Perform manual and automatic Design Space Exploration (DSE);
- Prototype directly from ANSI-C to an FPGA board;
- Introduction to SystemC;
- Apply C-based hierarchical design methods, including functions, multiple processes and bus structures to synthesize complete HW systems.

Target Participants

This course is mainly targeted at HW designers who want to learn how to synthesize and verify behavioral descriptions given in ANSI-C into RTL. In particular, the following groups can benefit from this course:

- HW designers (ASIC or FPGA) currently following a traditional RTL-based VLSI Design methodology (VHDL or Verilog);
- SW engineers who want to accelerate computational intensive applications using FPGAs e.g. banking IT departments for low-latency trading or simulation acceleration;
- R&D engineers/scientists who are interested in new VLSI design methodologies;
- Students interested in deepening their knowledge into VLSI design;

Pre-requisites

Knowledge of ANSI-C or any high-level programming language is required. VLSI design experience (RTL Design: VHDL or Verilog) is desirable but not compulsory.

Course Structure

The course duration is two full days. In order to facilitate the participation of working professionals the course will take place over the weekend (Saturday and Sunday)

The course is predominantly practical. Each class will start describing the theoretical background needed and will then be followed by an extensive laboratory hands-on session. For the laboratory sessions, state of the art commercial Electronic Design Automation (EDA) tools will be used.

Contact Information

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