Benjamin Carrion Schaefer

Associate Professor
Department of Electrical and Computer Engineering
The University of Texas at Dallas
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EDUCATION

MBA, McGill University, Canada	2008 - 2010
Ph.D., Reconfigurable Computing, The University of Birmingham, UK	1999 - 2003
M.Sc., Microelectronics, Birmingham City University, UK	1998 - 1999
B.Eng., Electronic Engineering, Universidad Politecnica, Madrid, Spain	1993 - 1997

EMPLOYMENT HISTORY

Associate Professor, ECE dept., The University of Texas at Dallas	2022 - present
Assistant Professor, ECE dept., The University of Texas at Dallas	2016 - 2022
Assistant Professor, EIE dept., The Hong Kong Polytechnic University	2012 - 2016
Researcher, NEC Corp. Central R&D Laboratories, Japan	2007 - 2012
Postdoc, Seoul National University, Korea	2005 - 2007
Postdoc, University of California Los Angeles, USA	2003 - 2004

RESEARCH INTERESTS

Reconfigurable Computing, FPGAs, Electronic Design Automation (EDA), High-Level Synthesis (HLS), Hardware Security, Low-power design, Approximate Computing.

HONORS AND OTHER RECOGNITIONS

UT Dallas Erik Jonsson School of Engineering & Computer Science dean's fellow, 2022-2023
32^{nd} Great Lakes Symposium on VLSI (GLSVLSI) best paper award, 2022
UT Dallas Erik Jonsson School of Engineering & Computer Science best teacher award, 2022
34^{th} Int'l Conference on VLSI Design (VLSID) Naresh Malipeddy honorable mention award, 2021
Best program committee member in GLSVLSI symposium, 2018
Hack at DAC competition, third place, 2017
Brain Korean 21 (BK21) scholarship, Seoul, Korea, 2005
Interdisciplinary Research Fund scholarship, University of Birmingham, UK, 1999
MS.c. Birmingham City University, UK, awarded with distinction, 1999
GFTN Gesellschaft zur Förderung technischen Nachwuchses, Darmstadt, Germany, 1998

SCHOLARLY AND PROFESSIONAL SERVICE ACTIVITIES

Service within the University

Member, University Committee on Student Technology Requirements	2022 - 2023
Member, Staffing Committee	2022 - 2023
Member, CE Graduate Committee	2020 - 2021
Member, University Library Committee	2020 - 2021
Member, CE Graduate Committee	2019 - 2020
Member, University Library Committee	2019 - 2020
Member, Undergraduate Teaching Committee	2018 - 2019
Member, Staffing Committee	2018 - 2019
Member, Staffing Committee	2017 - 2018
Member, Undergraduate Teaching Committee	2016 - 2017

Journal Editorial Activities

Associate Editor, IEEE Transaction on Sustainable Computing	2022-present
Associate Editor, Integration, The VLSI Journal (Elsevier)	2014 - 2022

Conference Organization and Executive Committee

Track Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2024
Technical Program co-Chair, IEEE Dallas Circuits and Systems Conference (DCAS)	2023
Track Chair, IEEE International Conference on Computer Design (ICCD)	2022
Workshop co-chair, 7th Workshop on Approximate Computing (AxC22)	2022
Special Sessions Chair, IEEE Dallas Circuits and Systems Conference (DCAS)	2022
Track co-Chair, ACM/IEEE International Conference on CAD (ICCAD)	2021
Track Chair, ACM/IEEE Design Automation Conference (DAC)	2021
Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI)	2021
Track Chair, ACM/IEEE Design Automation Conference (DAC)	2020
Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI)	2020
Track Chair, ACM/IEEE Design Automation Conference (DAC)	2019
Track Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI)	2019
Local Arrangement Chair, IEEE Midwest Symposium on Circuits and Systems (MWSCAS)	2019
Conference Chair, ESLsyn conference	2014

Member of the Technical Program Committee

ACM Great Lakes Symposium on VLSI (GLSVLSI)	2023
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2023
ACM/IEEE International Conference on Computer Aided Design (ICCAD)(student competition)	2022
IEEE Conference on Field Programmable Gate Arrays (FPL)	2022
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2022
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2022
IEEE International Conference on Computer Design (ICCD)	2021
IEEE Transaction on Computers. TPC for special issue on Compiler Optimizations for FPGAs	2021
ACM/IEEE International Conference on Computer Aided Design (ICCAD)	2021
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2021
ACM/IEEE Design Automation Conference (DAC)	2021
IEEE Design Automation and Test Europe (DATE)	2021
IEEE Conference on Field Programmable Gate Arrays (FPL)	2021
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2021
ACM/IEEE International Conference on Computer Aided Design (ICCAD)	2020
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2020
ACM/IEEE Design Automation Conference (DAC)	2020
IEEE Design Automation and Test Europe (DATE)	2020
IEEE Conference on Field Programmable Gate Arrays (FPL)	2020
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2020
ACM/IEEE International Conference on Computer Aided Design (ICCAD)	2019
IEEE Application-Specific Systems, Architectures and Processors (ASAP)	2019
ACM/IEEE Design Automation Conference (DAC)	2019
ACM/IEEE Design Automation and Test Europe (DATE)	2019
IEEE Conference on Field Programmable Gate Arrays (FPL)	2019
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2019
IEEE Conference on Field Programmable Gate Arrays (FPL)	2018
ACM Great Lakes Symposium on VLSI (GLSVtextbfLSI)	2018
ACM/IEEE Design Automation Conference (DAC)	2018
IEEE Conference on Field Programmable Gate Arrays (FPL)	2018
ACM Great Lakes Symposium on VLSI (GLSVLSI)	2018
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2017

IEEE Conference on Field Programmable Gate Arrays (FPL)	2017
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2016
Electronic System Level Synthesis Conference (ESLSyn)	2015
ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)	2015
Electronic System Level Synthesis Conference (ESLSyn)	2014
Electronic System Level Synthesis Conference (ESLSyn)	2013

NSF Panel Reviewer

NSF GRFP Reviewer	2022
NSF Ad-Hoc Reviewer	2021
NSF GRFP Reviewer	2021
NSF GRFP Reviewer	2019

External PhD Reviewer

Columbia University, USA	2022
Universidad Politecnica de Madrid, Spain	2021
Universidad Politecnica de Madrid, Spain	2020
Visvesvaraya Technological University (VTU), India	2018

ACHIEVEMENTS IN ORIGINAL INVESTIGATION

Total: 130 Publications (36 Journals, 90 Conferences, 1 Book and 3 Book chapters)
First author: 35 Publications (17 Journals, 16 Conferences,1 Book and 1 Book chapter)

Journals

[1] Md. Imtiaz Rashid and **B. Carrion Schafer**, "Fast and Inexpensive High-Level Synthesis Design Space Exploration : Machine Learning to the Rescue," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–13, 2023.

[2] Q. Si, P. Chowdhury, R. Sreekumar, and **B. Carrion Schafer**, "Application Specific Approximate Behavioral Processor," *IEEE Transactions on Sustainable Computing*, pp. 1–15, 2022.

[3] P. Goswami , **B. Carrion Schafer** and D. Bhatia, "Machine learning based fast and accurate high level synthesis design space exploration: From graph to synthesis," *Integration*, vol. 88, pp. 116–124, 2022.

[4] Z. Wang and **B. Carrion Schafer**, "Learning from the past: Efficient high-level synthesis design space exploration for fpgas," *ACM TODAES*, vol. 27, no. 4, pp. 1–23, Jul. 2022.

[5] Z. Wang, F. Lau, and **B. Carrion Schafer**, "SSSL: Secure Search Space Locking of Behavioral IPs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–10, 2021.

[6] Q. Si, S. Shetty, and **B. Carrion Schafer**, "Building Complete Heterogeneous Systems-on-Chip in C: From Hardware Accelerators to CPUs," *MDPI Electronics*, pp. 1–15, 2021.

[7] P. Chowdhury and **B. Carrion Schafer**, "Leveraging automatic high-level synthesis resource sharing to maximize dynamical voltage overscaling with error control," *ACM TODAES*, pp. 1–13, 2021.

[8] A. Yadav, S. Xu, **B. Carrion Schafer**, and A. Davoudi, "Hardware-assisted Simulation of Voltage-behind-reactance Models of Electric Machines on FPGA," *IEEE Transactions on Energy Conversion*, pp. 1–10, 2020.

[9] S. Liu, F. Lau, and **B. Carrion Schafer**, "Predictive compositional method to design and re-optimize complex behavioral dataflows," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–12, 2020.

[10] **B. Carrion Schafer** and Z. Wang, "High-level synthesis design space exploration: Past, present and future," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–12, 2020.

[11] S. Xu *et al.*, "Design space exploration of heterogeneous mpsocs with variable number of hardware accelerators," *Microprocessors and Microsystems*, vol. 65, pp. 169–179, 2019.

[12] S. Xu and **B. Carrion Schafer**, "Toward self-tunable approximate computing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 4, pp. 778–789, Apr. 2019.

[13] D. Aledo, **B. Carrion Schafer**, and F. Moreno, "Vhdl vs. systemc: Design of highly parameterizable artificial neural networks," *IEICE Transactions on Information and Systems*, vol. E102.D, no. 3, pp. 512–521, 2019.

[14] A. Mahapatra and **B. Carrion Schafer**, "Veriintel2c: Abstracting rtl to c to maximize high-level synthesis design space exploration," *Integration*, vol. 64, pp. 1–12, 2019.

[15] J. N. Randall *et al.*, "Highly parallel scanning tunneling microscope based hydrogen depassivation lithography," *Journal of Vacuum Science & Technology B*, vol. 36, no. 6, 06JL05, 2018.

[16] A. Mahapatra, Y. Liu, and **B. Carrion Schafer**, "Accelerating cycle-accurate system-level simulations through behavioral templates," *Integration*, vol. 62, pp. 282–291, 2018.

[17] S. Xu and **B. Carrion Schafer**, "Exposing approximate computing optimizations at different levels: From behavioral to gate-level," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 11, pp. 3077–3088, Nov. 2017.

[18] N. Veeranna and **B. Carrion Schafer**, "S3cbench: Synthesizable security systemc benchmarks for high-level synthesis," *J. Hardware and Systems Security*, vol. 1, no. 2, pp. 103–113, 2017.

[19] N. Veeranna and **B. Carrion Schafer**, "Trust filter: Runtime hardware trojan detection in behavioral mpsocs," *J. Hardware and Systems Security*, vol. 1, no. 1, pp. 56–67, 2017.

[20] **B. Carrion Schafer**, "Parallel high-level synthesis design space exploration for behavioral ips of exact latencies," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 22, no. 4, May 2017.

[21] **B. Carrion Schafer**, "Enabling high-level synthesis resource sharing design space exploration in fpgas through automatic internal bitwidth adjustments," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 1, pp. 97–105, Jan. 2017.

[22] N. Veeranna and **B. Carrion Schafer**, "Hardware trojan detection in behavioral intellectual properties (ip's) using property checking techniques," *IEEE Transactions on Emerging Topics in Computing*, vol. 5, no. 4, pp. 576–585, Oct. 2017.

[23] **B. Carrion Schafer**, "Probabilistic multi-knob high-level synthesis design space exploration acceleration," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 3, pp. 394–406, Mar. 2016.

[24] **B. Carrion Schafer**, "Tunable multiprocess mapping on coarse-grain reconfigurable architectures with dynamic frequency control," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 1, pp. 324–328, Jan. 2016.

[25] **B. Carrion Schafer**, "Source code error detection in high-level synthesis functional verification," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 1, pp. 301–312, Jan. 2016.

[26] **B. Carrion Schafer**, "Hierarchical high-level synthesis design space exploration with incremental exploration support," *IEEE Embedded Systems Letters*, vol. 7, no. 2, pp. 51–54, Jun. 2015.

[27] **B. Carrion Schafer** and A. Mahapatra, "S2cbench: Synthesizable systemc benchmark suite for high-level synthesis," *IEEE Embedded Systems Letters*, vol. 6, no. 3, pp. 53–56, Sep. 2014.

[28] **B. Carrion Schafer** and K. Wakabayashi, "Machine learning predictive modelling high-level synthesis design space exploration," *IET Computers Digital Techniques*, vol. 6, no. 3, pp. 153–159, May 2012.

[29] **B. Carrion Schafer** and K. Wakabayashi, "Divide and conquer high-level synthesis design space exploration," *ACM TODAES*, vol. 17, no. 3, 29:1–29:19, Jul. 2012.

[30] **B. Carrion Schafer** and K. Wakabayashi, "Precision tunable rtl macro-modelling cycle-accurate power estimation," *IET Computers Digital Techniques*, vol. 5, no. 2, pp. 95–103, Mar. 2011.

[31] **Benjamin Carrion Schafer** and M. Sarrafzadeh, "Semi-automatic control unit generationfor complex vlsi designs," *IPSJ Transactions on System LSI Design Methodology*, vol. 5, no. 4, pp. 234–243, 2010.

[32] **Benjamin Carrion Schafer**, Y. Iguchi, W. Takahashi, S. Nagatani, and K. Wakabayashi, "Fixed point data type modeling for high level synthesis," *IEICE Transactions on Electronics*, vol. E93.C, no. 3, pp. 361–368, 2010.

[33] **B. Carrion Schafer** and K. Wakabayashi, "Design space exploration acceleration through operation clustering," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 1, pp. 153–157, Jan. 2010.

[34] **B. Carrion Schafer** and T. Kim, "Autonomous temperature control technique in vlsi circuits through logic replication," *IET Computers Digital Techniques*, vol. 3, no. 1, pp. 62–71, Jan. 2009.

[35] **B. Carrion Schafer** and T. Kim, "Hotspots elimination and temperature flattening in vlsi circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 16, no. 11, pp. 1475–1487, Nov. 2008.

[36] **B. Carrion Schafer**, S. F. Quigley, and A. H. Chan, "Acceleration of the Discrete Element Method (DEM) on a reconfigurable co-processor," *Computers and Structures*, vol. 82, no. 20, pp. 1707–1718, 2004.

Conference Papers

[1] Qilin Si and **B. Carrion Schafer**, "PEPA: Performance Enhancement of Embedded Processors through HW Accelerator Resource Sharing," in *Great Lakes Symposium on VLSI*, ser. GLSVLSI'23, Association for Computing Machinery, 2023, pp. 1–6.

[2] Qilin Si and **B. Carrion Schafer**, "Advice: Automatic design and optimization of behavioral application specific processors," in *Great Lakes Symposium on VLSI*, ser. GLSVLSI'23, Association for Computing Machinery, 2023, pp. 1–6.

[3] Md Imtiaz Rashid, A.H. Torabi and **B. Carrion Schafer**, "Certify: Automatic measuring the quality of high-level synthesis," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2023, pp. 1–5.

[4] M. Imtiaz and **B. Carrion Schafer**, "MIRROR: MaxImizing the Re-usability of RTL thrOugh RTL to C CompileR," in *Design, Automation, and Test in Europe (DATE)*, Mar. 2023, pp. 1–6.

[5] C. Sathe, Y. Makris, and **B. Carrion Schafer**, "MANTIS: Machine Learning-Based Approximate ModeliNg of RedacTed Integrated CircuitS," in *Design, Automation, and Test in Europe (DATE)*, Mar. 2023, pp. 1–6.

[6] A. H. Md I. Rashid and **B. Carrion Schafer**, "Automatic modernization of hardware assets," in *GOMACTech*, 2023, pp. 1–5.

[7] C. S. Md I. Rashid and **B. Carrion Schafer**, "Rope: Re-usability lock of behavioral intellectual property," in *GOMACTech*, 2023, pp. 1–5.

[8] P. Chowdhury, Jorge Castro Godinez, and **B. Carrion Schafer**, "Approximating HWAccelerators through Partial Extractions onto shared Artificial Neural Networks," in *Asia and South Pacific Design Automation (ASP-DAC)*, Jan. 2023, pp. 1–6.

[9] P. Chowdhury, C.G. Sathe, **B. Carrion Schafer**, "Predictive model attack for embedded fpga logic locking," in *International Symposium on Low Power Electronics and Design (ISLPED)*, ser. ISLPED '22, ACM/IEEE, 2022, pp. 1–6.

[10] C.G. Sathe, Y. Makris and **B. Carrion Schafer**, "Investigating the effect of different efpgas fabrics on logic locking through hw redaction," in *Dallas Circuits and Systems Conference (DCAS)*, ser. DCAS'22, IEEE, 2022, pp. 1–6.

[11] Q. Si and **B. Carrion Schafer**, "Optimizing behavioral near on-chip memory computing systems," in *International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, ser. ASAP'22, IEEE, 2022, pp. 1–7.

[12] Md Imtiaz Rashid and **B. Carrion Schafer**, "Fast parallel high-level synthesis design space explorer: Targeting fpgas to accelerate asic exploration," in *Great Lakes Symposium on VLSI **(Best Paper Award)***, ser. GLSVLSI '22, Association for Computing Machinery, 2022, pp. 1–6.

[13] Md Imtiaz Rashid, Qilin Si and **B. Carrion Schafer**, "Modernizing hardware circuits through high-level synthesis," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2022, pp. 1–5.

[14] **B. Carrion Schafer**, "Hotspot Mitigation through Multi-Row Thermal-aware Re-Placement of Logic Cells based on High-Level Synthesis Scheduling," in *Asia and South Pacific Design Automation (ASP-DAC)*, Jan. 2022, pp. 1–6.

[15] M. I. Rashid and **B. Carrion Schafer**, "Improving the Quality of Hardware Accelerators through automatic Behavioral Input Language Conversion in HLS," in *Asia and South Pacific Design Automation (ASP-DAC)*, Jan. 2022, pp. 1–6.

[16] Z. Wang, S. O. Mohammed, Y. Makris and **B. Carrion Schafer**, "Functional Locking through Omission: From HLS to Obfuscated Design," in *IEEE 39th International Conference on Computer Design (ICCD)*, Nov. 2021, pp. 1–8.

[17] P. Chowdhury and **B. Carrion Schafer**, "ADAPT: ANN-ControlleD System-Level Runtime Adaptable APproximate CompuTing," in *IEEE 39th International Conference on Computer Design (ICCD)*, Nov. 2021, pp. 1–4, (invited paper).

[18] P. Chowdhury and **B. Carrion Schafer**, "Beacon : Best approximations for complete behavioral heterogeneous socs," in *International Symposium on Low Power Electronics and Design (ISLPED)*, ser. ISLPED '21, ACM/IEEE, 2021, pp. 1–6.

[19] Q. Si, I. Rashid, and **B. Carrion Schafer**, "Micro-architecture tuning for dynamic frequency scaling in coarse-grain runtime reconfigurable arrays with adaptive clock domain support," in *IEEE Computer Society Annual Symposium on VLSI*, ser. ISVLSI '21, IEEE, 2021, pp. 1–6.

[20] P. Chowdhury and **B. Carrion Schafer**, "Unlocking approximations through selective source code transformations," in *Great Lakes Symposium on VLSI*, ser. GLSVLSI '21, Association for Computing Machinery, 2021, pp. 1–6.

[21] S. Shetty and **B. Carrion Schafer**, "Enabling the design of behavioral systems-on-chip," in *ACM/IEEE Design Automation Conference (DAC)*, Jul. 2021, pp. 1–6.

[22] Z. Zhu and **B. Carrion Schafer**, "Reducing the complexity of fault-tolerant system amenable to approximate computing," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2021, pp. 1–5.

[23] Y. Gao and **B. Carrion Schafer**, "Effective high-level synthesis design space exploration through a novel cost function formulation," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2021, pp. 1–5.

[24] P. Kalimuthu, K. Basu, and **B. Carrion Schafer**, "Efficient Hierarchical Post-Silicon Validation and Debug," in *International Conference on VLSI Design (VLSID) **(Honorable Mention Award)***, Feb. 2021, pp. 1–6.

[25] J. Chen and **B. Carrion Schafer**, "Watermarking of Behavioral IPs: A Practical Approach," in *Design, Automation, and Test in Europe (DATE)*, Feb. 2021, pp. 1–4.

[26] Z. Wang and **B. Carrion Schafer**, "Locking the Re-usability of Behavioral IPs: Discriminating the Search Space through Partial Encryptions," in *Design, Automation, and Test in Europe (DATE)*, Feb. 2021, pp. 1–4.

[27] J. Chen and **B. Carrion Schafer**, "Area Efficient Functional Locking through Coarse Grained Runtime Reconfigurable Architectures," in *Asia and South Pacific Design Automation (ASP-DAC)*, Jan. 2021, pp. 1–6.

[28] M. Shah and **B. Carrion Schafer**, "Flexible runtime reconfigurable computing overlay architecture and optimization for dataflow applications," in *Hierarchical Parallelism for Exascale Computing (HiPar)*, Nov. 2020, pp. 1–6.

[29] R. Sreekumar, P. Chowdhury, and **B. Carrion Schafer**, "Bespoke approximate behavioral processors," in *IEEE 38th International Conference on Computer Design (ICCD)*, Nov. 2020, pp. 1–4.

[30] A. Balachandran and **B. Carrion Schafer**, "Efficient functional locking of behavioral ips," in *IEEE International Midwest Symposium on Circuits and Systems (MWCAS)*, Aug. 2020, pp. 1–4.

[31] Z. Wang and **B. Carrion Schafer**, "Machine learning to set meta-heuristic specific parameters for high-level synthesis design space exploration," in *ACM/IEEE Design Automation Conference (DAC)*, Jul. 2020, pp. 1–6.

[32] J. Chen, M. Zaman, Y. Makris, S. Blanton, S. Mitra, and **B. Carrion Schafer**, "Decoy: Deflection-driven hls-based computation partitioning for obfuscating intellectual property," in *ACM/IEEE Design Automation Conference (DAC)*, Jul. 2020, pp. 1–6.

[33] Z. Zhu and **B. Carrion Schafer**, "Light-weight soft-errors detection mechanism in high-level synthesis," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2020, pp. 1–5.

[34] M. M. Shihab *et al.*, "A transistor-level fabric for design obfuscation," in *GOMACTech*, Mar. 2020, pp. 1–4.

[35] Z. Wang, J. Chen, and **B. Carrion Schafer**, "Efficient and robust high-level synthesis design space exploration through offline micro-kernels pre-characterization," in *Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2020, pp. 1–6.

[36] B. Hu, M. Shihab, W. Swartz, Y. Makris, **B. Carrion Schafer**, and C. Sechen, "Oan efficient milp-based aging-aware floorplanner for multi-context coarse-grained runtime reconfigurable fpgas," in *2020 Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2020, pp. 1–6.

[37] S. Xu and **B. Carrion Schafer**, "On the design of high performance hw accelerator through high-level synthesis scheduling approximations," in *Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2020, pp. 1–6.

[38] B. Hu, M. Shihab, W. Swartz, Y. B. C. S. Makris, and C. Sechen, "Extending the lifetime of coarse-grained runtime reconfigurable fpgas by balancing processing element usage," in *International Conference on Field-Programmable Technology (FPT)*, Dec. 2019.

[39] F. Taher, A. Balajandran, and **B. Carrion Schafer**, "Learning-based diversity estimation: Leveraging the power of high-level synthesis," in *IEEE 37th International Conference on Computer Design (ICCD)*, Nov. 2019.

[40] J. Chen and **B. Carrion Schafer**, "Low power design through frequency-optimized runtime micro-architectural adaptation," in *IEEE 37th International Conference on Computer Design (ICCD)*, Nov. 2019.

[41] J. Chen and **B. Carrion Schafer**, "Exploiting the benefits of high-level synthesis for thermal-aware vlsi design," in *IEEE 37th International Conference on Computer Design (ICCD)*, Nov. 2019.

[42] S. Xu and **B. Carrion Schafer**, "Low power design of runtime reconfigurable fpgas through contexts approximations," in *IEEE 37th International Conference on Computer Design (ICCD)*, Nov. 2019.

[43] S. Xu and **B. Carrion Schafer**, "Approximating behavioral hw accelerators through selective partial extractions onto synthesizable predictive models," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2019, pp. 1–8.

[44] M. R. Babu, F. N. Taher, A. Balachandran, and **B. Carrion Schafer**, "Efficient hardware acceleration for design diversity calculation to mitigate common mode failures," in *IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Apr. 2019, pp. 267–270.

[45] J. Chen and **B. Carrion Schafer**, "Thermal fingerprinting of fpga designs through high-level synthesis," in *Great Lakes Symposium on VLSI*, ser. GLSVLSI '19, Tysons Corner, VA, USA: Association for Computing Machinery, 2019, pp. 331–334.

[46] Z. Zhu, F. N. Taher, and **B. Carrion Schafer**, "Exploring design trade-offs in fault-tolerant behavioral hardware accelerators," in *Great Lakes Symposium on VLSI*, ser. GLSVLSI '19, Tysons Corner, VA, USA: Association for Computing Machinery, 2019, pp. 291–294.

[47] B. Hu *et al.*, "Functional obfuscation of hardware accelerators through selective partial design extraction onto an embedded fpga," in *Great Lakes Symposium on VLSI*, ser. GLSVLSI '19, Tysons Corner, VA, USA: Association for Computing Machinery, 2019, pp. 171–176.

[48] S. Liu, F. C. Lau, and **B. Carrion Schafer**, "Accelerating fpga prototyping through predictive model-based hls design space exploration," in *56th ACM/IEEE Design Automation Conference (DAC)*, Jun. 2019, pp. 1–6.

[49] A. Mahapatra and **B. Carrion Schafer**, "Optimizing rtl to c abstraction methodologies to improve hls design space exploration," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–5.

[50] Z. Wang and **B. Carrion Schafer**, "Partial encryption of behavioral ips to selectively control the design space in high-level synthesis," in *Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2019, pp. 642–645.

[51] M. M. Shihab *et al.*, "Design obfuscation through selective post-fabrication transistor-level programming," in *Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2019, pp. 528–533.

[52] F. N. Taher, M. Joslin, A. Balachandran, Z. Zhu, and **B. Carrion Schafer**, "Common-mode failure mitigation: Increasing diversity through high-level synthesis," in *Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2019, pp. 1563–1566.

[53] Z. Zhu, J. Callenes-Sloan, and **B. Carrion Schafer**, "Control flow checking optimization based on regular patterns analysis," in *IEEE 23rd Pacific Rim International Symposium on Dependable Computing (PRDC)*, Dec. 2018, pp. 203–212.

[54] S. Xu and **B. Carrion Schafer**, "Deep: Dedicated energy-efficient approximation for dynamically reconfigurable architectures," in *IEEE 36th International Conference on Computer Design (ICCD)*, Oct. 2018, pp. 587–594.

[55] S. Xu and **B. Carrion Schafer**, "Autonomous temperature management through selective control of exact-approximate tiles," in *IEEE 36th International Conference on Computer Design (ICCD)*, Oct. 2018, pp. 346–349.

[56] F. N. Taher, M. Kishani, and **B. Carrion Schafer**, "Design and optimization of reliable hardware accelerators: Leveraging the advantages of high-level synthesis," in *IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS)*, Jul. 2018, pp. 232–235.

[57] S. Liu, F. Lau, and **B. Carrion Schafer**, "Investigation and optimization of pin multiplexing in high-level synthesis," in *Great Lakes Symposium on VLSI*, ser. GLSVLSI '18, Chicago, IL, USA: Association for Computing Machinery, 2018, pp. 427–430.

[58] F. N. Taher, J. Callenes-Sloan, and **B. Carrion Schafer**, "A machine learning based hard fault recuperation model for approximate hardware accelerators," in *55th Annual Design Automation Conference*, ser. DAC '18, San Francisco, California: Association for Computing Machinery, 2018.

[59] S. Xu, J. Chen, and **B. Carrion Schafer**, "Hw/sw co-design experimental framework using configurable socs," in *International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, Dec. 2017, pp. 1–6.

[60] S. Xu, **B. Carrion Schafer**, and Y. Liu, "Configurable soc in-situ hardware/software co-design design space exploration," in *IEEE International Conference on Computer Design (ICCD)*, Nov. 2017, pp. 509–512.

[61] S. Xu and **B. Carrion Schafer**, "Approximate reconfigurable hardware accelerators: Adapting the micro-architecture to dynamic workloads," in *IEEE International Conference on Computer Design (ICCD)*, Nov. 2017, pp. 1–7.

[62] S. Liu and **B. Carrion Schafer**, "Learning-based interconnect-aware dataflow accelerator optimization," in *27th International Conference on Field Programmable Logic and Applications (FPL)*, Sep. 2017, pp. 1–7.

[63] **B. Carrion Schafer**, D. Aledo, and F. Moreno, "Application specific behavioral synthesis design space exploration: Artificial neural networks. A case study," in *Euromicro Conference on Digital System Design, DSD*, 2017, pp. 129–136.

[64] Y. Liu, M. Villaverde, F. Moreno, and **B. Carrion Schafer**, "Characterization and optimization of behavioral hardware accelerators in heterogeneous mpsocs," in *12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*, Jul. 2017, pp. 1–8.

[65] M. Yasin, A. Sengupta, B. C. S. Schafer, Y. Makris, O. Sinanoglu, and J. (Rajendran, "What to lock? functional and parametric locking," in *Great Lakes Symposium on VLSI 2017*, ser. GLSVLSI '17, Banff, Alberta, Canada: Association for Computing Machinery, 2017, pp. 351–356.

[66] N. Veeranna and **B. Carrion Schafer**, "Efficient behavioral intellectual properties source code obfuscation for high-level synthesis," in *2017 18th IEEE Latin American Test Symposium (LATS)*, Mar. 2017, pp. 1–6.

[67] N. Veeranna and **B. Carrion Schafer**, "Hardware trojan avoidance and detection for dynamically re-configurable fpgas," in *International Conference on Field-Programmable Technology (FPT)*, Dec. 2016, pp. 193–196.

[68] Dong Liu and **B. Carrion Schafer**, "Efficient and reliable high-level synthesis design space explorer for fpgas," in *26th International Conference on Field Programmable Logic and Applications (FPL)*, Aug. 2016, pp. 1–8.

[69] A. Balachandran, N. Veeranna, and **B. Carrion Schafer**, "On time redundancy of fault tolerant c-based mpsocs," in *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Jul. 2016, pp. 631–636.

[70] Y. Liu and **B. Carrion Schafer**, "Optimization of behavioral ips in multi-processor system-on-chips," in *21st Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2016, pp. 336–341.

[71] I. Llamas-Garro *et al.*, "Recent trends and considerations for high speed data in chips and system interconnects," in *SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC)*, Nov. 2015, pp. 1–6.

[72] X. Li and **B. Carrion Schafer**, "Temperature-triggered behavioral ips hw trojan detection method with fpgas," in *25th International Conference on Field Programmable Logic and Applications (FPL)*, Sep. 2015, pp. 1–4.

[73] Y. Liu and **B. Carrion Schafer**, "Adaptive combined macro and micro-exploration of concurrent applications mapped on shared bus reconfigurable soc," in *Electronic System Level Synthesis Conference (ESLsyn)*, Jun. 2015, pp. 11–16.

[74] **B. Carrion Schafer**, "Process selection for maximum resource sharing in high-level synthesis," in *Electronic System Level Synthesis Conference (ESLsyn)*, Jun. 2015, pp. 35–40.

[75] Y. Liu and **B. Carrion Schafer**, "Hw acceleration of multiple applications on a single fpga," in *International Conference on Field-Programmable Technology (FPT)*, Dec. 2014, pp. 284–285.

[76] **B. Carrion Schafer**, "Time sharing of runtime coarse-grain reconfigurable architectures processing elements in multi-process systems," in *International Conference on Field-Programmable Technology (FPT)*, Dec. 2014, pp. 76–82.

[77] A. Mahapatra and **B. Carrion Schafer**, "Machine-learning based simulated annealer method for high level synthesis design space exploration," in *Proceedings of the 2014 Electronic System Level Synthesis Conference (ESLsyn)*, May 2014, pp. 1–6.

[78] **B. Carrion Schafer**, "Allocation of fpga dsp-macros in multi-process high-level synthesis systems," in *19th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2014, pp. 616–621.

[79] **B. Carrion Schafer**, "Automatic partitioning of behavioral descriptions for high-level synthesis with multiple internal throughputs," in *Electronic System Level Synthesis Conference (ESLsyn)*, May 2013, pp. 1–6.

[80] S. Golshan, E. Bozorgzadeh, **B. Carrion Schafer**, K. Wakabayashi, H. Homayoun, and A. Veidenbaum, "Exploiting power budgeting in thermal-aware dynamic placement for reconfigurable systems," in *Proceedings of the 16th ACM/IEEE International Symposium on Low Power Electronics and Design*, ser. ISLPED 2010, Austin, Texas, USA: ACM, 2010, pp. 49–54.

[81] **B. Carrion Schafer**, A. Trambadia, and K. Wakabayashi, "Design of complex image processing systems in esl," in *Asia and South Pacific Design Automation Conference (ASPDAC)*, IEEE, 2010, pp. 809–814.

[82] **B. Carrion Schafer**, Takashi Takenaka, and Kazutoshi Wakabayashi, "Adaptive simulated annealer for high level synthesis design space exploration," in *2009 International Symposium on VLSI Design, Automation and Test*, Apr. 2009, pp. 106–109.

[83] **B. Carrion Schafer**, Y. Lee, and T. Kim, "Temperature-aware compilation for vliwprocessors," in *13th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2007)*, Aug. 2007, pp. 426–431.

[84] **B. Carrion Schafer** and T. Kim, "Thermal-aware instruction assignment for vliw processors," in *11th Workship on Interaction between Compilers and Computer Architectures (INTERACT-11))*, Feb. 2007.

[85] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan, "Scalable implementation of the discrete element method on a reconfigurable computing platform," in *Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream*, Berlin, Heidelberg: Springer Berlin Heidelberg, 2002, pp. 925–934.

[86] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan, "Implementation of the discrete element method using reconfigurable computing (fpgas)," in *15th Engineering Mechanics Conference (EM2002)*, 2002.

[87] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan, "Analysis and implementation of the discrete element method using a dedicated highly parallel architecture in reconfigurable computing," in *10th Annual IEEE Symposium on Field-Programmable Custom Computing Machines*, 2002, pp. 173–181.

[88] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan, "Description of a dedicated hardware architecture for the discrete element method (dem) implemented on a field programmable gate array (fpga)," in *10th Annual conference of the Association for Computational Mechanics in Engineering (ACME)*, 2002, pp. 51–54.

[89] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan, "Evaluation of an fpga implementation of the discrete element method," in *Field-Programmable Logic and Applications*, Berlin, Heidelberg: Springer Berlin Heidelberg, 2001, pp. 306–314.

[90] **B. Carrion Schafer**, S. F. Quigley, and A. H. C. Chan, "Numeric modeling of the mechanical interaction between non-biological particles using reconfigurable computing," in *9th Annual conference of the Association for Computational Mechanics in Engineering (ACME)*, 2001, pp. 53–56.

Books

[B1] **B. Carrion Schaefer**, *High-Level Synthesis Made Easy*, 1st. highX Technologies, 2023.

Book Chapters

[BC1] S. Katkoori and S. A. Islam, *Source code obfuscation of behavioral ips: Challenges and solutions, chapter 3*, 2020.

[BC2] W. Vanderbauwhede and K. Benkrid, *High-level synthesis: From algorithm to digital circuit, chapter 7*, 2013.

[BC3] P. Coussy and A. Morawiec, *High-level synthesis: From algorithm to digital circuit*, 2008.

Patents

[P1] **B. Carrion Schafer**, *Method and apparatus for incremental design space exploration*, U.S. Patent 8,977,996 B2.

[P2] **B. Carrion Schafer**, *Method and apparatus for design space exploration*, JP Patent 2012-522281.

RESEARCH IMPACT AND CITATIONS

h-index (Google Scholar March 2023): 22
i10-index (Google Scholar March 2023): 33
Citations (Google Scholar March 2023): 1548

SOFTWARE ARTIFACTS RELEASED

DSE2Frame: DSE Explorer Framework
DSEFrame is a QT-based open source development framework to create and visualize High-Level Synthesis (HLS) design space exploration results. The development framework is freely available online at *https://github.com/DARCLabHao/DSEframe*.

S2CBench: Synthesizable SystemC Benchmark Suite
S2CBench is collection of over 20 SystemC benchmarks from different domain that comply with the latest Accelera's SystemC synthesizable subset. The benchmark suite is freely available online at *https://sourceforge.net/projects/s2cbench/* from where it has been downloaded over 1,000 times.

S3CBench: Security Synthesizable SystemC Benchmark Suite
S3CBench is the extension of the S2CBench benchmarks instrumented with malicious alterations a.k.a. Hardware Trojan that when triggered lead to deviation of the benchmark from its original intended behavior . The benchmark suite is freely available online at *https://sourceforge.net/projects/s3cbench/* from where it has been downloaded over 300 times.

UNIVERSITY COURSES TAUGHT

At the University of Texas at Dallas

Year	Semester	Code	Type	Title, Credits, Students
2022	Fall	EE/CE4307	Under/core	Embedded Systems, 3, 37
2022	Fall	EEDG6304	Grad/core	Computer Architecture, 3, 55
2022	Summer	EE/CE4304	Under/core	Computer Architecture, 3, 10
2022	Spring	EE/CE4307	Under/core	Embedded Systems, 3, 60
2021	Fall	EEDG/CE6331	Grad/elec	High-Level Synthesis, 3, 8
2021	Fall	EEDG6304	Grad/core	Computer Architecture, 3, 60
2021	Spring	EE/CE4307	Under/core	Embedded Systems, 3, 55
2020	Spring	EEDG7V81	Grad/elec	High-Level Synthesis, 3, 7
2020	Fall	EEDG6304	Grad/core	Computer Architecture, 3, 43
2020	Spring	EE/CE4307	Under/core	Embedded Systems 3, 60
2019	Fall	EEDG7V81	Grad/elec	High-Level Synthesis, 3, 7
2019	Fall	EEDG6304	Grad/core	Computer Architecture, 3, 43
2019	Spring	EE/CE4307	Under/core	Embedded Systems, 3, 49
2018	Fall	EEDG7V81	Grad/elec	High-Level Synthesis, 3, 15
2018	Fall	EEDG6304	Grad/core	Computer Architecture, 3, 13
2018	Spring	EEDG6304	Grad/core	Computer Architecture, 3, 13
2018	Spring	EE/CE4370	Under/core	Embedded Systems, 3, 43
2017	Fall	EEDG6304	Grad/core	Computer Architecture, 3, 16
2017	Spring	EEDG6304	Grad/core	Computer Architecture, 3, 16

At the Hong Kong Polytechnic University

Year	Semester	Code	Type	Title, Credits, Students
2016	Spring	EIE4110	Under/elect	VLSI&CAD, 3, 31
2015	Fall	EIE511	Grad/elect	VLSI System design,3, 15
2014	Spring	EIE4110	Under/elect	VLSI&CAD, 3, 63
2014	Spring	EIE3361	Under/core	Computer Fund, 3, 62
2014	Fall	EIE511	Grad/elect	VLSI System design, 3, 26
2014	Fall	EIE2105	Under/core	Digital Design, 3, 28
2014	Spring	EIE4110	Under/elect	VLSI&CAD, 3, 29
2014	Spring	EIE3361	Under/core	Computer Fund, 3, 74
2013	Fall	EIE2105	Under/elect	Digital Design, 3, 35
2013	Spring	EIE305	Under/elect	Digital Circuits, 3, 18
2013	Spring	EIE361	Under/core	Computer Fund, 3, 56
2013	Spring	EIE410	Under/elect	VLSI&CAD, 3, 22

GRADUATE STUDENTS CURRENTLY SUPERVISED

Ph.D. Candidates

Pandy Kalimuthu: Post-Silicon Debug	2017-present
Qilin Si : Behavioral Application Specific Processors	2018-present
Imtiaz Rashid: Behavioral Synthesis Optimizations	2020-present
Sai Kumar Marri : Behavioral ANNs	2021-present
Chaitali Sathe: Hardware Security	2021-present

M.S. Candidates

Amir H. Torabi	2022-present

GRADUATE STUDENTS PREVIOUSLY SUPERVISED

Ph.D. Students

Prattay Chowdhury, Ph.D. (UTD)	Qualcomm, USA	2019-2022
Zi Wang, Ph.D. (UTD)	Cadence, USA	2017-2021
Bo Hu, Ph.D. (UTD) (w. C. Sechen)	Apple, USA	2016-2021
Jianqi Chen, Ph.D. (UTD)	Cirrus Logic, USA	2016-2020
Anjana Balachandran Ph.D.(PolyU)	Huawei, HKSAR	2014-2020
Zhiqi Zhu, Ph.D.(UTD)	Nubis Communications, USA	2014-2020
Farah Naz Taher, Ph.D.(UTD)	Raytheon, USA	2016-2019
Siyuan Xu, Ph.D.(UTD)	Mathworks, USA	2017-2019
Shuangnan Liu, Ph.D. (PolyU)	Cadence, China	2014-2019
Ansuhree Mahapatra, Ph.D.(PolyU)	ASTRI, HKSAR	2013-2018
Nandeesh Veeranna, Ph.D.(PolyU)	NTU, Singapore	2014-2017

M.S. Students

Valliyappan Senthilkumar	Marvell Tech., USA	2022-2023
Santosh Shetty, M.S. (UTD)	AMD, India	2019-2020
Akshay Raju Krisnani, M.S. (UTD)	Intel, USA	2019-2020
Yiheng Gao, M.S. (UTD)	Nokia, USA	2019-2020
Rohit Sreekumar, M.S. (UTD)	Amazon, USA	2019-2020
Himanshu Patra, M.S. (UTD)	Intel, USA	2017-2019
Maheswaran R. Babu, M.S. (UTD)	Intel, USA	2017-2019
Mihir Shah, M.S. (UTD)	Varex Imaging Corp, USA	2016-2018
Monica J. Gowda, M.S. (UTD)	MicroChip Corp, USA	2016-2018
Vinay Nagard Dasandi, M.S, (UTD)	Delphi, USA	2016-2018
Songseok Choi, M.S. (UTD)	SK Hynix, South Korea	2015-2018
Susmitha Gogineni, M.S. (UTD)	Texas Instruments, USA	2014-2017
Siyuan Xu, MS.c. (PolyU)	PhD candidate UTD, USA	2014-2015
Zhendong Gao, MS.c. (PolyU)	PCCW, HKSAR	2014-2015
Jieshi Chen, MS.c. (PolyU)	DJI, China	2014-2015
Yu Li, MS.c. (PolyU)	ZTE, China	2013-2014
Xiaotong Li, MS.c. (PolyU)	TCL, China	2013-2014

VISITING GRADUATE STUDENTS SUPERVISED

Takafumi Miyazaki (Visiting from Ritsumeikan University, Japan)	09/2018-10/2018
Shuangnan Liu (Visiting from Hong Kong Polytechnic University, HKSAR)	09/2017-12/2018
Nandeesh Veeranna (Visiting from Hong Kong Polytechnic University, HKSAR)	04/2017-07/2017
Monica Villaverde (Visiting from Universidad Politecnica de Madrid, Spain)	01/2017-04/2017

UNDERGRADUATE AND HIGH SCHOOL STUDENTS SUPERVISED

Undergraduate Students

Axel Gamez **(Qualcomm Research Award Recipient)**	Fall 2022
Preston T. Glenn	Summer and Fall 2021
Kimberly Klein **(Qualcomm Research Award Recipient)**	Spring 2021
Michael Nelson	Fall and Spring 2017/2018
Rodolfo Martinez	Summer 2018
Ryota Watanabe	Summer 2018
Kristen Nguyen	Summer 2018
Sean Kennedy	Summer 2018

High School Students

Ishaan Javali	Summer 2019
Alondra Ramos	Summer 2018
Natasha Trayers	Summer 2018

STUDENT SUPERVISION SUMMARY

Ph.D. students currently supervised:	5
M.S. students currently supervised:	2
Ph.D. students graduated:	11
M.S. students graduated:	16
Undergraduate researchers supervised:	8
High School Students supervised:	3

KEYNOTES, INVITED TALKS AND SHORT COURSES TAUGHT

B. Carrion Schafer, "Techniques for Finding Security Vulnerabilities in SoCs,", ACM/IEEE Design Automation Conference (DAC), San Francisco, USA, June, 2018.

B. Carrion Schafer, "Behavioral IPs Micro-architectural Diversity and its Applications", ESLSyn, San Francisco, Co-located with DAC, June 2015,

B. Carrion Schafer and J.H. Anderson, "FPGA high-level synthesis: from software to programmable hardware," tutorial delivered at the ACM/IEEE Asia-South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2015.

A. Mahapatra and **B. Carrion Schafer**, "S2CBench:Synthesizable SystemC Benchmark Suite for HighLevel Synthesis", 20th meeting of the North American SystemC Users Group,San Francisco, June, 2014.

B. Carrion Schafer,"The ESL Hotspot - Where Software and Hardware Meet", Design Automation Conference (DAC), 10th annual ESL Symposium, San Francisco, (invited panelist), 2012.

B. Carrion Schafer,"High-Level Synthesis Production Deployment: Are We Ready?", Design Automation Conference (DAC), San Francisco, (invited speaker), 2012.

B. Carrion Schafer,"Challenges and Opportunities of Behavioral Level SoC Design", ESLSyn, Co-located with DAC, San Francisco, (Keynote speaker), 2012.

GRANTS, CONTRACTS AND DONATIONS

NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen). Continuation grant 2022-2023
Total amount : $125,000.
Annual amount/PI : $41,500

NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen). Continuation grant 2021-2022
Total amount : $125,000.
Annual amount/PI : $41,500

AFWERX, Microelectronics Challenge Phase III (lead-PI w. Makris and Sechen) 2020
Total amount : $200,000.
Annual amount/PI : $66,600

NSF CHEST I/UCRC,CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming(co-PI w. PI-Makris and Sechen) 2020-2021
Total amount : $100,000.
Annual amount/PI : $33,000

Boeing/AFRL (co-PI w. PI-Makris and Sechen) 2020
Total amount : $150,000.
Annual amount/PI : $50,000

AFWERX, Microelectronics Challenge Phase II (lead-PI w. Makris and Sechen) 2019
Total amount : $88,410.
Annual amount/PI : $30,000

NATO, Nerve Agent Detection, (co-PI w. PI-Llamas and Mung) 2019-2022
Total amount : $236,000.
Total amount/PI : $22,000

Huawei USA, Based Band SoC Approximate Computing (Sole PI) 2018
Total amount : $60,000.

Texas Instruments (Sole PI) 2018
Total amount : $14,000.

NEC Corporation, Software Grant (CyberWorkBench Software license donation) 2017
Value: $10,000

Altera Equipment Grant (Arria SoC and DE1 FPGA Boards) 2017
Value: $7,000

Xilinx Equipment Grant (Virtex-5 and Zynq FPGA Boards) 2017
Total amount : $8,000.

University of Texas at Dallas (Sole PI) 2016
Total amount : $285,000.

Early Career Scheme, University Grant Council, Hong Kong (Sole PI) 2014
Total amount : HKD $677,000 ($87,000).
Annual amount/PI : $29,000

National Natural Science Foundation of China (co-PI w. PI-Lau and Ho) 2014
Total amount : RMB $750,000 ($120,000).
Annual amount/PI : $13,000

PROFESSIONAL MEMBERSHIPS AND LICENSES

IEEE Senior Member since 2010