

## Fundamentals of Microelectronics

- CH1 Why Microelectronics?
- CH2 Basic Physics of Semiconductors
- CH3 Diode Circuits
- CH4 Physics of Bipolar Transistors
- CH5 Bipolar Amplifiers
- CH6 Physics of MOS Transistors
- CH7 CMOS Amplifiers
- CH8 Operational Amplifier As A Black Box

1

## Chapter 7 CMOS Amplifiers

- 7.1 General Considerations
- 7.2 Common-Source Stage
- 7.3 Common-Gate Stage
- 7.4 Source Follower
- 7.5 Summary and Additional Examples

2

## Chapter Outline

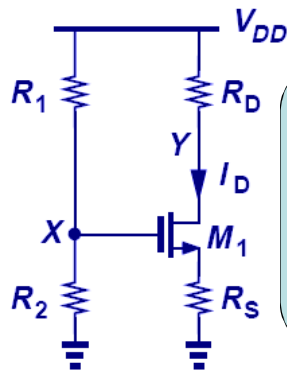
### General Concepts

- Biasing of MOS Stages
- Realization of Current Sources

### MOS Amplifiers

- Common-Source Stage
- Common-Gate Stage
- Source Follower

## MOS Biasing

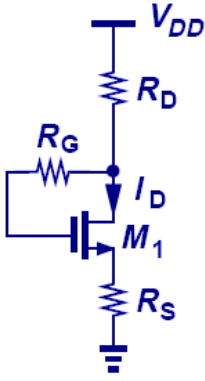


$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left( \frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH} \right)}$$

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}$$

- Voltage at X is determined by  $V_{DD}$ ,  $R_1$ , and  $R_2$ .
- $V_{GS}$  can be found using the equation above, and  $I_D$  can be found by using the NMOS current equation.

### Self-Biased MOS Stage

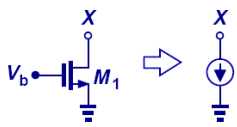


$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$

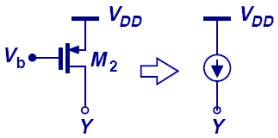
➤ The circuit above is analyzed by noting M1 is in saturation and no potential drop appears across  $R_G$ .

CH7 CMOS Amplifiers
5

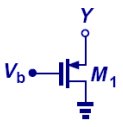
### Current Sources



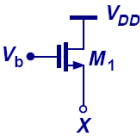
(a)



(b)



(c)



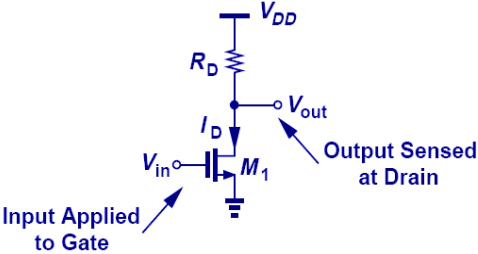
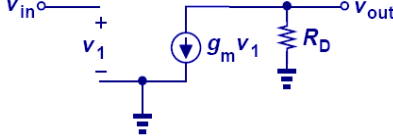
(d)

➤ When in saturation region, a MOSFET behaves as a current source.

➤ NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from  $V_{DD}$  to a point (sources current).

CH7 CMOS Amplifiers
6

### Common-Source Stage

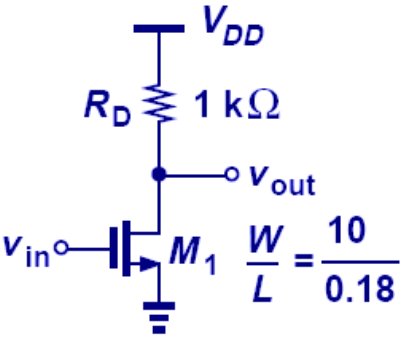
$\lambda = 0$

$A_v = -g_m R_D$

$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} R_D$

CH7 CMOS Amplifiers 7

### Operation in Saturation

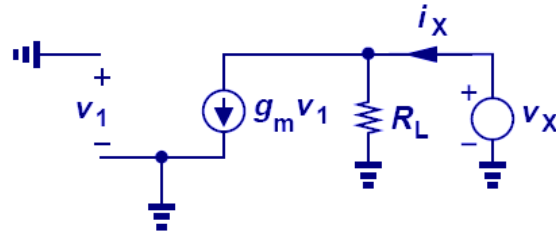


$$R_D I_D < V_{DD} - (V_{GS} - V_{TH})$$

- In order to maintain operation in saturation,  $V_{out}$  cannot fall below  $V_{in}$  by more than one threshold voltage.
- The condition above ensures operation in saturation.

CH7 CMOS Amplifiers 8

### CS Stage with $\lambda=0$



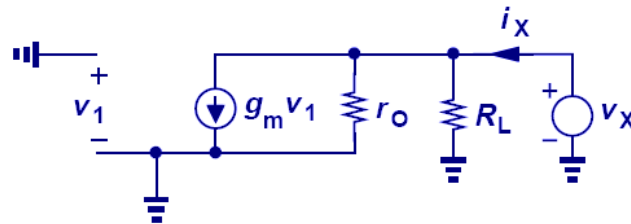
$$A_v = -g_m R_L$$

$$R_{in} = \infty$$

$$R_{out} = R_L$$

9

### CS Stage with $\lambda \neq 0$



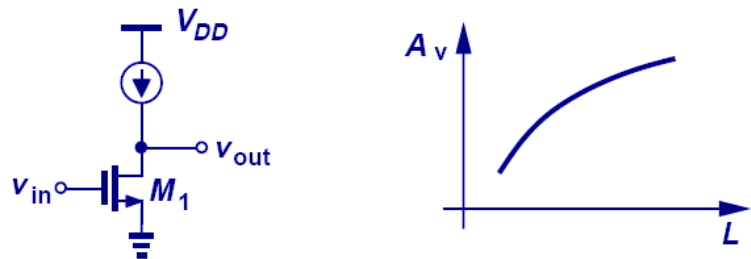
$$A_v = -g_m (R_L \parallel r_o)$$

$$R_{in} = \infty$$

$$R_{out} = R_L \parallel r_o$$

➤ However, Early effect and channel length modulation affect CE and CS stages in a similar manner.

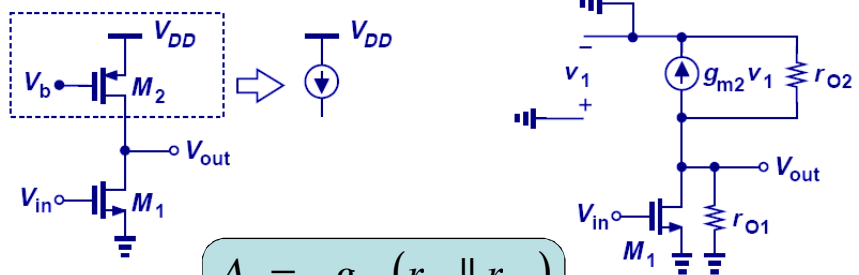
### CS Gain Variation with Channel Length



$$|A_v| = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L}}}{\lambda \sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

➤ Since  $\lambda$  is inversely proportional to  $L$ , the voltage gain actually becomes proportional to the square root of  $L$ .

### CS Stage with Current-Source Load

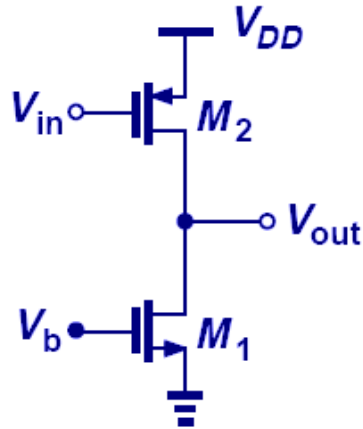


$$A_v = -g_{m1} (r_{O1} \parallel r_{O2})$$

$$R_{out} = r_{O1} \parallel r_{O2}$$

➤ To alleviate the headroom problem, an active current-source load is used.  
 ➤ This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.

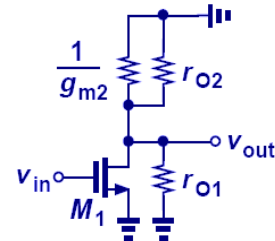
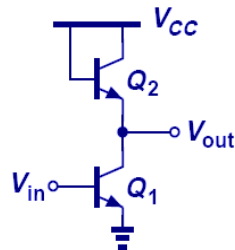
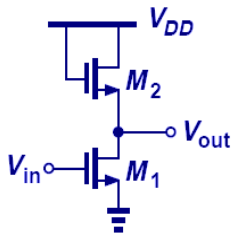
**PMOS CS Stage with NMOS as Load**



$$A_v = -g_{m2}(r_{o1} \parallel r_{o2})$$

➤ Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.

**CS Stage with Diode-Connected Load**

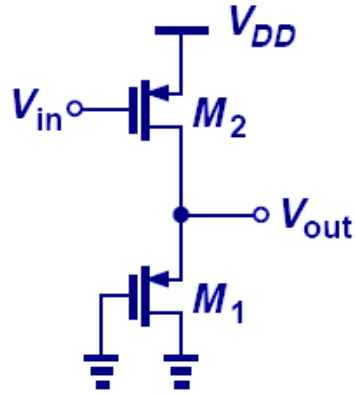


$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

$$A_v = -g_{m1} \left( \frac{1}{g_{m2}} \parallel r_{o2} \parallel r_{o1} \right)$$

➤ Lower gain, but less dependent on process parameters.

### CS Stage with Diode-Connected PMOS Device

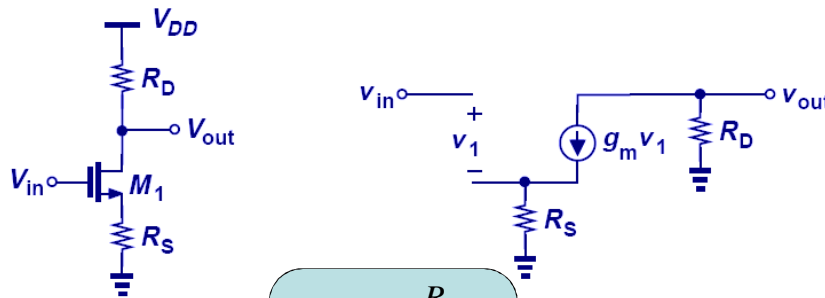


$$A_v = -g_{m2} \left( \frac{1}{g_{m1}} \parallel r_{o1} \parallel r_{o2} \right)$$

➤ Note that PMOS circuit symbol is usually drawn with the source on top of the drain.

15

### CS Stage with Degeneration



$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

$$\lambda = 0$$

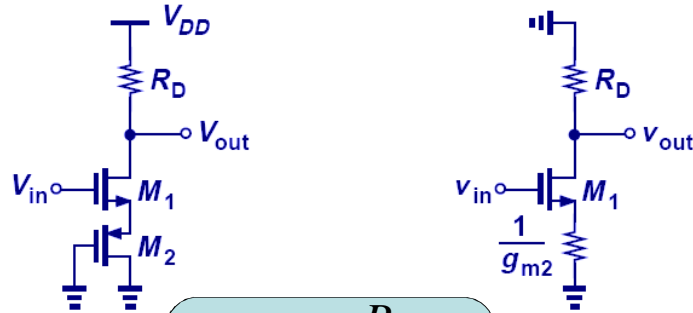
➤ Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.

CH7 CMOS Amplifiers

16



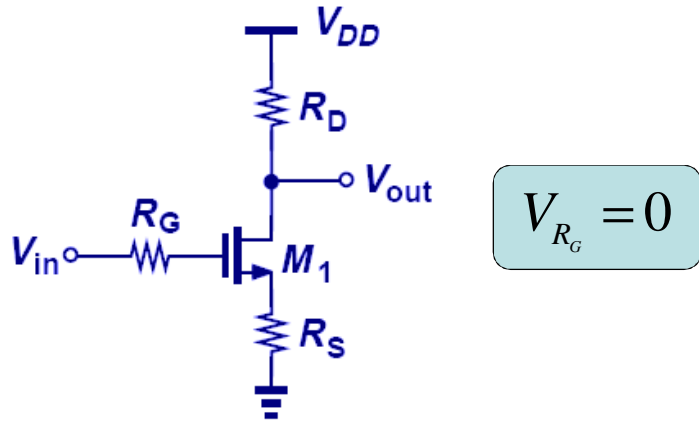
**Example of CS Stage with Degeneration**



$$A_v = - \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

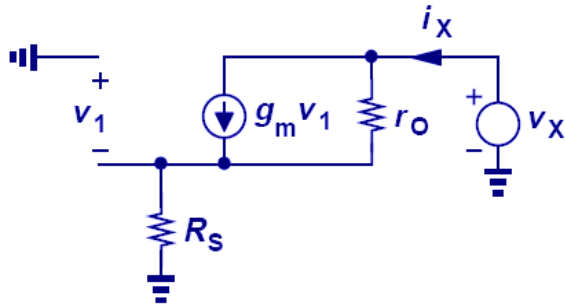
➤ **A diode-connected device degenerates a CS stage.**

**CS Stage with Gate Resistance**



➤ **Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.**

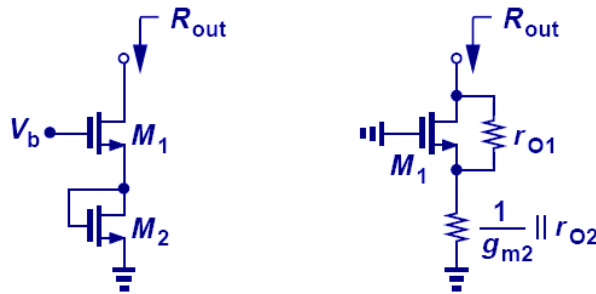
### Output Impedance of CS Stage with Degeneration



$$r_{out} \approx g_m r_O R_S + r_O$$

➤ Similar to the bipolar counterpart, degeneration boosts output impedance.

### Output Impedance Example (I)



$$R_{out} = r_{O1} \left( 1 + g_{m1} \frac{1}{g_{m2}} \right) + \frac{1}{g_{m2}}$$

➤ When  $1/g_m$  is parallel with  $r_{O2}$ , we often just consider  $1/g_m$ .

### Output Impedance Example (II)

$$R_{out} \approx g_{m1} r_{O1} r_{O2} + r_{O1}$$

➤ In this example, the impedance that degenerates the CS stage is  $r_O$ , instead of  $1/g_m$  in the previous example.

CH7 CMOS Amplifiers
21

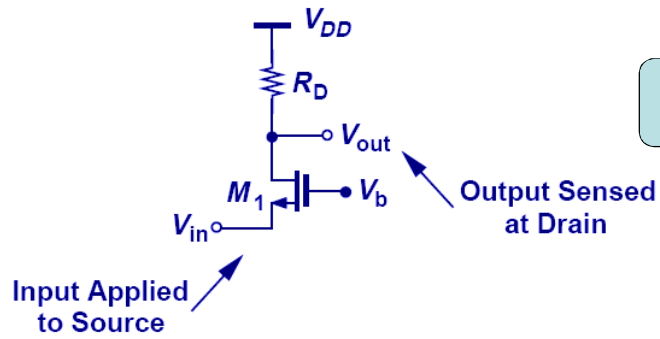
### CS Core with Biasing

$$A_v = \frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}, A_v = -\frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} g_m R_D$$

➤ Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.

CH7 CMOS Amplifiers
22

## Common-Gate Stage



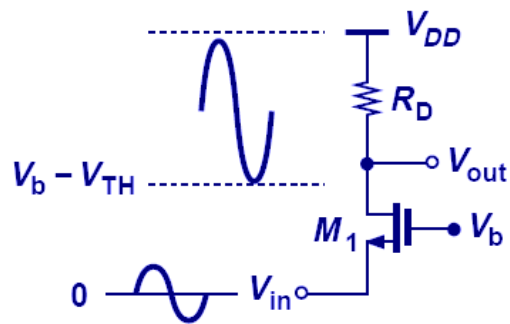
$$A_v = g_m R_D$$

- Common-gate stage is similar to common-base stage: a rise in input causes a rise in output. So the gain is positive.

CH7 CMOS Amplifiers

23

## Signal Levels in CG Stage

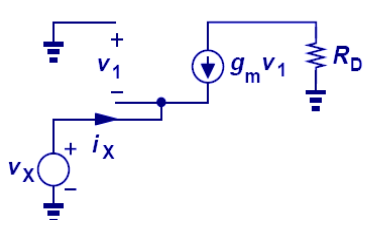
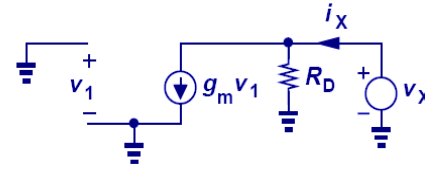


- In order to maintain  $M_1$  in saturation, the signal swing at  $V_{out}$  cannot fall below  $V_b - V_{TH}$ .

CH7 CMOS Amplifiers

24

### I/O Impedances of CG Stage

$$R_{in} = \frac{1}{g_m}$$

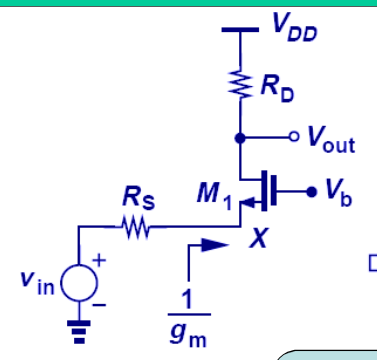
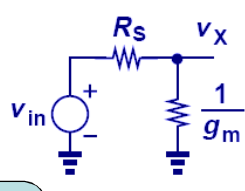
$$\lambda = 0$$

$$R_{out} = R_D$$

➤ The input and output impedances of CG stage are similar to those of CB stage.

CH7 CMOS Amplifiers
25

### CG Stage with Source Resistance

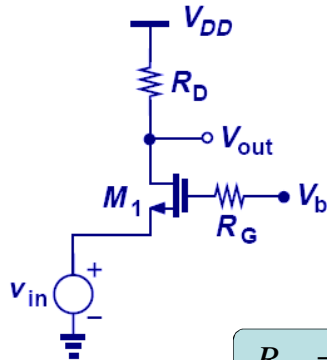
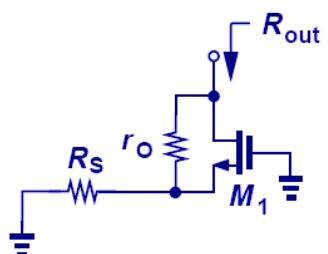

➔


$$A_v = \frac{R_D}{\frac{1}{g_m} + R_s}$$

➤ When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.

CH7 CMOS Amplifiers
26

### Generalized CG Behavior

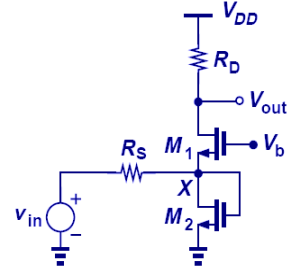
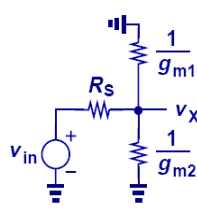
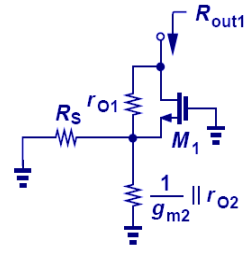



$$R_{out} = (1 + g_m r_O) R_S + r_O$$

- When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it ( at low frequencies).
- The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.

CH7 CMOS Amplifiers
27

### Example of CG Stage

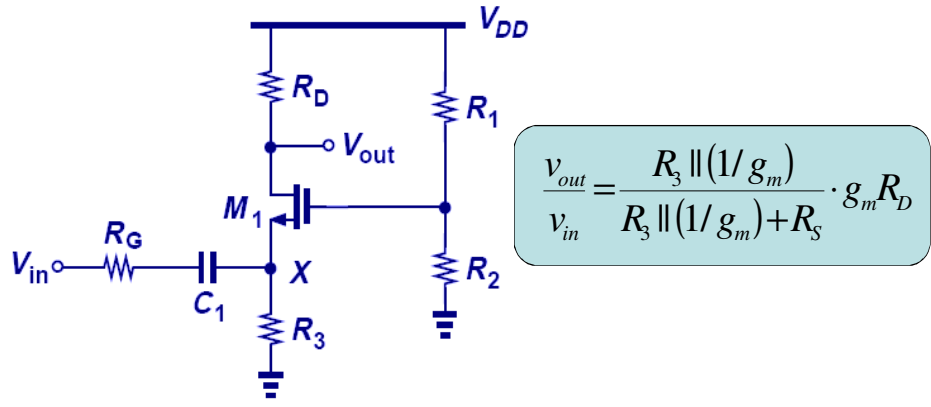




$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} R_D}{1 + (g_{m1} + g_{m2}) R_S} \quad R_{out} \approx \left[ g_{m1} r_{O1} \left( \frac{1}{g_{m2}} \parallel R_S \right) + r_{O1} \right] \parallel R_D$$

- Diode-connected M<sub>2</sub> acts as a resistor to provide the bias current.

CH7 CMOS Amplifiers
28

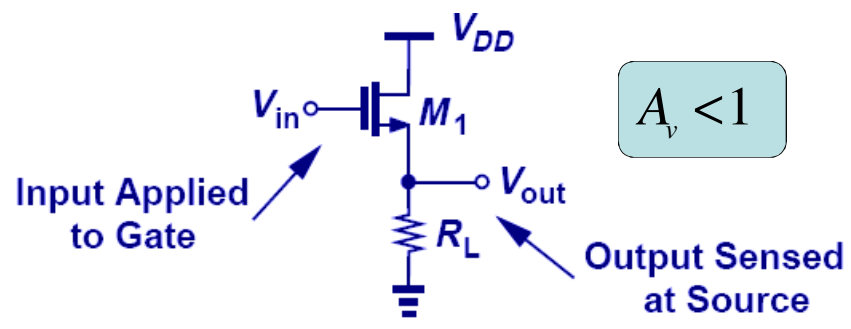
**CG Stage with Biasing**



$$\frac{v_{out}}{v_{in}} = \frac{R_3 \parallel (1/g_m)}{R_3 \parallel (1/g_m) + R_S} \cdot g_m R_D$$

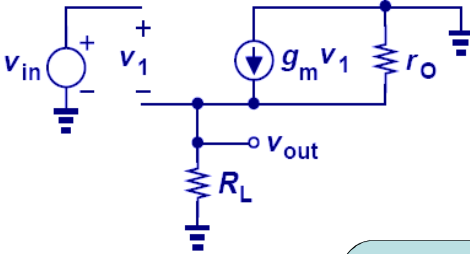
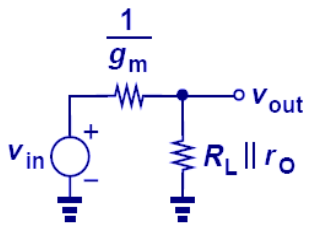
➤ R<sub>1</sub> and R<sub>2</sub> provide gate bias voltage, and R<sub>3</sub> provides a path for DC bias current of M<sub>1</sub> to flow to ground.

**Source Follower Stage**



$$A_v < 1$$

### Source Follower Core

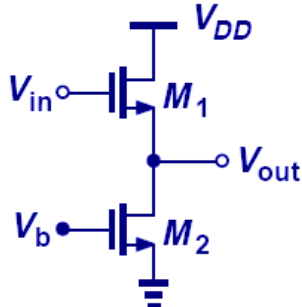
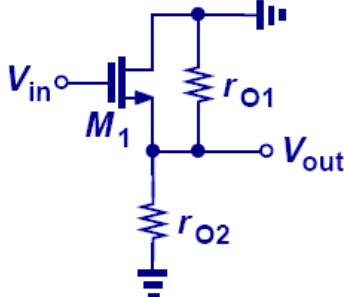
$$\frac{v_{out}}{v_{in}} = \frac{r_o \parallel R_L}{\frac{1}{g_m} + r_o \parallel R_L}$$

➤ Similar to the emitter follower, the source follower can be analyzed as a resistor divider.

CH7 CMOS Amplifiers

31

### Source Follower Example

$$A_v = \frac{r_{o1} \parallel r_{o2}}{\frac{1}{g_{m1}} + r_{o1} \parallel r_{o2}}$$

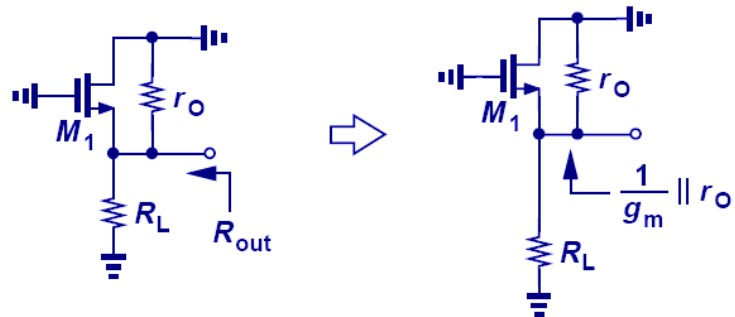
➤ In this example, M<sub>2</sub> acts as a current source.

CH7 CMOS Amplifiers

32



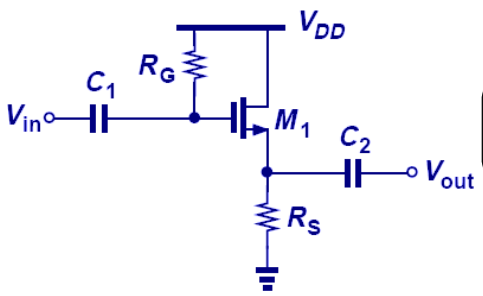
**Output Resistance of Source Follower**



$$R_{out} = \frac{1}{g_m} \parallel r_o \parallel R_L \approx \frac{1}{g_m} \parallel R_L$$

➤ The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.

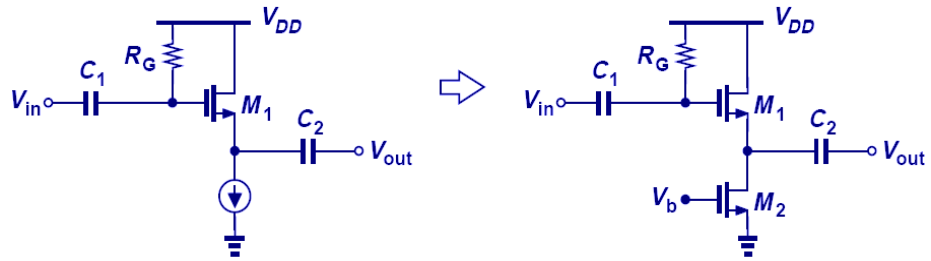
**Source Follower with Biasing**



$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - I_D R_S - V_{TH})^2$$

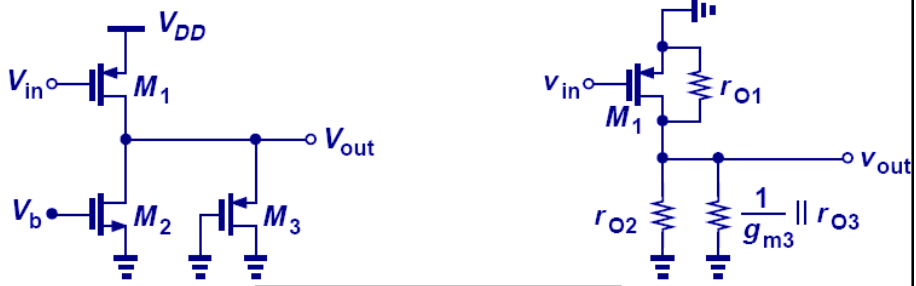
➤  $R_G$  sets the gate voltage to  $V_{DD}$ , whereas  $R_S$  sets the drain current.  
 ➤ The quadratic equation above can be solved for  $I_D$ .

### Supply-Independent Biasing



➤ If  $R_s$  is replaced by a current source, drain current  $I_D$  becomes independent of supply voltage.

### Example of a CS Stage (I)

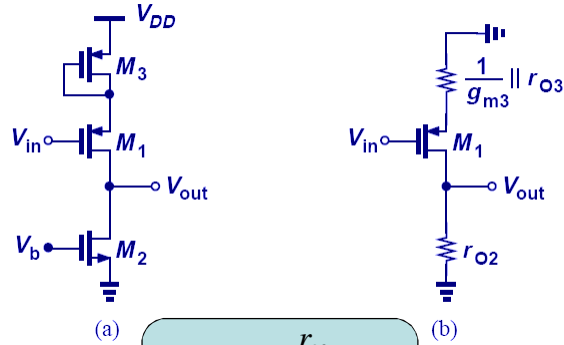


$$A_v = -g_{m1} \left( \frac{1}{g_{m3}} \parallel r_{o1} \parallel r_{o2} \parallel r_{o3} \right)$$

$$R_{out} = \frac{1}{g_{m3}} \parallel r_{o1} \parallel r_{o2} \parallel r_{o3}$$

➤  $M_1$  acts as the input device and  $M_2, M_3$  as the load.

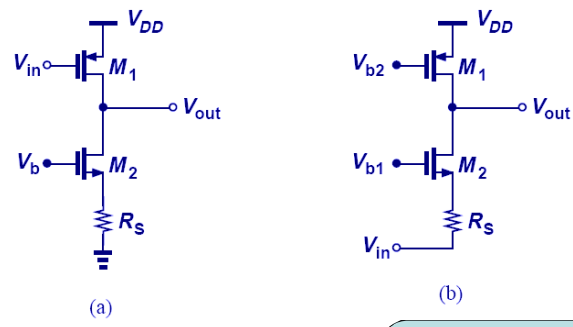
**Example of a CS Stage (II)**



$$A_v = -\frac{r_{O2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}} \parallel r_{O3}}$$

➤ **M<sub>1</sub> acts as the input device, M<sub>3</sub> as the source resistance, and M<sub>2</sub> as the load.**

**Examples of CS and CG Stages**

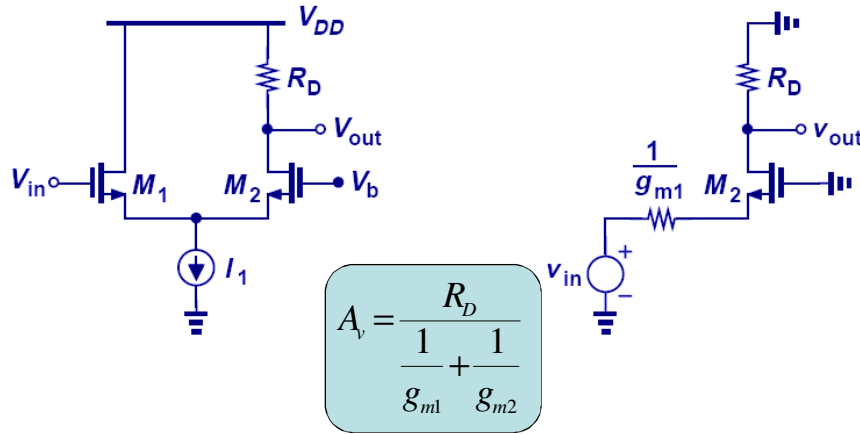


$$A_{v\_CS} = -g_{m2} [(1 + g_{m1} r_{O1}) R_S + r_{O1}] \parallel r_{O1}$$

$$A_{v\_CG} = \frac{r_{O2}}{\frac{1}{g_m} + R_S}$$

➤ **With the input connected to different locations, the two circuits, although identical in other aspects, behave differently.**

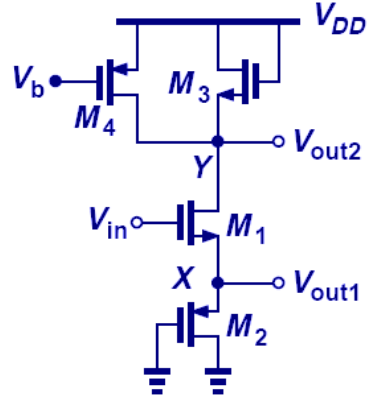
**Example of a Composite Stage (I)**



$$A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

➤ By replacing the left side with a Thevenin equivalent, and recognizing the right side is actually a CG stage, the voltage gain can be easily obtained.

**Example of a Composite Stage (II)**



$$\frac{v_{out2}}{v_{in}} = - \frac{\frac{1}{g_{m3}} \parallel r_{O3} \parallel r_{O4}}{\frac{1}{g_{m2}} \parallel r_{O2} + \frac{1}{g_{m1}}}$$

➤ This example shows that by probing different places in a circuit, different types of output can be obtained.  
 ➤  $V_{out1}$  is a result of  $M_1$  acting as a source follower whereas  $V_{out2}$  is a result of  $M_1$  acting as a CS stage with degeneration.