IC Laser Trimming Speed-Up through Wafer-Level Spatial Correlation Modeling

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***Abstract*—Laser trimming is used extensively to ensure accurate values of on-chip precision resistors in the presence of process variations. Such laser resistor trimming is slow and expensive, typically performed in a closed-loop, where the laser is iteratively fired and some circuit parameter (i.e. current) is monitored until a target condition is satisfied. Toward reducing this cost, we introduce a novel methodology for predicting the laser trim length, thereby eliminating the closed-loop control and speeding up the process. Predictions are obtained from wafer-level spatial correlation models, learned from a sparse sample of die on which traditional trimming is performed. Effectiveness is demonstrated on an actual wafer of laser-trimmed ICs.**

I. Introduction

Ensuring performances of high-end integrated circuit (ICs) often relies on precision resistance values or resistance ratios. To this end, IC laser trimming has been extensively used for several decades as a means to controlling the impact of process variation on these sensitive resistors, which, in turn, assist in calibrating shifted electrical parameters of the IC. As reported in [1], over 70% of the world's analog semiconductor companies use laser-based trimming and/or link-blowing in thin-film semiconductor and silicon manufacturing. Several on-chip resistors are placed in ICs to trim the parameters in question and trimming is performed by burning away small portions of these resistors using a laser trimming machine, in order to raise their resistance values until a target is reached. This laser trimming operation is usually conducted while the circuit is being tested by automatic test equipment (ATE), leading to appropriate final values for the resistors in the trimmed circuit. Figure 1 illustrates the objective of this trimming procedure, which essentially seeks to center the distribution of IC performances in order to enhance the manufacturing yield of a given design.

While this laser trimming procedure permits test engineers to efficiently center the distribution of IC performances and enhance manufacturing yield, it remains an expensive processing step which significantly increases the IC production costs [2]. Indeed, trimming is a lengthy procedure which is typically performed in a closed-loop, where the laser is iteratively fired and the IC parameter in question is monitored until a target condition is satisfied.

In this work, we introduce a methodology for reducing the trimming cost by predicting the laser trim length, thereby eliminating the closed-loop control and speeding up the trimming process. In particular, we employ a spatial correlation modeling methodology based on Gaussian Process (GP), which has been successfully implemented in the context of analog/RF test cost reduction [3]–[6]. In this approach, instead of performing the closed-loop trimming procedure for every die on a wafer, we only trim a small sample of devices. The effective trim lengths of the sampled devices are then used to train spatial regression models, which are subsequently used to predict the required trim length for the remaining die on the wafer. The underlying conjecture is that the required trim length is spatially correlated across a wafer, therefore a sample is sufficient for us to accurately predict trim lengths at other die locations. The effectiveness of the proposed approach is demonstrated on an actual wafer of laser-trimmed ICs. Herein, we show that the proposed approach significantly reduces the time and, thereby, the cost of the trimming procedure.

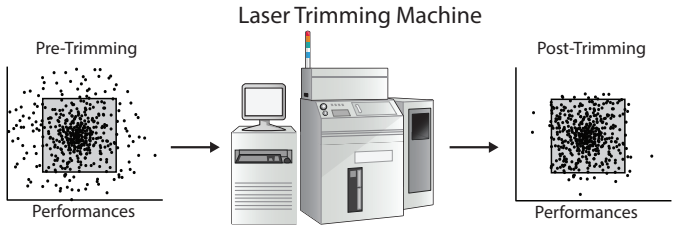

Fig. 1. Trimming procedure to center IC performances that shift due to process variations.

The remainder of this paper is organized as follows. In Section II, we give a brief introduction of a typical IC laser trimming procedure. In Section III, we describe the proposed methodology for predicting the required trim length and reducing the time and cost of laser trimming based on wafer-level spatial correlation modeling. An introduction to the latter, with emphasis on the Gaussian process model, which is used in our work, is given in Section IV. In Section V, we provide experimental results in support of the proposed method, and conclusions are drawn in Section VI.

II. IC laser trimming

As the semiconductor industry continues scaling devices toward smaller process nodes, maintaining acceptable yield despite process variations has become increasingly challenging.

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Uncertainty is introduced by various sources during manufacturing and each step, such as lithography, ion implantation, thermal treatments, etc., can be considered as a source of variation. To handle these challenges, designers have traditionally resorted to conservative circuit design approaches, trading off some performance for higher yield and better variation tolerance.

Alternatively, post-silicon calibration methods, such as laser trimming, can be used to adjust various parameters of interest in an IC and to compensate parametric shifts caused by process variation. A number of laser trimmable resistors are often implemented on-die for this purpose and, depending on the application and the required tolerance, various cutting patterns and resistor geometries have been introduced. Accordingly, the IC laser resistor trimming procedure is comprised of three main components [7]: the device under test (DUT), the guided laser trimmer and a measurement tracking system.

During the laser trimming process, the guided laser beam fires pulses on the resistor causing the material on its surface to heat rapidly and vaporize. Consequently, the resistance value is increased after each laser pulse. The amount by which the resistance increases after a single pulse determines the accuracy and speed of the trimming process. Tracking of the desired parameter is achieved by a measurement system, as shown in Figure 2. The connection between the DUT and the measurement system is usually done by probes which are connected to the ends of the laser trimmable resistors. As shown in Figure 2, the trimmed resistance value is converted to a current value by a current sensor. The converted current value is monitored after each laser pulse and is compared with a user specified target value, as shown on the upper left side of Figure 2. The target current value is typically set according to the specification limits of one or more particular performances of the DUT and is being fed to the comparator by a computer driven control system. When the target is reached, a stop signal is sent to the laser to halt the cutting, as shown on the upper right side of Figure 2. The total trimmed length l_{tot} on the resistor during the trimming procedure can then be expressed as:

$$l_{tot} = l_1 + l_2 + \cdots + l_k \tag{1}$$

where l_i denotes the trimmed length cut by the i-th laser pulse and k denotes the total number of laser pulses required to reach the target current value. Consequently, the time required for the laser control system to achieve the target current value is expressed as:

$$t_{tot} = \sum_{i=1}^{k} (t_{\text{cut i}} + t_{\text{set i}}) \tag{2}$$

where $t_{\text{cut i}}$ denotes the trimming time on the i-th laser pulse and $t_{\text{set i}}$ denotes the settling time that is needed in order for the current measurement that is fed to the comparator to stop rippling. As we can observe in equation (2), the total time of the laser trimming process depends on the time required to perform each laser pulse, the total number of laser pulses and the settling time needed to obtain an accurate measurement. In high-accuracy applications, this constraint hinders the laser trimming process as a large number of laser pulses is required to achieve the target, thus increasing the total penalty induced by settling time.

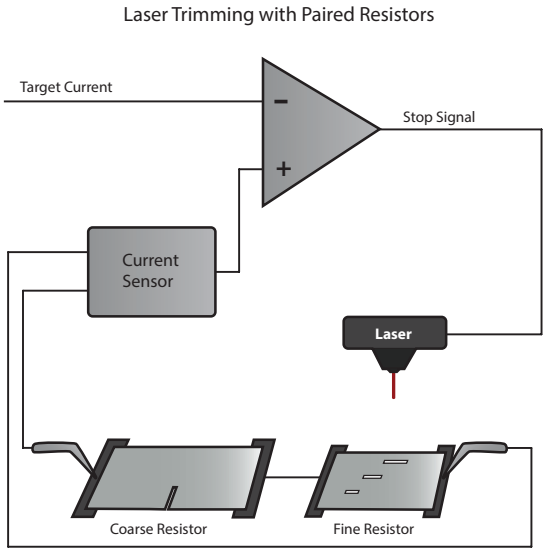

Fig. 2. Measurement tracking system for Laser control.

In order to speed up the trimming process, a two-resistor approach is commonly employed by designing trimmable resistors into pairs, as shown in Figure 2. The first resistor is trimmed to an initial target value with longer pulses and fewer intermediate measurements. This procedure is known as coarse-trim and although it is not as precise as the next step, it is significantly faster. However, a conservative target is typically set in order to avoid over-trimming beyond the final target, which would result in yield loss. Following the coarse-trim, small cuts are performed on the second resistor until the final target value is reached. This is referred to as fine-trim and is much slower than its coarse counterpart. Figure 3 depicts the expected speedup between the single resistor and the paired-resistor laser trimming techniques, with Δt denoting the time saved by the paired-resistor approach.

III. Proposed approach

As noted in the previous section, tracking of the current value during trimming is an iterative and time-consuming process. The current value corresponding to the trimmed resistance is measured and compared to the target value after each laser pulse. The number of intermediate measurements delineates the time overhead, as portrayed in Figure 3. In this work, we propose a new approach to speed up the trimming procedure by employing a spatial correlation modeling methodology. In the proposed approach, instead of using the time-consuming tracking system to monitor the trimming process for every die location on the wafer, we use it only for a sparse subset of die samples. We, then, use the recorded data

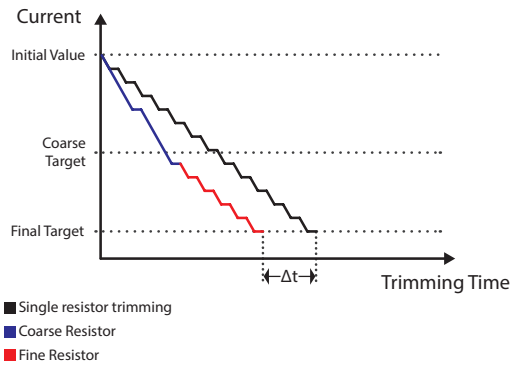

Fig. 3. Single vs Paired resistor processes.

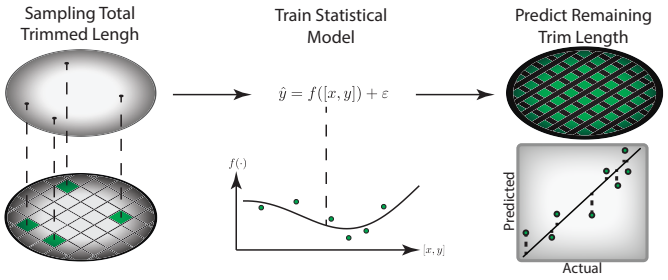

Fig. 4. Proposed approach for trimming speed-up.

to build a model of the trim length as a function of the die coordinates on the wafer, using which we predict the required trim length for the remaining die. Finally, we instruct the laser to cut the resistors based on the predicted length, without taking any intermediate current measurements, i.e. without engaging the closed-loop control. Below, we introduce three methods for predicting the required trim length.

A. Length-based, original target prediction.

The first method uses directly the trim lengths of the sparse sample of die that are trimmed using the closed-loop approach. The conjecture here is that this physical parameter (i.e. the trim length) is spatially correlated across the wafer. Therefore, a model that predicts the required trim length as a function of the die coordinates can be trained. The underlying idea is shown in Figure 4, where the sampled lengths are used to train the statistical model which, in turn, is used to generate the predicted lengths. For this purpose, we use the Gaussian process spatial correlation model, which we explain in detail in Section IV. These lengths will be fed directly to the laser and will be trimmed in a single laser pulse. We refer to the process of using pre-determined trim lengths as open-loop, as opposed to the closed-loop approach which iteratively trims and measures the current in multiple small increments. In Figure 5, we depict the expected time savings of our approach. The black line represents the classic closed-loop trimming method as the baseline. The blue line represents the length-based open-loop method. As may be observed, the open-loop completes the coarse-trim faster and, as a result, the complete trimming (i.e. coarse plus fine) is expedited over the closed-loop approach. The saved time is denoted by Δt_1.

B. Rate-based, original target prediction.

Alternatively, for reasons that will become apparent in the next subsection, we can predict the required trim length indirectly by first building a GP spatial correlation model that predicts the trim rate of each die as a function of die coordinates. We define the trim rate as the ratio of the difference between the pre-trim and the post-coarse trim current measurements over the trimmed length. Let r_t denote the trim rate for a particular die location, then r_t can be expressed as:

$$r_t = \frac{m_{Pre} - m_{Post}}{L} \tag{3}$$

where m_{Pre} denotes the pre-trim current measurement, m_{Post} denotes the post-coarse trim current measurement and L denotes the corresponding trimmed length. In this case, the sampling process depicted in Figure 4 would generate the predicted trim rate values $\hat{r_t}$ and pre-trim current measurements $\hat{m_{Pre}}$ for every non-sampled device, which in turn would be used to compute the coarse-trim length $\hat{L}$:

$$\hat{L} = \frac{\hat{m_{Pre}} - m_{target}}{\hat{r_t}} \tag{4}$$

where m_{target} denotes the target current which controls the closed-loop and terminates the coarse-trim stage in Figure 2.

Since in this method we are predicting the length needed to reach the coarse target, just as we did in Section III-A, the time savings are the same as before. In other words, the blue line in Figure 5 also depicts the expected savings of the rate-based prediction.

C. Rate-based, optimized target prediction.

Predicting the required trim length based on the trim rate offers an additional advantage. Specifically, we can now set the target current to any value and predict the corresponding trim length, rather than being constrained by the original target of the closed-loop method. In fact, the long laser beam of the coarse-trim stage forces the test engineer to set a rather pessimistic target value in order to avoid over-trimming. As a result a longer cut, at the much slower fine-stage is required for the final target to be reached. In an open-loop configuration, however, we can be more aggressive at the coarse-trim stage and seek to get closer to the final target value, thereby further improving the overall savings.

Using the value of maximum expected error and the difference between the post-coarse trim target current and the final post-fine trim target current, we can then determine a new safe post-coarse trim target value which is closer to the final post-fine trim target current. Then, we can replace the new post-coarse trim current target in equation 4 and get the corresponding coarse-trim length required, as shown below:

$$\hat{L} = \frac{\hat{m_{Pre}} - m_{\text{Optimized target}}}{\hat{r_t}} \tag{5}$$

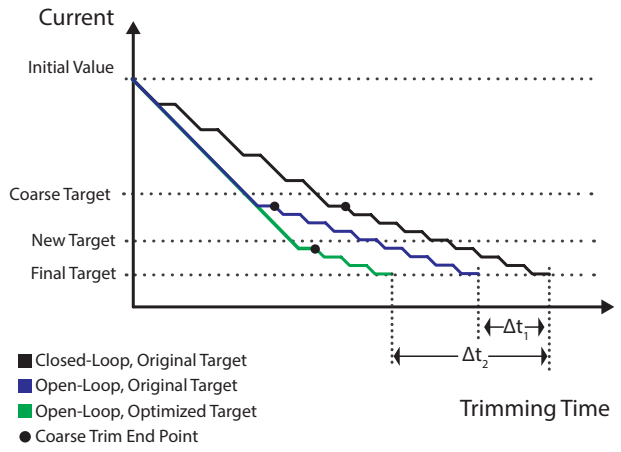

Fig. 5. Current value vs. trim time in paired resistor trimming approach.

where $m_{\text{Optimized target}}$ is the new target post-coarse trim current value and $\hat{L}$ is the predicted trim length required to reach this new target. Revisiting Figure 5, the green line depicts the process when the optimized target has been set closer to the final one. In this case, the open-loop coarse-trim is again faster than the closed-loop version, even though it cuts a longer length, because it requires a single laser pulse. Moreover, additional savings are obtained by the fact that the slow fine-trim stage has a much shorter distance to cover. The overall amount of time that is being saved is reflected by Δt_2.

D. Limitations for laser trimming deployment.

Since the goal of laser trimming is to control the resistance value with high precision, the accuracy of the length that is cut by the laser is crucial. As with every machine learning-based method, however, the proposed approach will inevitably exhibit some prediction error, either in the positive or in the negative direction. While typically very small, such error may result in a device that is outside its specification range. The existence of a secondary resistor (i.e. fine-trim) is, therefore, particularly important, as it provides the additional cushioning needed in case of overshooting and the compensation mechanism needed in case of undershooting. While such two-stage resistor configurations are extensively used in industry, a single-stage resistor is more economical. While our method can be applied to a single-stage resistor as well, the trade-off between trim-time savings and potential yield loss should be carefully analyzed prior to deployment of this solution.

IV. Wafer-Level Spatial Correlation Modeling

Recent research on modeling spatial measurement correlation has shown great promise in capturing wafer-level spatial variation and, thereby, reducing test cost of electrical measurements [3], [4], [6], [8]–[11]. The underlying idea is to collect measurements for a sparse subset of die on each wafer and subsequently train statistical spatial models to predict performance outcomes at unobserved die locations.

For example, in [9], the expectation-maximization (EM) algorithm is used to estimate spatial wafer measurements, assuming that data comes from a multivariate normal distribution and the Box-Cox transformation is used in case data is not normally distributed. The Virtual Probe (VP) approach [10] models spatial variation via a Discrete Cosine Transform (DCT) that projects spatial statistics into the frequency domain. The author of [8] laid the groundwork for applying Gaussian Process (GP) models to spatial interpolation of semiconductor data based on Generalized Least Square fitting and a structured correlation function. This model has been further enhanced with radial feature inclusion and introduction of a regularization parameter [3], [4], as well as a clustering approach to handle spatially discontinuous effects [6].

The GP approach works by extrapolating a function over a Gaussian random field on limited observations [12]. Consider a training set of nt data points $\{m_1, \ldots, m_{nt}\}$ located at the Cartesian coordinate denoted by $X = \{\mathbf{x}_1, \ldots, \mathbf{x}_{nt}\}$, $\mathbf{x} = [x, y]$. Using the GP approach, we define a Gaussian process as a collection of random variables $f(\mathbf{x}_i)$, $i = 1, \ldots, n_t$, for which any finite set of n_s function evaluations $f(\mathbf{x}_j)$, $j = 1, \ldots, n_s$, $n_s \leq n_t$ over the coordinates is jointly Gaussian-distributed. To derive a GP model for regression, we first consider a noise-free linear model:

$$f(\mathbf{x}) = \phi(\mathbf{x})^\top \mathbf{w} \tag{6}$$

where $\phi(\mathbf{x})$ is a function of $\mathbf{x}$ mapping the input columns into some high dimensional feature space, and $\mathbf{w}$ is the coefficient of the linear model which can be assigned a Bayesian prior such that $\mathbf{w} \sim \mathcal{N}(0, \Sigma_p)$. By assuming the random variables $f(\mathbf{x}_j)$ have zero mean, we can then specify the GP with mean and covariance functions:

$$\mathbb{E}[f(\mathbf{x})] = \phi(\mathbf{x})^\top \mathbb{E}[\mathbf{w}] = 0, \tag{7}$$

$$\begin{aligned}\mathbb{E}[f(\mathbf{x}) f(\mathbf{x}')] &= \phi(\mathbf{x})^\top \mathbb{E}[\mathbf{w}\mathbf{w}^\top] \phi(\mathbf{x}') \\ &= \phi(\mathbf{x})^\top \Sigma_p \phi(\mathbf{x}')\end{aligned} \tag{8}$$

It can be shown that the covariance function in (8) can be further written as a kernel function $k(\mathbf{x}, \mathbf{x}')$, which enables us to express the covariance between $f(\mathbf{x})$ and $f(\mathbf{x}')$ as a function of $\mathbf{x}$ and $\mathbf{x}'$, without explicitly computing $\phi(\mathbf{x})$. Any kernel function that satisfies Mercer's condition is a valid kernel function [13]. Once the covariance function is specified, for new input $\mathbf{x}_*$, we can readily predict $m_* = f(\mathbf{x}_*)$ by computing the conditional distributions of the joint Gaussian distribution.

In this work, the most important criterion for choosing the spatial correlation modeling method is computation time. Modern high-performance analog devices often have numerous laser-trimmable resistors which translates to an equal number of model fitting instances. The authors of [3] have compared the two state-of-the-art wafer-level spatial correlation modeling methods and showed that GP significantly outperforms VP in computation time. In particular, GP takes on average seven times less time than VP while offering equal or better accuracy and is, therefore, our choice for this work.

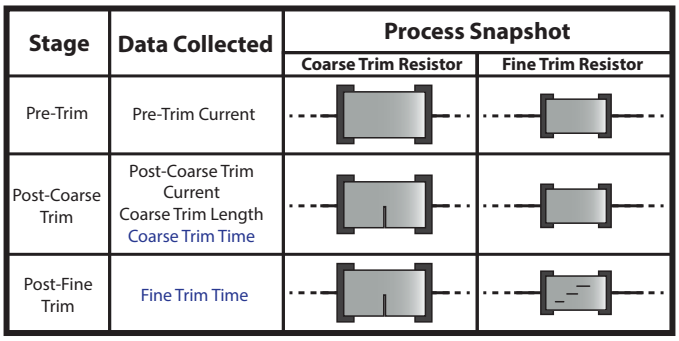

Fig. 6. Per stage data collection of the laser trimming process.

V. Experimental results

We now evaluate the effectiveness of the proposed method on two dual-stage laser-trimmed precision resistors on a current transmitter device. The resistors have a top hat geometry [7] and they are coarse-trimmed with a single plunge type cut [7]. Our dataset consists of one wafer with 1,924 devices, on which both coarse and fine laser trim has been performed for each of the two resistors of interest. Figure 6 shows the data that was collected during each stage of the process. Specifically, prior to trimming, the pre-trim current value is measured and logged. Coarse trim is then performed in a closed-loop, until the monitored current reaches the target value. At that point, the post-coarse trim current value, the coarse-trim length, and the coarse-trim time are logged. Subsequently, fine-trim is performed in a closed-loop, until the final current target is reached. The fine-trim time is then logged. In our analysis, current and length measurements are used for building the spatial correlation models, while time measurements are used for predicting the speed-up achieved by our method.

For the purpose of our experiment, we randomly sample 10% of the available die in order to build wafer-level spatial correlation models. Figures 7(a2) and 7(b2) show the sampled die locations for each resistor. We note that the same 10% sample is used for both resistors, emulating what would happen in manufacturing (i.e. the probe would collect all data from a limited sample of die). Using the spatial correlation models, we then predict the required coarse-trim length for the remaining 90% of the die on the wafer. As explained in Section III, we predict this coarse-trim length in three ways.

A. Length-based, original target prediction.

The first prediction method is based on the actual length that was coarse trimmed for the 10% sample of resistors. The conjecture is that the coarse-trim length required is spatially correlated. Hence, we can use this sample to build a GP wafer-level spatial correlation model that will predict the required length for the remaining 90% of the die on the wafer as a function of their die coordinate. Thereby, we can blindly perform coarse-trim in an open-loop by simply providing the length, which is faster than the closed-loop iterative laser firing and current monitoring method.

Figures 7(a1) and 7(b1) show the actual coarse-trim length across the entire wafer. As can be observed, spatial correlation indeed exists on the wafer, with a radial component being prominent. GP is very effective in modeling this spatial correlation based on the 10% sample. Indeed, this can be observed in Figures 7(a3) and 7(b3), where the predicted coarse-trim length wafer maps are shown for the two resistors. A visual comparison with the actual values confirms that the coarse-trim length can be accurately predicted by our method. For further visualization, the prediction error, which is the difference between the actual wafer maps (Figures 7(a1) and 7(b1)) and predicted wafer maps (Figures 7(a3) and 7(b3)), is also shown in Figures 7(a5) and 7(b5) for the two resistors, respectively. Evidently, the error variance is very low and balanced across the wafer. The maximum prediction error for Resistors A and B (corresponding to the yellow colored die on the error maps) is less than 3%, while the overall mean percent prediction error is 0.68% for Resistor A and 0.55% for Resistor B, as shown in the second column of Table I.

B. Rate-based, original target prediction.

The second method also seeks to predict the coarse-trim length but in an indirect way. Specifically, instead of building a wafer-level spatial correlation model for the coarse-trim length itself, we build a spatial correlation model for the coarse-trim rate. The trim rate is computed through Equation 3 using the collected pre-coarse trim current, post-coarse trim current, and coarse-trim length measurements on the 10% die sample. Then, using the trim rate predicted for each die as a function of its spatial coordinates, as well as the pre-coarse trim current measurement and the targeted post-coarse trim current measurement[1], we can predict the required coarse-trim length for each of the remaining 90% die locations.

The predicted wafer maps for the two resistors are presented in Figures 7(a4) and 7(b4), respectively, and the corresponding error maps in Figures 7(a6) and 7(b6), respectively. As can be observed, the trim rate-based method is also very effective in correctly predicting the required coarse-trim lengths. The overall mean percent prediction error is 0.78% for Resistor A and 0.76% for Resistor B, as shown in the third column of Table I. While this is slightly higher than the corresponding error of the length-based method, the maximum prediction error remains below 3%. This can also be verified by visual inspection of the Figures 7(a6) and 7(b6), where the highest colored value is similar to that of the length-based prediction error maps, shown in Figures 7(a5) and 7(b5).

TABLE I
Overall Mean Percent Prediction Error

Resistor	Length-based, Original Target	Rate-based, Original Target
A	0.68%	0.78%
B	0.55%	0.76%

[1]In order to accurately calculate the coarse-trim length prediction error of the rate-based method, the post-coarse trim current target value was set to the observed post-coarse trim current measurement for each die.

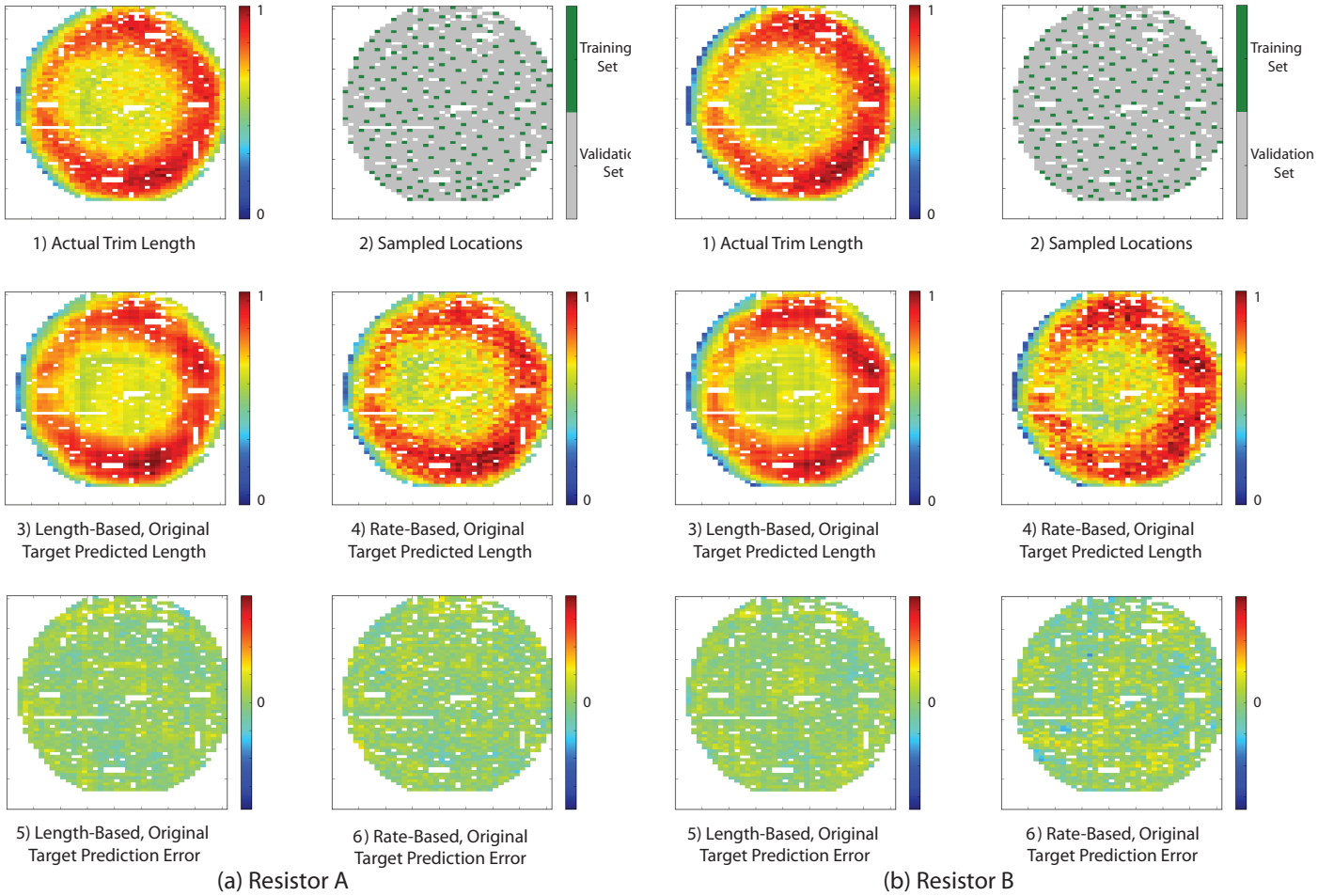

Fig. 7. Actual and predicted lengths for each proposed method.

In both of the above methods, the error maybe either in the positive or in the negative direction. We note that if this error results in a shorter laser cut by the coarse-trim stage, the fine-trim stage will have to compensate with a longer cuts(i.e. extra fine-trim time), while if the error results in a longer laser cut, the fine-trim will have to compensate with a shorter cut (i.e. less fine-trim time). In either case, the time savings from performing open-loop coarse-trim outweigh any additional fine-trim time. To evaluate the obtained speedup of open-loop over closed-loop coarse-trim, we measured the actual trim times on 200 die locations on a new, untrimmed wafer, on which we performed open-loop coarse-trim.

Accordingly, in the second and fourth column of Table II we report the expected average trim time per die for the closed-loop and open-loop case respectively, for each of the two resistors. As expected, there is a significant improvement in coarse-trim time, as a result of eliminating the need for the time-consuming closed-loop current monitoring. Note that the fine-trim time, reported in the third and fifth columns of this table, remains the same, as we are essentially trimming the same length in the coarse stage, whether in closed-loop or in open-loop configuration. The overall (i.e. coarse and fine-trim) average time for the two configurations and the speedup are shown in the second through fourth columns of Table III. As may be observed, the speedup is 1.25 for Resistor A and 1.32 for Resistor B, indicating that significant savings can be obtained by applying the proposed method, even if our coarse-trim target of the open-loop option remains the same as the original target of the closed-loop configuration.

C. Rate-based, optimized target prediction.

The third method takes advantage of the fact that the required coarse-trim length can be accurately predicted through the trim-rate estimated for each die location using a GP wafer-level spatial correlation model. Since the maximum prediction

TABLE II
AVERAGE TRIMMING TIMES PER DIE

Resistor	Closed-Loop		Open-Loop, Original Target		Open-Loop, Optimized Target	
	Coarse	Fine	Coarse	Fine	Coarse	Fine
A	312 ms	281 ms	190 ms	281 ms	233 ms	66 ms
B	338 ms	231 ms	200 ms	231 ms	244 ms	57 ms

TABLE III
TOTAL AVERAGE TRIMMING TIMES AND SPEEDUP PER DIE

Resistor	Closed-Loop	Open-Loop Original Target		Open-Loop Optimized Target	
	Total Time	Total Time	Speedup	Total Time	Speedup
A	593 ms	471 ms	1.25	299 ms	1.98
B	569 ms	431 ms	1.32	301 ms	1.89

error remains very low and the range of pre-trim to post-fine trim current values is known, we can adaptively choose a new, optimized coarse-trim target. Thereby, we can use the fast, open-loop, coarse-trim option to get closer to the final target, leaving less work for the slower fine-trim stage. To this end, we can use equation (5) to predict the trim lengths for the new optimized post-coarse trim current target. In our analysis, we set this target such that 75% of the fine-trim effort could be replaced by a more aggressive coarse-trim stage[2]. We note that this optimized target leaves plenty of margin so that even the maximal prediction error observed in our experiments would not overshoot the final post-trim target, therefore no yield loss is incurred by this method.

The sixth and seventh columns of Table II show the extrapolated trim times for this rate-based optimized-target coarse-trim length prediction method, while the fifth and sixth columns of Table III show the anticipated speedup over the baseline closed-loop method, which is estimated at 1.98 for Resistor A and 1.89 for Resistor B, respectively. Based on these promising results, in our future work we plan to deploy and evaluate the rate-based optimized target method on a larger-scale experiment.

VI. CONCLUSION

The key conjecture corroborated by the research described in this paper is that the physical parameters which are typically calibrated through IC laser trimming are spatially correlated. Therefore, wafer-level spatial correlation modeling methods, which have previously been introduced and leveraged for electrical test cost reduction, may also be used to reduce the cost of the expensive and time-consuming IC laser-trimming process. Experimental results with two laser-trimmed precision resistors on a wafer of $\sim$2K devices indicate that almost half of the time needed for laser trimming can be eliminated without impacting yield, thereby offering substantial savings in high volume production of such devices.

VII. ACKNOWLEDGEMENT

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[2]An NDA under which this data was provided to us prevents us from disclosing the actual current values.

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