An Adaptive Checker for the Fully Differential Analog Code

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***Abstract*—This paper discusses the design of an adaptive checker for concurrent error detection in fully differential analog circuits. The checker monitors the fully differential analog code, which states that, in nominal operation, the common mode signal of any symmetric node pair remains within a narrow band around the quiescent DC bias. The checker measures the common mode voltage and reports an error whenever the measured value exceeds a threshold. Its key feature is that this comparison threshold is dynamically adjusted in order to lower the probability of false alarms. The design was fabricated in a 0.5-μm CMOS technology. The chip test results prove the feasibility of the adaptive thresholding concept.**

***Index Terms*—Analog circuit testing, checkers, concurrent error detection, fully differential circuits.**

I. Introduction

MISSION-CRITICAL applications require *concurrent error detection* (CED) mechanisms in order to monitor the operation of each circuit and issue alert signals whenever errors occur. In the past, the problem of CED has been studied for several classes of analog circuits, such as switched-capacitor filters [1], linear time-invariant circuits [2], A/D converters [3] and OTA-C filters [4]. A formal theory on the self-checking properties of analog and mixed signal circuits is presented in [5]. In this paper, we propose a checker for performing CED in *fully differential* (FD) analog circuits. FD realizations are preferable for high-accuracy applications since they double the effective voltage swing and, in addition, they tend to cancel out clock feedthrough effects, power-supply noise, $1/f$ noise and other common-mode signals.

In FD analog circuits, signals are carried in two physically distinct signal paths that are symmetrical. The signal pair corresponding to two symmetrical nodes of the paths is called the *conjugate pair*. The small-signal voltages of a conjugate pair have equal magnitude and opposite polarity. Thus, at any time, the common-mode voltage of a conjugate pair equals the quiescent bias voltage. A fault that manifests itself during the lifetime of the circuit, or a transient that does not translate into a common-mode signal, will affect the two signal paths distinctively, thus it will corrupt the balance of the circuit, shifting the common-mode voltage of a conjugate pair away from the specified bias. The steady common-mode voltage can be viewed as an inherent *invariant* property of nominal FD circuits. This property stems from the redundancy that is encoded in FD signals and is referred to as *fully differential analog code* (FDAC). In practice, the common-mode voltage is likely to vary due to finite common-mode rejection ratio, limited common-mode feedback bandwidth, clock feedthrough and nominal process drifts. Thus, two signals are deemed FD, i.e., they satisfy the FDAC, if their common-mode voltage, $v_{\rm com}$, lies within a tolerance band around the bias:

$$|v_{\rm com} - V_b| < \text{threshold} \tag{1}$$

where $v_{\rm com} = (V^+ + V^-)/2$, $V^\pm = v^\pm + V_b$, and (v^+, v^-), V_b denote the small-signal voltages and the quiescent DC bias value of the conjugate pair, respectively.

CED mechanisms for FD circuits consist of checkers that monitor a select set of conjugate nodes across the signal path and provide an error indication whenever the above inequality is violated. In [6]–[8], the authors discuss the design of checkers that compare the common-mode voltage to a static threshold,[1] i.e., they monitor a *static* FDAC. A static threshold, however, is lenient for relatively small signals and restrictive for relatively large signals, resulting in inadvertent false alarms. In order to minimize the occurrence of false alarms, it is therefore necessary to impose an input-referred threshold, i.e., a threshold that adapts to the amplitude of the monitored conjugate pair. This threshold definition results in a *dynamic* FDAC.

The inefficiency of the static threshold was first observed in [11], where the common-mode voltage is compared to a threshold that varies proportionately to the average absolute amplitude of the conjugate signals. The comparison is decomposed into two signal inequalities, which are examined consecutively by a sample and compare switched-capacitor circuit. The high-frequency components of the conjugate pair need to be much smaller than the clock frequency at which the sampling and comparison operations are performed. In addition, clock feedthrough may jeopardize the error detection capability when small amplitude signals are processed. In the worst case scenario, and unless an autozeroing technique is employed, clock feedthrough may have an accumulative effect that, eventually, will lead to misguided decisions.

In this paper, we describe the design of a checker for the dynamic FDAC, which compares uninterruptedly at frequencies close to the limits imposed by the technology. The underlying principle of the design is a window comparator with infinite programmability, which emulates the dynamic tolerance band of the monitored common-mode signal. The design was fabricated using the $C5N$ 0.5-μm minimum feature size, n-well, double-polysilicon, three-metal process provided by MOSIS.

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[1]Checkers have also been used as a design for off-line testability of FD analog circuits in [9] and [10].

The rest of this paper is organized as follows. In Section II, we define the dynamic FDAC. In Section III, we present in detail the design of the adaptive checker that examines the dynamic FDAC. In Section IV, we present test results from the fabricated chip. Section V concludes the paper.

II. Adaptive Threshold

The advantage of an adaptive over a static threshold will be explained with the help of Fig. 1(a), which represents the entire space of conjugate signals (v^-, v^+).

Let V_δ denote the static threshold. The parallel continuous lines $v^+ = -v^- \pm 2 \cdot V_\delta$ bound the area of conjugate pairs that satisfy the static FDAC. A fault or transient translates into a percentile shift in the common mode voltage of the monitored conjugate pair. For conjugate signals with relatively small amplitudes, a static threshold is lenient and, thus, it may not suffice to detect an unacceptably large percentile shift, resulting in false positives. Similarly, for conjugate signals with relatively large amplitudes, a static threshold is restrictive and, thus, it may inadvertently indicate acceptable small percentile shifts as errors, resulting in false negatives. The shaded areas in Fig. 1(a) contain the FD space where the static FDAC is prone to erroneous decisions. In the case of conjugate pairs with wide dynamic range, the threshold should adapt to the absolute amplitude of the conjugate pair, in order to lower the probability of false alarms.

The adaptive threshold is defined as

$$V'_\delta = \epsilon_r \cdot \left(|v^+| + |v^-|\right) + \alpha \cdot V_\delta \tag{2}$$

where ϵ_r is a positive constant that defines the amplitude dependence and $\alpha \cdot V_\delta$, $0 < \alpha < 1$, is a static threshold that compensates for nominal offset errors and process drifts. This threshold definition results in an FDAC that is dynamically adjusted as the conjugate pair voltages evolve in time. The piece-wise linear dashed boundaries $v^+ = -v^- \pm 2 \cdot V'_\delta$ in Fig. 1 surround the valid dynamic FDAC area. The dynamic FDAC minimizes the occurrence of false alarms since it moderates the bias of the static FDAC toward rejecting large amplitude conjugate pairs and accepting small amplitude conjugate pairs.

The FDAC can be equivalently expressed in terms of the differential and common-mode voltages of the conjugate pair:

$$|v_{\rm com} - V_b| < \epsilon_r \cdot |v_{\rm diff}| + \alpha \cdot V_\delta. \tag{3}$$

The codeword region boundaries in the $(v_{\rm com}, v_{\rm diff})$ space are shown in Fig. 1(b). If we define the signal coding quality [11] as

$$Q = \frac{|v_{\rm diff}|}{|v_{\rm com} - V_b|} \tag{4}$$

then, for a perfect differential conjugate pair, $Q = \infty$. The larger the Q, the more likely it is that the circuit operates correctly.

III. Checker Design

The proposed checker for FD analog circuits monitors simultaneously the following two inequalities: $v_{\rm com} - V_b < V'_\delta$ and $v_{\rm com} - V_b > -V'_\delta$. Thus, fundamentally, it operates as a window comparator with variable window width. Since V'_δ is a continuous function of $|v^+| + |v^-|$, window comparators with discrete width programmability [12], [13] are not suitable. In the following section, we discuss a novel design where the width depends linearly on a differential voltage pair. The circuits that deliver the necessary control voltages to the comparator are discussed in Sections III-B and III-C.

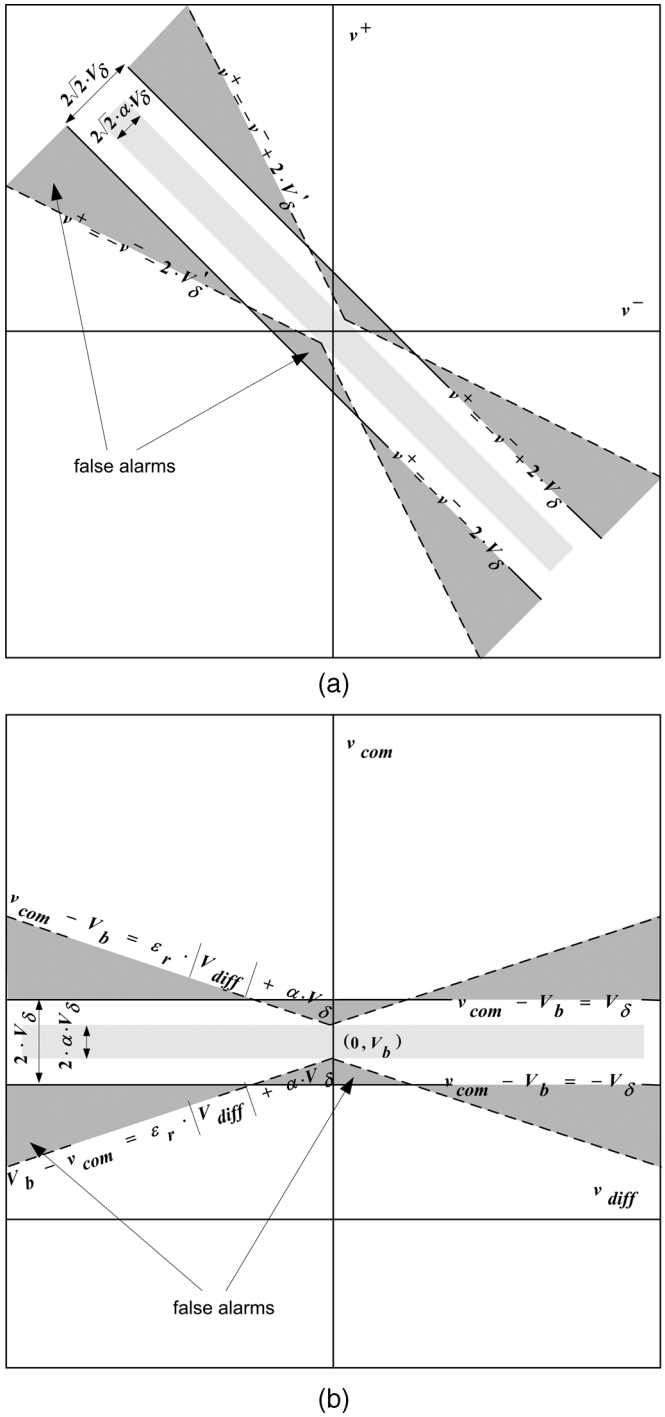

Fig. 1. Fully differential analog encoding.

A. Variable Window Comparator

The schematic of the window comparator is shown in Fig. 2. It consists of two modified inverters that share a common input

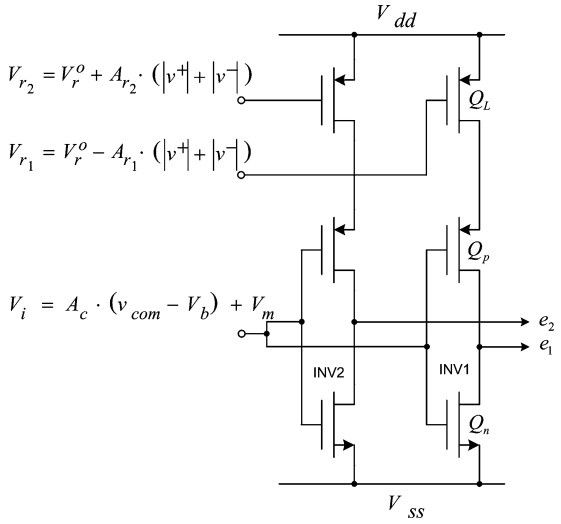

Fig. 2. Schematic of the variable window comparator.

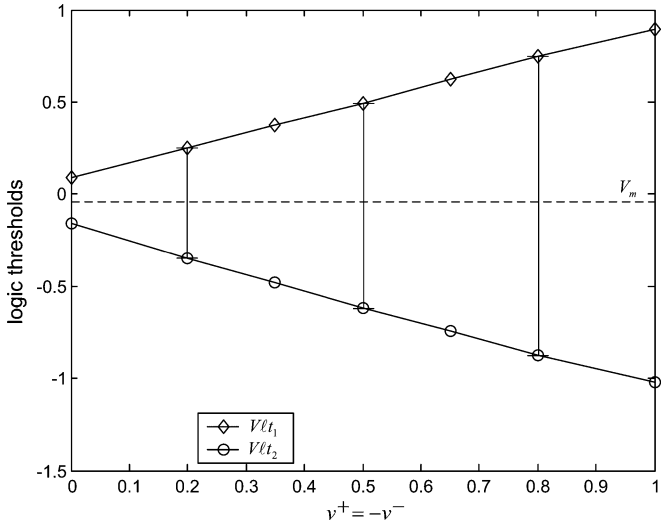

Fig. 3. Measured relation between logic thresholds and the amplitude of an FD signal pair.

$V_i = A_c \cdot (v_{\rm com} - V_b) + V_m$. The modified inverters are composed of a regular complementary CMOS inverter and a load transistor Q_L connected between the source of the pMOS device and the positive supply. The gate voltages of the load transistors are given by $V_{r_{1,2}} = V_r^o \mp A_{r_{1,2}} \cdot (|v^+| + |v^-|)$.

Due to the symmetry of the circuit, we narrow our discussion to the operation of the modified inverter. Let $V_{\ell t}$ denote its logic threshold. When the output switches states, i.e., when $V_i = V_{\ell t}$, both devices of the regular inverter operate in the saturation region. The logic threshold can be found by setting $-I_{ds_{Qp}} = I_{ds_{Qn}}$:

$$V_{\ell t} = \frac{V_{ss} + V_{tn} + \sqrt{\frac{2 \cdot \beta_p}{\beta_n}} \left(V_{D_{QL}} + V_{tp}\right)}{1 + \sqrt{\frac{2 \cdot \beta_p}{\beta_n}}}. \tag{5}$$

Thus, $V_{\ell t}$ is controlled by the drain voltage $V_{D_{QL}}$ of Q_L. The control voltage V_r is maintained smaller than $V_{D_{QL}} - |V_{tp}|$ in order to ensure that Q_L operates in the triode region at the time of the transition. Suppose now that the circuit operates at $V_i = V_{\ell t}$. In this region, Q_n behaves like an ideal current source. If we increase V_r, then $V_{GS_{QL}}$ decreases and, thus, $V_{D_{QL}}$ drops in order to maintain the current equilibrium $I_{ds_{Qn}} = -I_{ds_{QL}}$. From (5), this reduces the logic threshold of the inverter, shifting its transfer characteristic to the left. Similarly, if V_r decreases, then $V_{D_{QL}}$ rises, resulting in an increase of $V_{\ell t}$ and a corresponding shifting of the transfer characteristic to the right. To a good approximation, $V_{\ell t}$ and V_r satisfy a linear relationship:

$$V_{\ell t} \simeq V_{\ell t}^o - |k| \cdot (V_r - V_r^o). \tag{6}$$

The pMOS devices of the modified inverters are designed to be asymmetric with $\beta_{p_2} < \beta_{p_1}$, such that their logic thresholds satisfy $V_{\ell t_2}^o < V_{\ell t_1}^o$ when $|v^+| = |v^-| = 0$. We define V_m to be

$$V_m = \frac{V_{\ell t_1}^o + V_{\ell t_2}^o}{2}. \tag{7}$$

Thus, $V_{\ell t_1}^o - V_m = V_m - V_{\ell t_2}^o = d^o$. This asymmetry results in a different $|k|$ in (6) for each of the two inverters. In order to have equidistant shifts of the logic thresholds from V_m, the gains A_{r_1} and A_{r_2} are chosen to satisfy $|k_1| \cdot A_{r_1} = |k_2| \cdot A_{r_2} = |k^*|$. Thus, under the above conditions, substituting the expressions of the control voltages V_{r_1}, V_{r_2} in (6) yields

$$V_{\ell t_{1,2}} \simeq V_{\ell t_{1,2}}^o \pm |k^*| \cdot \left(|v^+| + |v^-|\right). \tag{8}$$

The result in (8) indicates that the logic thresholds follow bidirectionally the changes in $|v^+| + |v^-|$, such that the equality $V_{\ell t_1} - V_m = V_m - V_{\ell t_2}$ is always satisfied. Fig. 3 shows the measured relation between the logic thresholds and $|v^+| + |v^-|$, when the signal pair (v^+, v^-) is FD.

Let the distance d be $d = V_{\ell t_1} - V_m = V_m - V_{\ell t_2}$. The circuit examines whether V_i remains within a window $V_{\ell t_1} - V_{\ell t_2} = 2 \cdot d$ centered at V_m, i.e., it examines the inequality $|V_i - V_m| < d$. Substituting the expressions of V_i and the distance d, this inequality can be rewritten as

$$\begin{aligned} \frac{|v^+ + v^-|}{2} &< A_c^{-1} \cdot \left(d^o + |k^*| \cdot \left(|v^+| + |v^-|\right)\right) \\ &< V_\delta' \end{aligned} \tag{9}$$

provided that

$$\alpha \cdot V_\delta = A_c^{-1} \cdot d^o \tag{10}$$

$$\epsilon_r = A_c^{-1} \cdot |k^*|. \tag{11}$$

From (11), it is seen that, for a specific value of $|k^*|$, the error threshold ϵ_r is set to the desired value by assigning an appropriate gain A_c. For the selected A_c and the desired static threshold $\alpha \cdot V_\delta$, the geometry of the regular inverters is chosen such that the initial distance d^o satisfies (10). Given the geometry of the regular inverters, the slopes A_{r_1} and A_{r_2} are adjusted accordingly such that $|k^*|$ has the value assumed

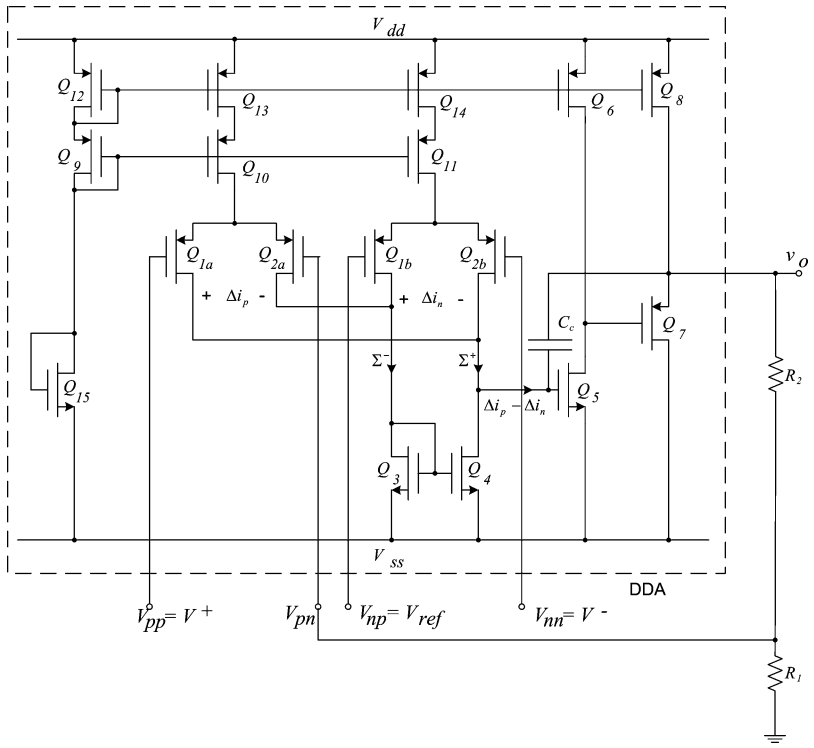

Fig. 4. CMOS realization of a differential difference amplifier.

initially. Note that, since $\alpha \cdot V_\delta$ and ϵ_r are statistical quantities, making (10) and (11) strict equalities is not a concern.

According to (9), the circuit examines the dynamic FDAC. In essence, it models a window comparator, permanently centered at the bias V_b, with edges that adjust dynamically to $V_b + V'_\delta$ and $V_b - V'_\delta$. The two bit digital output assumes one out of three possible value combinations:

$$e_1e_2 = \begin{cases} 00 & : \quad v_{\rm com} > V_b + V'_\delta \\ 10 & : \quad |v_{\rm com} - V_b| < V'_\delta \\ 11 & : \quad v_{\rm com} < V_b - V'_\delta. \end{cases} \tag{12}$$

The output $e_1e_2 = 10$ indicates correct operation, while $e_1e_2 = 00$ and $e_1e_2 = 11$ indicate a violation of the FDAC. In particular, the first modified inverter is triggered by unacceptably large positive shifts of the FDAC and the second one by unacceptably large negative shifts.

In the following sections, we discuss the circuits that generate V_i and the control voltages V_{r_1} and V_{r_2}.

B. Differential Difference Amplifier

The circuit that delivers the desired input V_i to the comparator is based on a differential difference amplifier (DDA) [14]. A CMOS realization of the DDA is shown in Fig. 4. It is a two-port input device with input terminals designated as V_{pp}, V_{pn} for the noninverting input port and V_{np}, V_{nn} for the inverting input port. This circuit extends the concept of the classical op-amp. If it is completed with a negative feedback network, then it virtually shorts its two differential inputs:

$$V_{pp} - V_{pn} = V_{np} - V_{nn}. \tag{13}$$

The operation of the DDA is as follows. The transconductance elements (Q_1–Q_2) convert the voltage differences $\Delta v_p = V_{pp} - V_{pn}$ and $\Delta v_n = V_{np} - V_{nn}$ into two current differences Δi_p and Δi_n. If $|\Delta v_{p,n}|$ remains smaller than $\sqrt{I_c/\beta}$, where β stands for the geometry-dependent amplification factor of the matched transistors Q_1 and Q_2, then both Q_1 and Q_2 operate in the saturation region. Under this condition, the current differences $\Delta i_{p,n}$ are given by

$$\Delta i_{p,n} = \frac{\Delta v_{p,n}}{|\Delta v_{p,n}|} \cdot \frac{I_c}{2} \sqrt{1 - \left(1 - \frac{\beta \Delta v_{p,n}^2}{I_c}\right)^2}. \tag{14}$$

The outputs of the transconductance elements are directly cross-connected to two summing buses Σ^+ and Σ^-. The high-gain output stage is composed of a current mirror (Q_3–Q_4) that converts the buses into a single-ended current $\Delta i_p - \Delta i_n$ and a standard integrator (Q_5–Q_6, C_c) followed by a buffer stage (Q_7–Q_8). Thus, the output of the circuit is given by

$$v_o = \mu[\Delta i_p - \Delta i_n], \quad \mu \gg 1. \tag{15}$$

Since $\Delta i_{p,n}$ are identical functions of $\Delta v_{p,n}$ and invertible for the specified $\Delta v_{p,n}$, the output can be equivalently rewritten as $v_o = \mu^*[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})]$, $\mu^* \gg 1$.

For the resistive feedback network shown in Fig. 4 and for $V_{pp} = V^+$, $V_{nn} = V^-$, $V_{np} = V_{\rm ref}$, (13) yields

$$\begin{aligned} v_o &= \left(1 + \frac{R_2}{R_1}\right) \cdot (V^+ + V^- - V_{\rm ref}) \\ &= A_c \cdot (v_{\rm com} - V_b) + V_m \end{aligned} \tag{16}$$

where

$$A_c = 2 \cdot \left(1 + \frac{R_2}{R_1}\right)$$

and

$$V_{\text{ref}} = 2 \cdot \left(V_b - A_c^{-1} V_m\right).$$

The reference voltage is used to cancel out the nominal DC component of the conjugate pair and, in addition, to bias the output of the DDA to the middle point V_m of the comparison window.

C. Full Wave Rectifier

For the purpose of generating the window's width control voltages V_{r_1} and V_{r_2}, it is required to rectify each conjugate signal separately and, subsequently, sum up the rectified signals. If, however, the conjugate signals remain differential, then we can write $|v^+| + |v^-| = |v^+ - v^-|$ and rectify the difference voltage $v^+ - v^-$ instead, which requires a much simpler circuit that occupies less area. The error induced by implementing a threshold $V_\delta'' = \epsilon_r \cdot |v^+ - v^-| + \alpha \cdot V_\delta$, instead of the theoretical definition in (2), is shown graphically in Fig. 5, which is a zoomed version of Fig. 1(a) near the origin. Fig. 5 shows the allocation of the boundaries for the two different threshold definitions in the space where the conjugate signals cease being differential. In this region, $|v^+ + v^-| = |v^+| + |v^-|$. Thus, the boundary corresponding to V_δ' is composed of the conjugate signals that satisfy $(0.5 - \epsilon_r) \cdot (|v^+| + |v^-|) = \alpha \cdot V_\delta$ and the boundary corresponding to V_δ'' is composed of the conjugate signals that satisfy $(0.5-\epsilon_r)\cdot|v^+|+(0.5+\epsilon_r)\cdot|v^-| = \alpha\cdot V_\delta$, for $|v^+| > |v^-|$, and $(0.5+\epsilon_r)\cdot|v^+|+(0.5-\epsilon_r)\cdot|v^-| = \alpha\cdot V_\delta$, for $|v^+| < |v^-|$. The shaded regions between the two boundaries comprise the conjugate pairs that would be erroneously evaluated by using the new threshold V_δ'' instead of V_δ'. The area of these regions is very small since, typically, $\epsilon_r < 0.1$. Furthermore, V_δ' in (2) is not exact, since it contains statistically defined quantities. Thus, we consider V_δ'' to be an equally satisfactory definition. Under this condition, the control voltages correspond to a negative and positive full-wave rectification of the conjugate signals' difference.

A high-level description of the circuit that generates V_{r_1} and V_{r_2} is shown in Fig. 6. It is based on a fully differential transconductance amplifier with two decoupled output stages, as shown in Fig. 7. The currents flowing out of the two output ports satisfy $i_{p,n}^+ = -i_{p,n}^-$. Due to the inherent symmetry of the circuit, we narrow our discussion to the operation of the left-hand part. Negative currents i_n^+ and i_n^- flow through the diodes D_{1a} and D_{2a}, respectively. Two clamp diodes, D_{1b} and D_{2b}, are connected to the cathodes of D_{1a} and D_{2a}, in order to provide a path for positive output currents i_n^+ and i_n^-. The negative source $V_{BBn} = 2V_T$, where V_T is the threshold voltage of a diode, prepares the diode pairs for conduction at the beginning of a cycle. Due to this pre-bias condition, at high frequencies the rectifier recovers at a rate comparable to $d(v^+ - v^-)/dt$, introducing a minimal distortion during the zero crossing of $v^+ - v^-$.

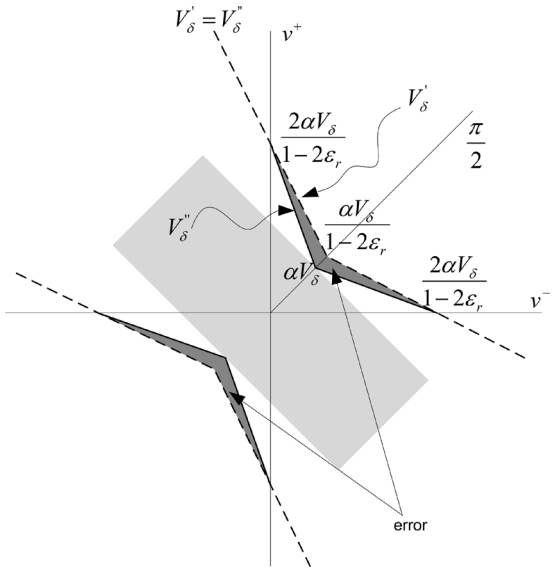

Fig. 5. Error induced by implementing the threshold $V_\delta'' = \epsilon_r \cdot |v^+ - v^-| + \alpha \cdot V_\delta$ instead of V_δ'.

The equivalent CMOS circuit shown in Fig. 8 was used to implement the circled pre-biased diode of Fig. 6 [15]. The circuit has matched transistor pairs Q_{27a}, Q_{27b} and Q_{28a}, Q_{28b}. The voltage divider (Q_{25}–Q_{26}) sources a small current to the diode-connected transistors Q_{27a} and Q_{28a}, such that a constant voltage $V_{G_{Q27a}} - V_{G_{Q28a}} \simeq V_{T_{Q27}} + V_{T_{Q28}}$, where $V_{T_{Q27}}$, $V_{T_{Q28}}$ denote the threshold voltages of Q_{27} and Q_{28}, is generated across their gates. This voltage is also shared by Q_{27b} and Q_{28b}, thus it keeps them ready for conduction. The common node of Q_{27a} and Q_{28a} is connected to a voltage source V_x that is equal to the DC value of the input node. Negative input currents flow through Q_{27b} to the output node, driving Q_{28b} into cut-off. In contrast, positive input currents flow through Q_{28b} to ground, driving Q_{27b} into cut-off. Therefore, the circuit in Fig. 8 operates as a class-AB negative rectifier. The output current flows through a resistor R_{rec-}, whose value defines the slope of the rectification. Similarly, the positive pre-biased diode rectifiers at the right-hand side of Fig. 6 are implemented by connecting the drain of Q_{27b} to the positive supply and using the drain of Q_{28b} as the output node. Fig. 9 shows a measured transient response of the positive full-wave rectifier for a conjugate pair of 10-kHz sinusoidal signals.

IV. Measurements

The checker was fabricated using the $C5N$, 0.5-μm minimum feature size, n-well, double-polysilicon, three-metal process provided by MOSIS. A microphotograph of the circuit layout is shown in Fig. 10. Certain differential transistor pairs were arranged in common-centroid geometries in order to achieve better matching properties. Dummy structures were also used in places, in order to create identical environments.

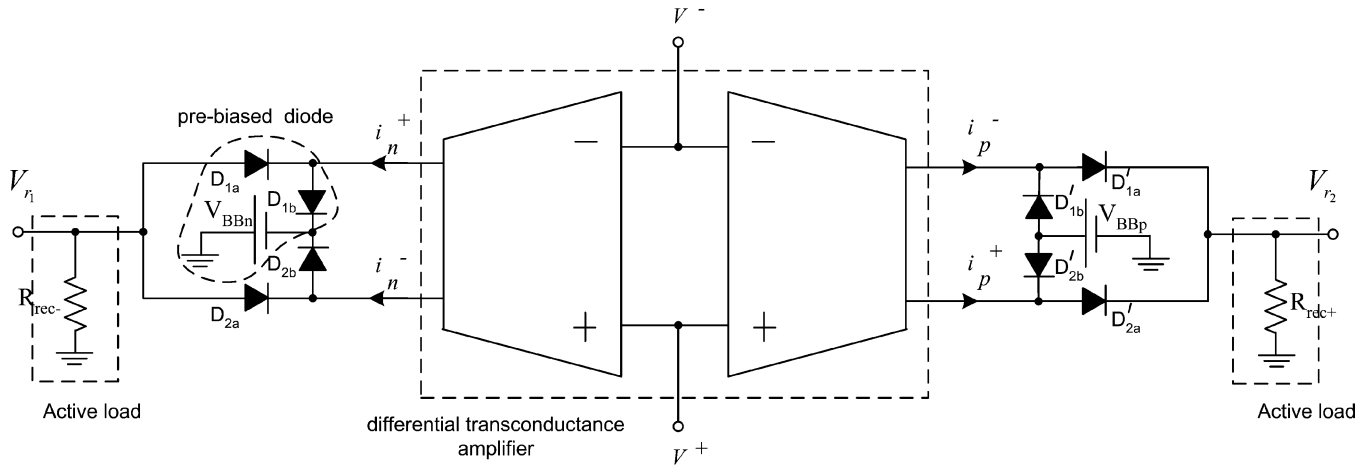

Fig. 6. Full-wave rectifier.

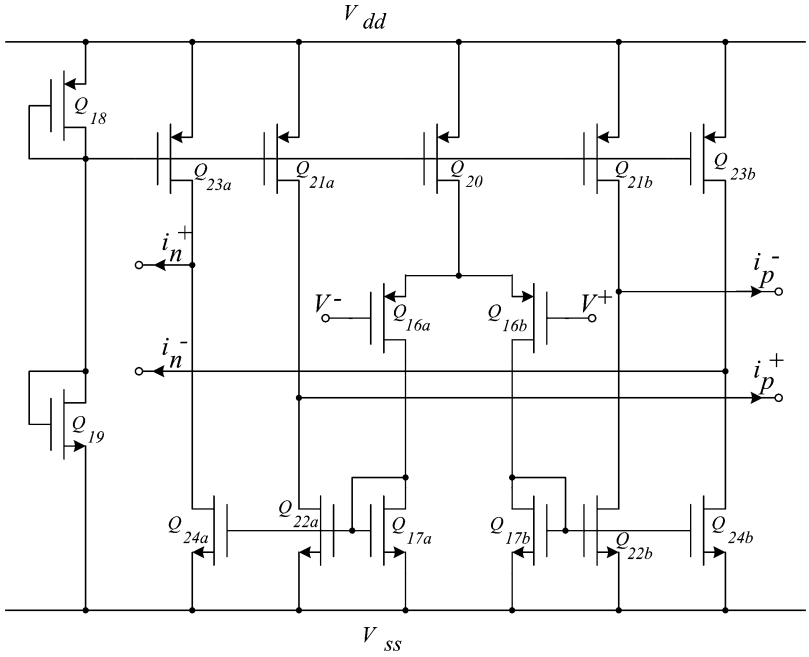

Fig. 7. Differential transconductance amplifier.

The comparator is shielded with a p^+ guard ring to reduce the transmittance of switching noise to the sensitive analog circuitry. For this purpose, we are also using distinct power supply buses with separate bonding pads for the comparator and the analog circuitry. Note that the feedback resistors R_1 and R_2 of the DDA are not integrated, but, instead, we chose to connect them externally in order to be able to calibrate the circuit for different error thresholds ϵ_r.

The checker occupies 0.058 mm^2 and runs from symmetrical bipolarity supplies of ± 5 V. Its speed is primarily limited by the rise and fall times of the output modified inverters, since they are not necessarily of minimum size. The dynamic threshold assignment is affected in high frequencies due to the phase lag between the DDA and full-wave rectifier paths. The checker is observed to operate correctly for frequencies up to 100 kHz. The average power dissipation for the experiments below is around 20 mW (the power supplies draw, on average, a 2-mA current). The checker requires one pin since its two bit digital output can be XNORed. The reference potential $V_{\rm ref}$ can be generated on-chip.

Fig. 11 shows the measured boundaries allocated by the checker in the space of conjugate signals (v^+, v^-) for three different gains A_c. These curves are obtained by first assigning a specific voltage to v^+, then varying v^- and marking the values of v^- that trigger the output of the modified inverters. The procedure is repeated for several values of v^+ in order to obtain a representative number of points along each boundary.[2] The picture matches well the encoding proposed in Fig. 1.

[2]In order to ensure that the CED scheme satisfies the totally self-checking goal [5], i.e., that the checker is triggered if and only if a noncodeword input occurs, this procedure can be applied periodically during idle times, in order to test the checker.

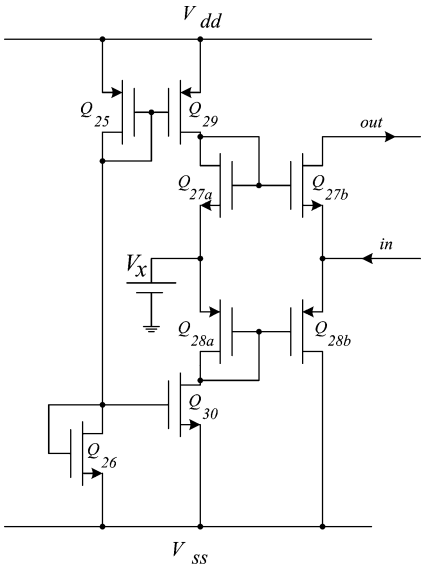

Fig. 8. Pre-biased CMOS diode implementation.

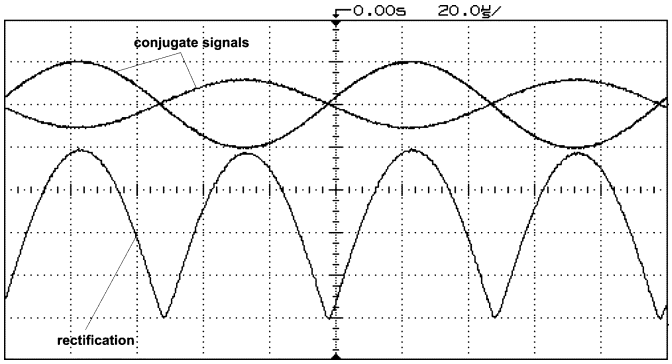

Fig. 9. Measured response of the rectifier for a sinusoidal conjugate pair.

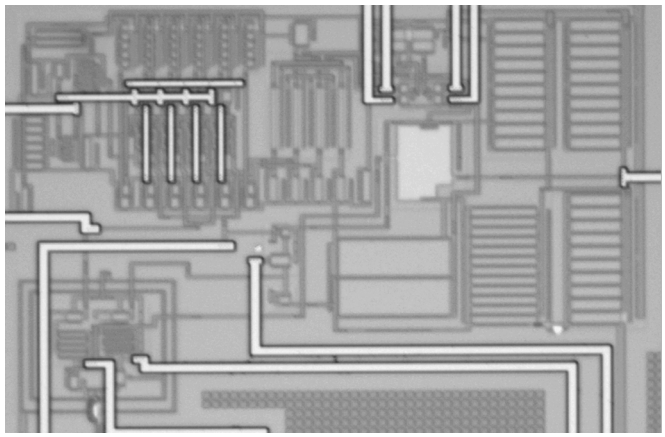

Fig. 10. Microphotograph of the fabricated chip.

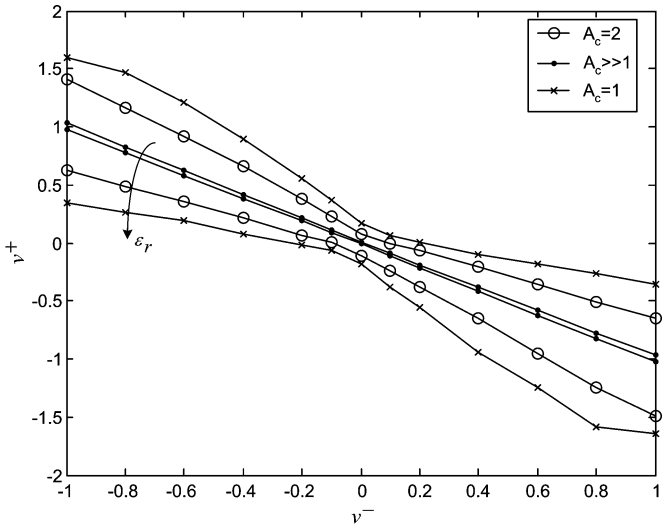

Fig. 11. Measured boundaries in the space of conjugate signals.

For $A_c \gg 1$, i.e., $R_2 \gg R_1$, the boundaries reduce to two parallel lines indicating a static behavior. This is compatible with (11), which yields $\epsilon_r \simeq 0$ and, thus, from (2), $V'_\delta = \alpha V_\delta$. For $A_c \simeq 1$, i.e., $R_2 \ll R_1$, the error threshold obtains its maximum possible value $\epsilon_r \simeq |k^*|$ indicating the maximum possible opening for the funnel-shaped code-word space. For $A_c = 2$, i.e., $R_2 = R_1$, the error threshold obtains an intermediate value between the above limits. Since we do not have the option to modify on chip the width $2 \cdot d^o$ of the window for zero conjugate signals, αV_δ from (10) becomes an inverse function of A_c, thus it increases as ϵ_r increases. The nonlinearity of the boundaries for maximum ϵ_r, which is observed for large conjugate signals, is attributed to the saturation of the DDA. In the following experiments, the threshold resulting from $A_c = 2$ is used, corresponding to $\alpha \cdot V_\delta \simeq 53$ mV and $\epsilon_r \simeq 0.1$. The respective threshold for $A_c = 1$ is $\epsilon_r \simeq 0.182$.

The response of the checker for an input conjugate pair with phase lag is shown in Fig. 12. The checker indicates $e_1e_2 = 11$ whenever the common-mode voltage is negative and unacceptably large and $e_1e_2 = 00$ whenever the common-mode voltage is positive and unacceptably large. During the time where the signals satisfy the FDAC, the checker indicates correct operation $e_1e_2 = 10$.

Fig. 13 shows the response of the checker for a conjugate pair that is fully differential during the first half of the period and differs by a constant voltage $v_p = 0.1$ V during the second half. This input pair was obtained by summing an input pulse to the v^- signal, with step from zero to $-v_p$. During the time where $v^+ + v^- = 0$, the checker indicates correct operation $e_1e_2 = 10$. When the pulse is active, the checker indicates erroneous operation only when the conjugate signals have small enough amplitudes. From a certain amplitude and upwards, the constant discrepancy of 0.1 V becomes relatively small and, thus, ceases to corrupt the FDAC. In essence, in this measurement, the conjugate pair moves across the line $v^+ + v^- = -v_p$ while the pulse is low. The inverters are triggered at the points where this line crosses the boundary.

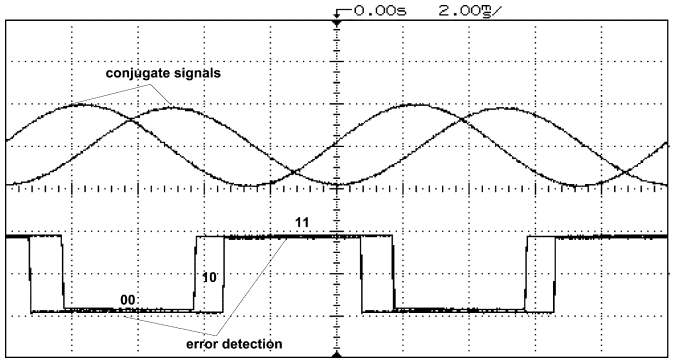

Fig. 12. Circuit response to a conjugate pair with phase lag.

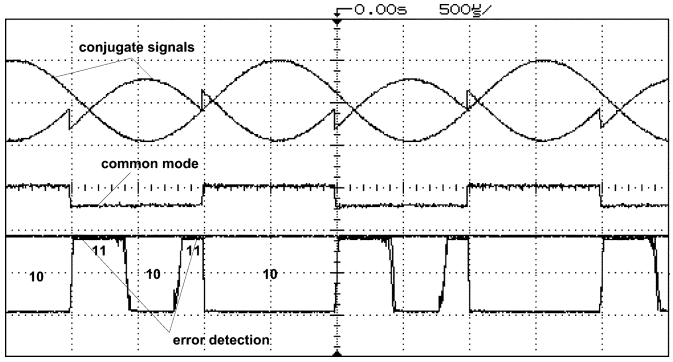

Fig. 13. Circuit response to a conjugate pair with common-mode voltage offset.

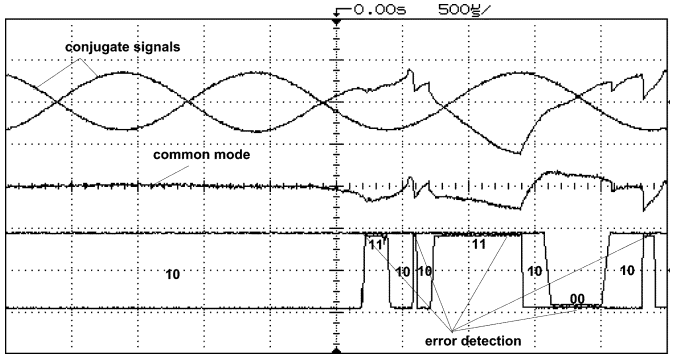

Fig. 14. Circuit response to a transient error.

As a last measurement, we examine the response of the checker to a transient error. Such errors inject a charge on a node that temporarily alters the form of the conjugate signals. For the purpose of modeling a transient error, we added an abrupt arbitrary signal to v^- for a short time interval. Fig. 14 shows the response of the checker. It can be seen that the checker detects the unacceptable deviation of the common-mode voltage in both directions by raising e_2 or lowering e_1.

V. Conclusion

We introduced and characterized experimentally an adaptive checker for concurrent error detection in fully differential analog circuits. The checker is based on a window comparator with continuous width updates. It examines the fully differential analog code by comparing the common mode signal of a conjugate pair to a threshold value. The checker moderates the bias of the threshold by adjusting it dynamically to the amplitude of the conjugate pair. The results from the fabricated chip show that the boundary allocated in the space of conjugate signals coincides with the proposed dynamic fully differential analog code.

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