Knob Non-Idealities in Learning-Based Post-Production Tuning of Analog/RF ICs: Impact & Remedies

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***Abstract*—As CMOS technology continues to scale down, the effect of process variations on yield and performance of analog/RF ICs is becoming more prominent. To counteract this effect, learning-based post-production tuning has been proposed, wherein regression functions are trained and used to adjust tunable knobs based on low-cost alternate tests, thereby improving the performances of a circuit and, by extension, increasing yield. Of course, tunable knobs are also subject to process variations; yet this is not an issue when the knobs are part of the procedure that generates the data with which the regression models are trained, as this data reflects the impact of process variations on both the tunable circuit and the knobs. In various cases, however, such as in heterogeneous integrated systems, 3D ICs, or multi-chip modules, the knob circuitry may not be integrated on the same die, thereby limiting our ability to obtain a comprehensive set of training data. Accordingly, in this work we investigate the impact of knob non-idealities which are not captured in the training data, on the ability of the learned regression functions to accurately predict the optimum knob position that maximizes the performance of a circuit. Using a tunable cascode low-noise amplifier (LNA) fabricated in 130nm CMOS process, alongside external knobs designed as linear low drop out regulators (LDOs) and voltage dividers operating on the bias voltages of the LNA, we first quantify this impact. Then, we demonstrate that by explicitly introducing "noise" in the knob output values used during training set generation, we can effectively alleviate external knob non-idealities and improve quality of tuning.**

I. Introduction

Scaling of CMOS technologies into the deep sub-micrometer regime is driven by two main reasons: (i) ultra low-power requirements, and (ii) high frequency operation of analog/RF ICs used in communications, medical and automotive applications. To accommodate power requirements in the order of μW and operating frequencies close to or higher than mm-wave, i.e., 30GHz and above, which seems to be the case for 5G next-generation communication networks, the only viable solution is to use advanced CMOS technology nodes due to their low supply voltages and high transit frequencies. Despite the many advantages CMOS scaling offers, several disadvantages also occur, among which process variations proves to be the one that most greatly impacts performance of analog/RF ICs. As a consequence, fabricated analog/RF ICs experience significant shifts from their expected performance, which results in an increase in yield loss.

To address this issue, circuit designers often follow a conservative design approach, pushing the device operating point closer to the center of the design specification space rather than closer to the specification limits defined by communication protocols. However, conservative design approaches counteract the advantages of CMOS scaling since critical performances, such as gain and bandwidth, are deteriorated. On the other hand, when aggressive design is employed, the most common practice for recovering the effects of process variations on device performances and yield is to use post-production calibration techniques [1]–[13]. The underlying principle of post-production calibration, which can be performed either off-line [1], [3], [4], [6], [8] or on-line [2], [5], [7], [9], is based on tuning knobs which counteract the impact of process variations by adjusting performances after a device has been fabricated.

Tuning knobs are an integral part of the calibration process and operate on the design parameters of the IC, e.g., bias voltages and currents. In [1]–[3], [8], [10], [14], tuning knobs are considered as ideal supply sources. Practical implementations of tuning knobs have been proposed in the literature, mainly in the form of tunable MOS capacitors [4], [6], current sources [4], [15], transistors with programmable width [16], adjustable inductors [5], [7], bias actuators, and transmission lines [9]. Reported results verify that tuning knobs can adjust performances of RF ICs, such as power amplifiers and LNAs, and recover yield under excessive process variations. Nevertheless, tuning knobs are also subject to process variations and, thus, their impact on tuning effectiveness has to be considered.

When the knob circuity is an integral part of the tunable design and is used during generation of the training set, the impact of process variations is inherently reflected in the trained regression models. For example, the impact of knob variations on the tuning process was previously considered in [16], wherein the calibrated device is an operational transconductance amplifier and its tunable components are transistors with programmable width. However, as we describe in Section II, there exist scenarios wherein it is not possible to create a training set through a process that includes instances of the tuning knob circuitry, as affected by process variations.

This paper focuses on such scenarios and seeks to (i) elucidate the problem, (ii) investigate the impact of external knob non-idealities, arising due to process variations, on device performances and on the ability of the tuning process to predict the optimum knob position for optimizing the overall device performance, and (iii) present a remedy for counteracting the impact of external knob non-idealities on tuning effectiveness. Results are reported using 36 tunable LNA instances fabricated

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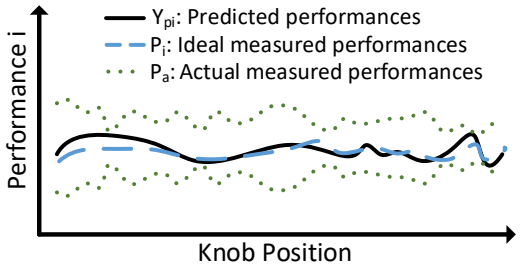

Fig. 1. Knob non-idealities for a single chip.

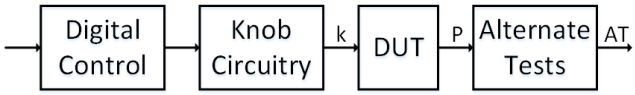

Fig. 2. Limitations of existing tuning architectures.

in IBM's 130nm CMOS process, alongside external tuning knobs implemented as linear drop out regulators [17] and voltage dividers operating on the bias voltages of the LNA.

II. Dealing with Knob Non-Idealities

A. Calibration Process

Post-production tuning consists of two phases. In the pre-production phase, a training data set is generated, consisting of device performances and alternate tests which are measured for several, if not all, knob combinations for each available device. Alternate tests [11] are low cost measurements which are essential in order to eliminate the need for expensive measurements and reduce cost. Using this data set, regression models are trained to correlated performances to alternate tests. In the testing phase, the trained models predict device performances from the measured alternate tests. Accordingly, the optimal knob setting is chosen based on a selection criterion seeking to optimize performance and/or yield.

Calibration methods are divided into iterative test-and-tune [3], [10], [13] and one-shot approaches [1], [2], [8], [12], [14]. The former require low-cost measurements for all possible knob settings, whereas the latter require low-cost measurements for a single knob setting, which is usually the nominal knob position, i.e., the knob values used in the IC design.

B. Problem Definition

When ideal knobs are considered in the tuning process, as is the case in [1]–[3], [8], [10], [14], training and testing is performed with ideal values, i.e., values not affected by knob process variations. For example, in the one-shot method, if k_i are the ideal knob values and AT_i, P_i are the corresponding low-cost alternate tests and performances respectively, then in the pre-production phase a regression function $f(k_i, AT_i, P_i)$ is trained. In the testing phase, the inputs to this regression function are, again, k_i, as well as a single set of low-cost measurements, AT_i. Accordingly, the trained function, f, predicts a performance: $Y_{pi} = f(k_i, AT_i)$. The process is repeated until all performances are predicted. In this case, the regression error, ϵ_{reg}, i.e., the difference between measured and predicted performances, is only due to model imperfections.

In reality, however, the output values of knobs controlling the tunable device characteristics, e.g., bias voltages, will be affected by process variations. Let us assume that the number of ideal knob settings is m and the number of possible variant knob values for each ideal knob setting is N. Accordingly, predicted performances, Y_{pi}, and measured performances, P_i, for the ideal knob settings are vectors of m elements, whereas actual performances, P_a, for the variant knob values are an $m \times N$ matrix. Figure 1 shows Y_{pi}, P_i, and P_a, for a single device over all knob positions. Y_{pi} and P_i can have a single value for each knob position as opposed to P_a which can have any of the N values. The two dotted lines in Figure 1 represent the upper and lower limits of the N possible values for each knob position.

Knob variation in itself does not necessarily pose an issue. Consider, for example, the on-die tuning architecture in Figure 2, which consists of a device under test (DUT) whose performances are calibrated by knobs that are controlled by digital circuitry, as well as circuitry that produces low-cost alternate tests. If the data set used for training the regression models employed in post-manufacturing tuning is obtained from multiple instances of the entire end-to-end tuning architecture, then the impact of knob process variations is inherently taken into account. Indeed, in this case, training and tuning are performed with actual tuning knob values (k_a), alternate test (AT_a) and performance (P_a) values, all of which have been consistently subjected to process variations. Therefore, any error ϵ_{reg} in the tuning method is attributed only to regression imperfections.

However, there exist various scenarios in which multiple instances of the knob circuitry are not available during derivation of the training dataset. For example, consider the case of heterogeneous integrated circuits, 3D ICs, or multi-chip modules, where multiple die are integrated together through interposer or other advanced interconnect and packaging technologies. In such an environment, it is possible that the tuning knob outputs for multiple die will be generated in a centralized fashion through a single die, such as a power management unit (PMU). In this case, during post-production tuning of individual tunable die, the corresponding knob circuity is not available. Therefore, either the ideal outputs of the knob circuitry (i.e., voltage biases) will be directly provided through external sources, or a reference knob circuitry housed on the load-board of the automatic test equipment (ATE) will be used. In either case, an inconsistency between the training and the testing process is introduced, jeopardizing accuracy of the learned regression models. Specifically, training will be performed with the exact same values for each knob position, i.e. with ideal values k_i, AT_i, and P_i, whereas actual values k_a and AT_a will be employed in testing. In this case, knob variations introduce an additional error, ϵ_{knob}, acting on top of ϵ_{reg}, thereby producing an overall error ϵ_{tot}, which is due to both ϵ_{reg} and ϵ_{knob}. Thus, $\epsilon_{tot} > \epsilon_{reg}$. Because of the higher ϵ_{tot}, post-production calibration may not only predict a sub-optimal knob position but may also cause yield loss if the chosen knob setting results in performances falling out of their specifications.

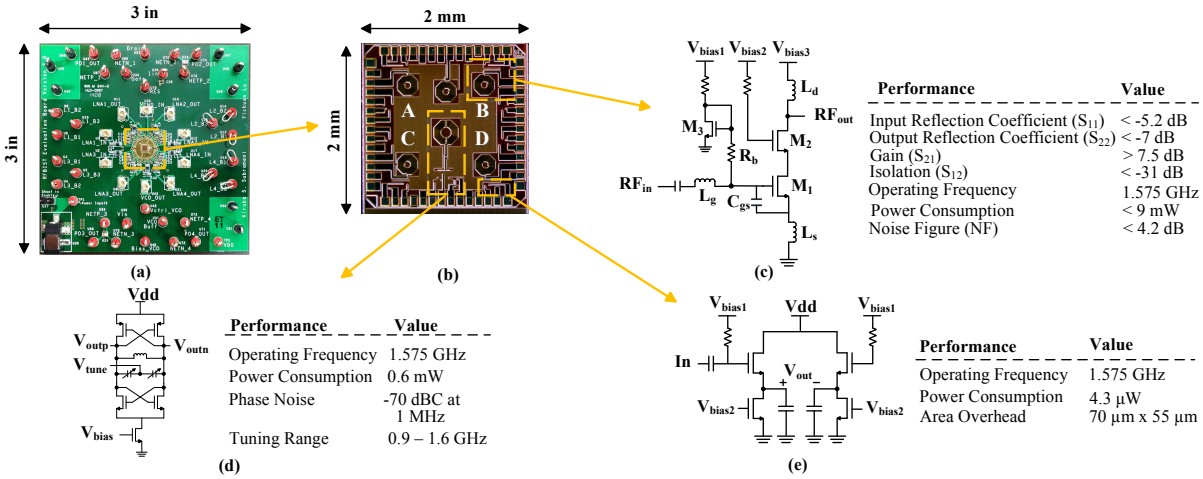

Fig. 3. Tunable Circuit: (a) evaluation board, (b) micro-photograph of fabricated die, (c) LNA schematic, (d) VCO schematic, (e) peak detector schematic.

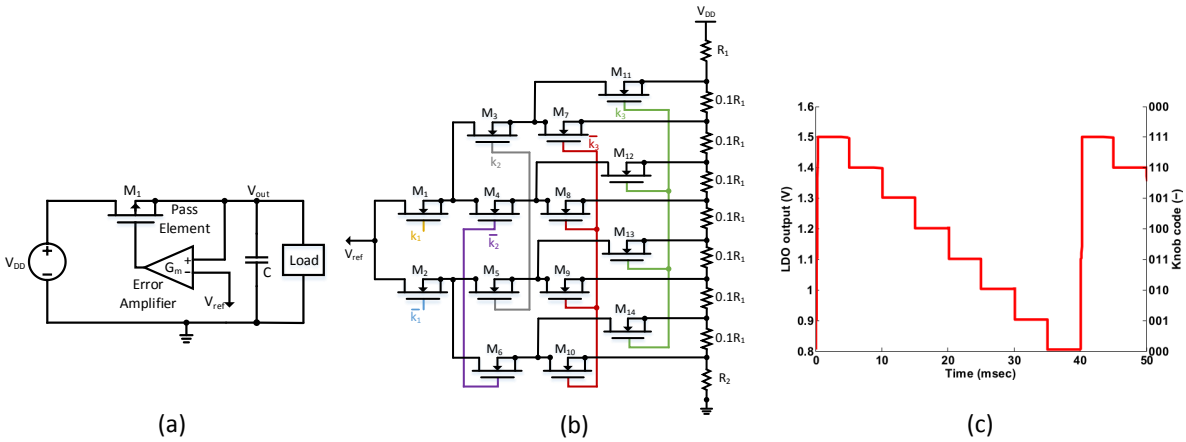

Fig. 4. Tuning Knobs: (a) LDO schematic, (b) reference voltage supply, and (c) simulated LDO output from Cadence.

C. Remedy

To account for such external knob non-idealities and the corresponding higher error, training of the regression functions, f, should be done using performances, alternate tests and knob settings resembling the realistic scenario where all of them are affected by knob process variations. Since such training data is not available, we synthetically enrich the existing data to account for the impact of knob process variations on the performances and alternate tests, by adding noise to the ideal outputs of the tuning knob circuitry. Specifically, assuming that the Spice model of the tuning circuitry is known, Monte Carlo simulation can be used for each ideal knob position in order to generate a set of N variants, each of which results in slightly different knob output values. We can, then, use these variant knob output values during training dataset generation, in order to obtain performances and alternate tests which encompass the impact of knob process variation. In this way, ϵ_{tot} is reduced, becoming comparable to ϵ_{reg}.

Respectively, we point out that: (i) the term noise is used to capture the impact of process variations on the knob circuitry, (ii) this noise is not Additive White Gaussian Noise (AWGN); rather, it reflects the statistics of how process variations impact the knob circuitry and, accordingly, it has statistical structure, which is what we seek to learn, and (iii) training with noise, in this case, results in models which have considered both the impact of process variations on the DUT/alternate tests and the impact of process variations on the knob circuitry

III. Experimental Platform

The experimental platform that was used to demonstrate the impact of external knob non-idealities on the prediction accuracy and the ability of the calibration process to correctly tune the device is an LNA whose tuning knobs have been implemented as an LDO and resistive voltage dividers.

A. Tunable LNA

The fabricated chip is a cascode LNA in IBM's 130nm CMOS process. To facilitate measurements, the chip is mounted on a printed circuit board (PCB). The PCB is shown in Figure 3(a), whereas Figure 3(b) depicts a microphotograph of a die, carrying 4 LNAs. The LNA schematic along with its specifications are shown in Figure 3(c). The circuit comprises two transistors connected in a common source, M_1, and common gate, M_2, configuration. M_3 on the other hand is used for bias purposes. RF transistors have been used in order to achieve high performance; thus, their

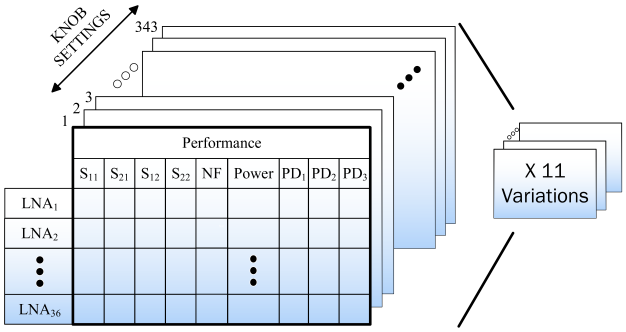

Fig. 5. Experimental dataset.

supply voltage is limited by the technology to 1.2V. The device tunable characteristics are bias voltages V_{bias1}, V_{bias2}, as well as supply voltage, V_{bias3}, and are shown in Figure 3(c). For alternate test purposes, the LNA is excited by a voltage-controlled oscillator (VCO), which has a tuning range of 0.9GHz-1.6GHz and which in our case provides a signal of 1.57GHz, as described in Figure 3(d). The output of the circuit is connected to a peak detector, which translates the high frequency input signal to a DC value. Schematic and performance characteristics of the peak detector are shown in Figure 3(e). More details on the fabricated chip can be found in [2], [12].

B. Knob Implementation

Unlike inductors, MOS capacitors, current sources, etc., which can only control specific LNA performances, voltages have the ability to determine the behavior of all LNA performances, either directly or indirectly. Therefore, in this work, bias voltages have been chosen as the tunable LNA characteristics. In the case of the supply voltage (V_{bias3}), the implemented knob should not only provide a constant voltage, but also a current that properly biases the circuit. To satisfy both requirements, we have implemented the knob controlling the supply voltage as an LDO, whose simplified schematic is shown in Figure 4(a). The LDO consists of a transistor acting as a pass element and an error amplifier, which senses the output voltage, compares it with a reference voltage, V_{ref}, and accordingly drives the pass element until the output voltage, V_{out}, becomes equal to V_{ref} [17]. The reference voltage is provided by the circuit of Figure 4(b). The gates of switches $M_1 - M_{14}$ are controlled by a digital knob code, providing one of the desirable output voltages. These voltages are created through a resistive voltage divider network. Since LNA transistors M_1 and M_2 in Figure 3(c) do not demand current supply, the resistive voltage divider can be used for implementing knobs that provide V_{bias1} and V_{bias2}. The LDO circuit was designed in the same 130nm technology using transistors which are biased at 2.5V. Cadence simulations, which are depicted in Figure 4(c), show the output of the LDO, ranging from 0.8V-1.5V versus time for all possible knob codes.

C. Experimental Flow and Dataset

The minimum and maximum values that the knobs can provide are defined by the maximum V_{DD} of the technology. Thus, considering that for the LNA $(V_{DD})_{max} = 1.2V$, knob values were set from 0.8V-1.4V with a step of 0.1V. This results in 7 positions per knob and $7^3 = 343$ settings per LNA.

To emulate the effect of knob non-idealities, each LNA is supplied with the ideal knob setting values as well as process-varied knob values. These non-ideal knob values are generated through Monte Carlo simulations of the LDO and the two voltage dividers. Specifically, we generate 11 Monte Carlo values per knob combination. For these values, we measure 6 performances: input reflection coefficient (S_{11}), reverse isolation (S_{12}), power gain (S_{21}), output reflection coefficient (S_{22}), noise figure (NF) and power consumption (P_{cons}). We also measure 3 peak detector values (PD_{1-3}), which are generated through 3 different VCO frequencies. Measurements are repeated for all available 36 LNAs. This results in a dataset of $11 \times 343 \times 36 \times 9 = 1,222,452$ entries, which is illustrated in Figure 5.

We randomly split the available LNAs into a dataset of 26 devices for training and 10 devices for testing. In the training phase, regression functions $f_1 - f_6$ are built for the 6 individual performances $(S_{11}, S_{12}, S_{21}, S_{22}, NF, P_{cons})$ using peak detector values corresponding to the median knob position, i.e., $(k_1, k_2, k_3) = (1.2, 1.2, 1.2)V$, of the ideal circuit for every knob setting. For the remaining 10 LNAs of the testing set, peak detector values for each of the 11 knob-variants at the median knob position, along with all possible knob settings are used as inputs to $f_1 - f_6$ in order to obtain predicted performances for all 343 knob settings.

IV. Experimental Results

In an LNA the crucial parameters that reflect its performance are voltage/power gain (S_{21}) - equal in this work since the device is matched at 50Ω at its input and output - NF, and P_{cons}. Due to the increased demand for low-power, yet high performance ICs, an explicit way to characterize the overall performance of an LNA is provided by the following Figure of Merit (FoM) [18]:

$$FoM = \frac{S_{21}}{P_{cons} \cdot (NF - 1)} \quad (1)$$

Using this dataset, in the following sections we investigate: (i) the impact of knob-variations on the ability of the calibration method to accurately predict the knob position that maximizes the FoM, and (ii) the modified model that is needed in order to account for knob-variations and consequently select the optimum knob setting.

A. Impact of Knob Non-Idealities

The distribution of knob output voltages is shown in Figure 6. The neutral position corresponds to the bold line of the box plot and ranges from 0.8V-1.4V. The most extreme cases of knob-variations result in knob values shifted by approximately

TABLE I
OPTIMAL-KNOB SELECTION ABILITY

LNA	Ranking			Percentile Difference		
	Non-variant	Variant	Training w. noise	Non-variant(%)	Variant(%)	Training w. noise(%)
1	4	16	10	2.7	11.4	8.7
2	3	20	9	1.3	37.3	8.3
3	7	23	3	5.1	15.1	0.6
4	3	90	4	0.05	29.6	3.4
5	7	45	16	3.8	20.2	8.9
6	5	19	9	2.5	10.2	4.2
7	1	38	30	0	17.3	13.9
8	2	20	1	0.2	6.7	0
9	6	22	3	2.4	33.4	2.3
10	7	81	1	1.8	24.9	0
Average	4.5	37.4	8.5	1.8	22.5	5

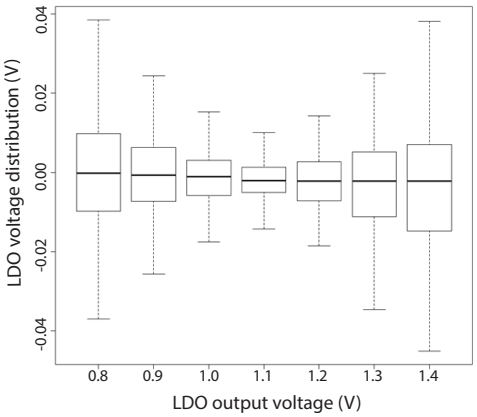

Fig. 6. Simulated LDO variations for all possible voltage outputs.

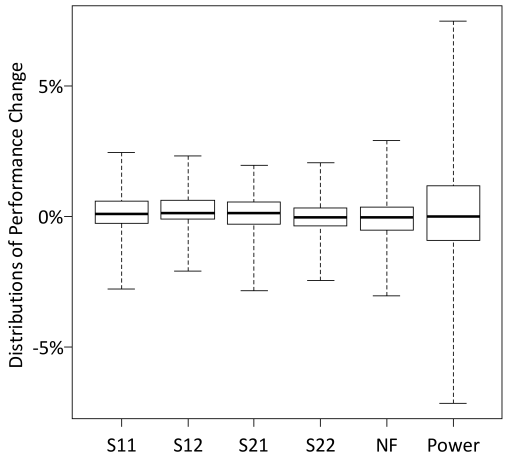

Fig. 7. Measured performance variations for all LNAs.

0.04V from the ideal position. We note that the distribution of knob output voltages is highly dependent on the specific voltage level because of the LDO linearity. Due to these knob variations, excessive performance variations are also produced.

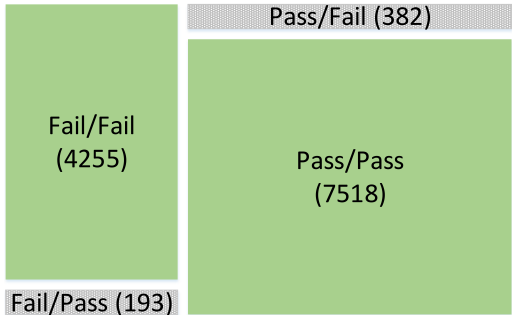

Fig. 8. Truth table for ideal and varied knob settings.

This is highlighted in Figure 7, wherein actual measured performances, i.e., performances affected by knob process variations, $S_{11}, S_{12}, S_{21}, S_{22}$, NF, and P_{cons} for all 3430 knob-variant positions are compared against ideal measured performances, i.e., performances corresponding to the 343 ideal, non-variant knob positions (bold line). For the purpose of comparison, for each of the 343 ideal knob positions, we use the absolute distance between the LNA performances for this knob position and those obtained for each of the 10 knob-variant positions. Reported values in Figure 7 are normalized over their range. Knob non-idealities also have an impact on yield. This is shown in Figure 8, where measured performances are projected as passing or failing devices based on the LNA specifications (Figure 3(c)). When knob-variations are considered, a significant number of test escapes and yield loss, in the order of 4.6% occurs. Specifically, for the entire population, 382 ideal knob-settings are marked as passing whereas their variant counterparts are marked as failing. The opposite case is observed for 193 knob settings.

The impact of knob non-idealities on effectiveness of optimal knob prediction is also investigated. This is illustrated in Table I, in which for the 10 LNAs of the testing set, selection ability is shown in terms of ranking and percentile difference between the predicted position and the measured position corresponding to the maximum FoM. These values

are calculated as follows: after the model predicts FoM values for all possible combinations, we pick the one corresponding to the maximum FoM. Then, we refer to the corresponding position in the measured dataset and compare its performance with the measured best FoM. For the *non-variant case*, i.e., when the peak detector values of the ideal knobs are provided as inputs to the regression model, the model predicts on average a knob setting with a ranking of 4.5, which is 1.8% different from the measured best FoM. The error in this case is only due to regression error. In the practical case, where knobs are subject to process variations but for reasons such as the those discussed in Section II.B. the tuning circuitry is not available during training, knob variation error acts on top of regression error, resulting in a higher total error. This is shown in Table I as the *variant* case for which the predicted knob position has a ranking of 37.4 with a corresponding difference of 22.5% as compared to the measured best FoM. We note that the reported variant values for each LNA refer to the worst of the 10 variant cases. Yet, they represent knob values which can occur in a practical knob implementation. When the proposed remedy is applied, i.e., when knob values obtained via Monte Carlo simulations are used for training the regression model, the model becomes more accurate in terms of knob selection, as depicted in Table I. When *training with noise*, the average ranking among the 10 LNAs of the testing set is improved from 37.4 to 8.5 and the percentile error is reduced from 22.5% to 5%. The inability of the proposed remedy to always identify the optimum solution comes from both error sources, i.e., ϵ_{reg} and ϵ_{knob}. While it is difficult to decouple and distinguish regression error from knob variation error, the overall error of the new model is significantly decreased, as compared to the *variant case*, thus resulting in an important improvement in terms of knob selection effectiveness.

V. Conclusion

This work highlighted a limitation of learning-based post-production calibration in analog/RF ICs, which occurs when the tuning circuitry and the IC are not integrated on the same die. For this purpose, we designed an LDO and two voltage dividers as tuning knobs for an LNA fabricated in IBM's 130nm CMOS process, and we showed that when the knob circuitry is not available during training, knob non-idealities greatly affect the ability of the trained regression functions to accurately predict and select the knob setting that optimizes the overall performance of the LNA. Subsequently, we proposed a remedy which is based on training the regression functions with Monte-Carlo generated "noise" in the knob output values, and we demonstrated that a significant improvement can be achieved in terms of calibration effectiveness.

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References

[1] M. Andraud, H. G. Stratigopoulos, and E. Simeu, "One-shot non-intrusive calibration against process variations for analog/RF circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 2022–2035, 2016.

[2] G. Volanis, D. Maliuk, Y. Lu, K. S. Subramani, A. Antonopoulos, and Y. Makris, "On-die learning-based self-calibration of analog/RF ICs," in *IEEE VLSI Test Symposium (VTS)*, 2016, pp. 1–6.

[3] T. Zhu, M. B. Steer, and P. D. Franzon, "Surrogate model-based self-calibrated design for process and temperature compensation in analog/RF circuits," *IEEE Design Test of Computers*, vol. 29, no. 6, pp. 74–83, 2012.

[4] D. Chang, J. Kitchen, and S. Ozev, "Post-production adaptation of RF circuits for application-specific performance metrics," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 2775–2778.

[5] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A CMOS low-noise amplifier with reconfigurable input matching network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1054–1062, 2009.

[6] K. Jayaraman, Q. Khan, B. Chi, W. Beattie, Z. Wang, and P. Chiang, "A self-healing 2.4GHz LNA with on-chip S11/S21 measurement/calibration for in-situ PVT compensation," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2010, pp. 311–314.

[7] T. Das, A. Gopalan, C. Washburn, and P. R. Mukund, "Self-calibration of input-match in RF front-end circuitry," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 12, pp. 821–825, 2005.

[8] V. Natarajan, S. Sen, A. Banerjee, A. Chatterjee, G. Srinivasan, and F. Taenzler, "Analog signature-driven postmanufacture multidimensional tuning of RF systems," *IEEE Design Test of Computers*, vol. 27, no. 6, pp. 6–17, 2010.

[9] S. M. Bowers, K. Sengupta, K. Dasgupta, B. D. Parker, and A. Hajimiri, "Integrated self-healing for mm-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1301–1315, 2013.

[10] V. Natarajan, A. Banerjee, S. Sen, S. Devarakond, and A. Chatterjee, "Yield recovery of RF transceiver systems using iterative tuning-driven power-conscious performance optimization," *IEEE Design Test*, vol. 32, no. 1, pp. 61–69, 2015.

[11] S. Larguech, F. Azas, S. Bernard, M. Comte, V. Kerzerho, and M. Renovell, "Efficiency evaluation of analog/RF alternate test: Comparative study of indirect measurement selection strategies," *Microelectronics Journal*, vol. 46, no. 11, pp. 1091 – 1102, 2015.

[12] Y. Lu, K. S. Subramani, H. Huang, N. Kupp, K. Huang, and Y. Makris, "A comparative study of one-shot statistical calibration methods for analog/RF ICs," in *IEEE International Test Conference (ITC)*, 2015, pp. 1–10.

[13] S. Sun, F. Wang, S. Yaldiz, X. Li, L. Pileggi, A. Natarajan, M. Ferriss, J. O. Plouchart, B. Sadhu, B. Parker, A. Valdes-Garcia, M. A. T. Sanduleanu, J. Tierno, and D. Friedman, "Indirect performance sensing for on-chip self-healing of analog and RF circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2243–2252, 2014.

[14] D. Han, B. S. Kim, and A. Chatterjee, "DSP-Driven self-tuning of RF circuits for process-induced performance variability," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 18, no. 2, pp. 305–314, 2010.

[15] D. Han, S. S. Akbay, S. Bhattacharya, A. Chatterjee, and W. R. Eisenstadt, "On-chip self-calibration of RF circuits using specification-driven built-in self test (S-BIST)," in *IEEE International On-Line Testing Symposium (IOLTS)*, 2005, pp. 106–111.

[16] S. Banerjee, M. P. Gupta, A. Banerjee, S. Kumar, and A. Chatterjee, "Digitally-compatible ring oscillator frequency driven tuning of CN-TFT amplifiers: Performance compensation under statistical and morphological variations," in *IEEE International Mixed-Signals Testing Workshop (IMSTW)*, 2015, pp. 1–6.

[17] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, 2005.

[18] A. Antonopoulos, M. Bucher, K. Papathanasiou, N. Makris, R. K. Sharma, P. Sakalas, and M. Schroter, "CMOS RF noise, scaling, and compact modeling for RFIC design," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 53–56.