

Reducing Hierarchical Test Path Cost via Modular Test Requirement Analysis

Yiorgos Makris
EE Department - Yale University
New Haven, CT 06520
yiorgos.makris@yale.edu

Alex Orailoglu
CSE Department - U.C. San Diego
La Jolla, CA 92093
alex@cs.ucsd.edu

Abstract

We propose a methodology that examines design modules and identifies appropriate vector justification and response propagation requirements for hierarchical test. Based on a cell-level analysis and transparency composition methodology, test requirements for a module are defined as a set of fine-grained input and output bit clusters and pertinent justification and propagation values. The identified test requirements are independent of the actual test set and are adjusted to the cell-level connectivity and inherent regularity of the module. As a result, they combine the generality required for fast hierarchical test path construction with the accuracy necessary for minimizing the incurred DFT hardware overhead, thus fostering cost-effective hierarchical test. Experimental results verify the ability of the proposed methodology to moderate the cost of hierarchical test path construction through accurate, compact, and highly parametrizable test requirement definition.

1. Summary

Hierarchical methods leverage on the ability to individually target each module in a design and generate highly efficient local test. This benefit, however, comes at the cost of necessitating hierarchical test paths through the upstream and downstream logic, which establish transparent access to the module under test (MUT), as depicted in Figure 1(a). During hierarchical test path construction, however, the module under test is treated as a black box and no information pertaining to its inherent test requirements is utilized. Consequently, excessive DFT hardware is employed in order to construct hierarchical test paths. In an effort to reduce the DFT cost of hierarchical test path construction, two directions have been examined. Along the first direction, several research efforts have been invested in efficiently defining, extracting, and utilizing inherent design transparency. Along the second direction, inherent functionality of the upstream and downstream logic is utilized to constrain local test generation in an effort to render highly translatable test. Not much attention has been paid, however, to a third alternative, namely the possibility of moderating the cost of hierarchical test paths through an examination and informed definition of test requirements for each module. This idea is depicted in Figure 1(b), where the internal cell-level connectivity of the MUT is examined and its test requirements are defined in terms of several input and output bit clusters. This, in turn, necessitates several narrow hierarchical test paths instead of a single coarse path, thus increasing the probability of their inherent existence in the design and reducing the expected DFT cost for their construction. In this work, we examine the impact of test requirement granularity on the severity of hierarchical test path construction and we propose a methodology for reducing the cost of hierarchical test path construction by adjusting the generality of test requirements. A cell-level analysis and a symbolic path composition result in the definition of fine-grained test requirements on sets of input and output bit clusters.

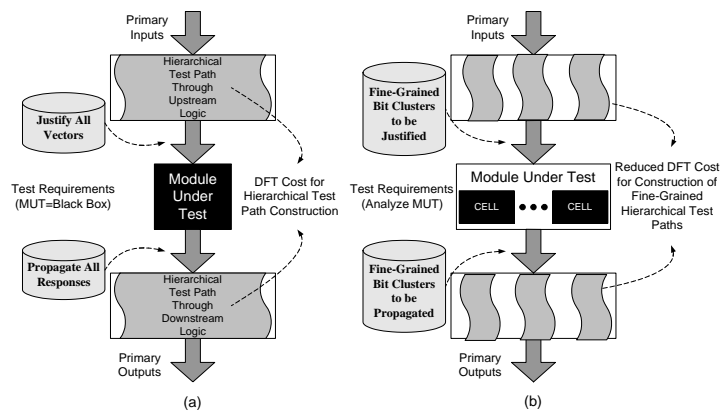


Figure 1. Granularity of Test Requirements

