ISTFA™ 2018: Conference Proceedings from the 44th
International Symposium for Testing and Failure Analysis
October 28–November 1, 2018, Phoenix, Arizona, USA

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Pattern Matching Rule Ranking Through Design of Experiments and Silicon Validation

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Abstract

Continued technology scaling has led to exposure of many 'weak-points' in the designs fabricated in some of the most advanced technology nodes. Weak-points are certain layout patterns which are found to be sensitive to process non-idealities and have a higher tendency to cause defects. They may be coded in the form of Pattern Matching (PM) rules and included within the Design for Manufacturability Guidelines (DFMGs) to ensure product manufacturability. Often, during Integrated Circuit (IC) design, a trade-off is made between meeting performance specifications and complying with DFMGs. As a result, designs may reach the foundry with some DFMG violations. Fixing such violations generally causes a 'ripple effect' where one change requires many changes in other metal layers, making the process tedious. Therefore, providing a ranked list of guidelines to the designers helps them in assessing the criticality of violations, prioritizing, and fixing them accordingly. Past research suggests using diagnosis data to determine the impact of DFMG violations. However, this is a reactive approach wherein DFMGs are ranked only based on their hard-defect causing nature. To make the ranking process more robust, we propose a proactive silicon validation based approach which not only considers the yield loss due to hard-defects but also takes into account the parametric and reliability degradation caused by DFMG violations. We evaluate the effectiveness of the proposed methodology through on-silicon experiments on an advanced Fully-Depleted Silicon-On-Insulator (FD-SOI) technology node.

I. Introduction

With continued scaling and the introduction of new technology nodes, the complexity of the IC fabrication process is ever-increasing. New nodes expose new manufacturability issues and design 'weak-points' (popularly known as 'hotspots') are one of such problems. Weak-points are certain areas of a design, which despite being Ground Rule (GR) clean, show abnormal variation and tend to cause defects. Root cause analysis for every weak-point is expensive, time-consuming, and often intractable. Mostly, complex design process interactions of the polygons surrounding the defect area (neighborhood) is believed to be the root cause. While some of the weak-points are found to be common across technology nodes (with scaled dimensions), the technology specific ones are usually discovered during technology development.

Weak-points causing consistent yield loss or reduced process margins can be deemed as 'risky' or 'hard-to-manufacture' patterns. In order to make such patterns 'safe' and ensure manufacturability, a guideline is specified for each of them and added to DFMGs [1]. Pattern-specific guidelines are often referred to as PM rules. Designs are screened for PM rule violations and flagged areas may require fixing.

While the primary objective of the designers is to meet the stringent Power, Performance and Area (PPA) specifications, adhering to PM rules may take a lower priority. Often, they either request waivers for PM rule violations, seek detailed and quantified analysis demonstrating the impact of such violations, or request for the list of rules to be ranked based on their criticality. Combining the ranking information with other design details such as critical paths, device drive strengths etc., designers can analyze the criticality of violations and fix them accordingly.

In the past, statistical occurrence-based pattern scoring was proposed in [2]. Scoring methods based on pattern-complexity [3] and pattern-regularity [4] were proposed but they suffer from high false positives and false negatives, respectively. None of these works considered actual electrical effects or silicon data for pattern criticality assessment. However, many researchers have used yield data to rank DFMGs in general [5][6][7][8][9]. The basic idea in all such works was to perform diagnosis on failing ICs, check whether any DFMGs were violated at the diagnosed defect locations and rank them based on the frequency of such violations. Such methods perform reasonably well but have many drawbacks: (a) Accuracy of ranking depends on the accuracy of diagnosis. (b) They take a reactive approach, where rule rankings are available only after fabricating and learning from a few products, leaving early customers deprived of such information. (c) They perform ranking mainly based on locations showing hard-defects, while some DFMG violations may not cause significant yield loss due to hard-defects; instead, as shown in later sections of this paper, their presence may lead to significant performance degradation or reliability issues. Ignoring such effects of DFMG violations may lead to inaccurate rankings.

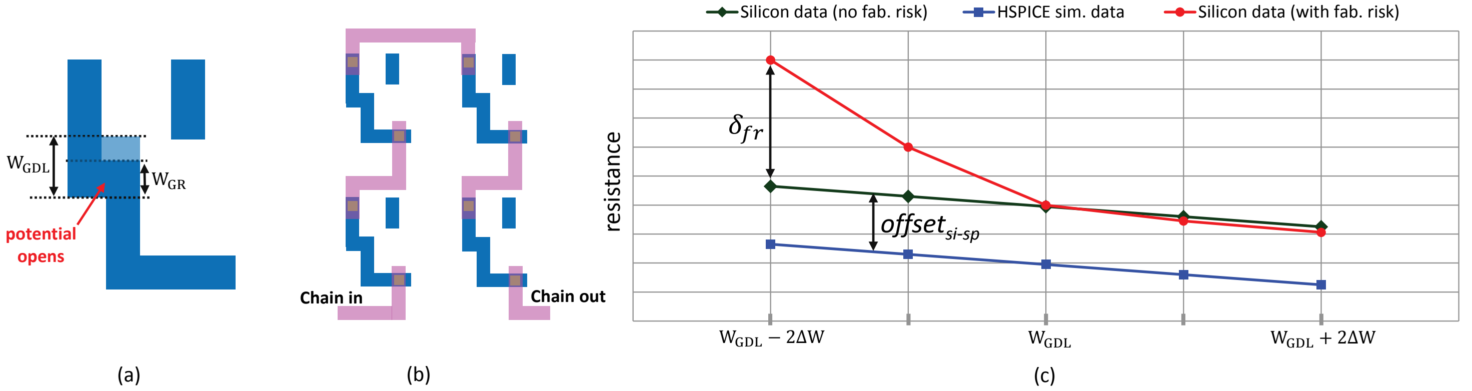


Figure 1: (a) An example pattern / PM rule (b) Chain based test structure (c) Example data

In this work, we propose a methodology to improve the ranking process through silicon validation. We not only take into account the hard-defects but also consider the parametric degradation and reliability effects of rule violations. Traditionally, testing for reliability effects such as Time Dependent Dielectric Breakdown (TDDB) has been expensive, time-consuming and destructive in nature. As part of this study, we also present alternative low-cost, non-destructive, in-line tests which can be used as a proxy to understand the reliability effects.

The rest of this paper is structured as follows: The proposed methodology is explained in section II. Its challenges and key differences from Ground Rule Validation (GRV) are discussed in section III. Experimental results are presented in section IV and conclusions are drawn in section V.

II. Proposed methodology

The criticality of a pattern or a PM rule mainly depends on its likelihood of causing hard-defects, parametric degradation, and/or reliability issues (latent defects). Since, the hard-defect causing nature of patterns has already been extensively studied [5][6][7][8][9], the focus of this work is on establishing methodologies to understand the parametric degradation and reliability issues caused by them.

A. Parametric Degradation

The two main parameters of interest in circuit design are Resistance (R) and Capacitance (C) because they directly impact the performance (timing) of a design. A PM rule violation may affect the performance by varying either R, C, or both. It may be difficult for a foundry to estimate the change in the parametrics of the complete IC due to the localized degradation caused by a pattern, because it depends on whether the risky pattern is present on a critical path, slack available on that path, number of instances of the pattern along the path, etc. Designers, who have access to such design-related information, can estimate the impact of pattern-related localized degradation on the overall design and decide if fixing is necessary. The proposed methodology to identify the type and degree of degradation caused by risky patterns is explained using the following example.

The pattern shown in Figure 1a can be considered as risky, because it tends to cause a metal pinch-off (potential opens) in the indicated area and increases the resistance of the path. This occurs when the width (W) is $W_{GR} \leq W < W_{GDL}$, where W_{GR} is the minimum ground rule value and W_{GDL} is the suggested minimum value to ensure reliable fabrication (guideline value). To capture the change in resistance, the pattern is transformed into a chain-based test structure, as shown in Figure 1b, and W is varied in fine intervals of ΔW. The details of test structure design are out of the scope of this work and the reader is referred to [10]. For the sake of brevity, a Design of Experiment (DOE) with only five steps is considered for this discussion and its results are shown in Figure 1c. HSpice simulation data for such an experiment can be expected as shown by the blue line.

If this pattern is not risky, we can expect its silicon data (indicated by the green line) to be consistent with Spice data but with a constant offset. Such a silicon-to-Spice offset ($offset_{si-sp}$) exists in any process. If Spice models are well calibrated to the process, we can expect the offset to be minimum, but always finite. It can be either positive or negative depending on the process conditions.

On the other hand, if this pattern is indeed risky, we expect its silicon data to show a trend as indicated by the red line, which is consistent with the Spice data at widths W_{GDL} and higher but deviates from the model at smaller widths ($< W_{GDL}$). Such a deviation suggests the occurence of complex design process interactions during fabrication, causing higher degradation in patterns with widths below the guideline value. This confirms that the pattern is truly risky at smaller widths and violating this PM rule would result in increased resistance and parametric degradation. The deviation is captured as fabrication risk (δ_{fr}) and used as a metric to express the severity of the rule violation. Thus, the total deviation of silicon data from spice is given by:

$$\delta_{tot} = \delta_{fr} + offset_{si-sp}$$

The precise value of δ_{fr} is not of high interest to us, instead, a mere indication that the pattern is sensitive to the process at certain rule values, and an approximate estimate of its sensitivity is sufficient for this analysis.

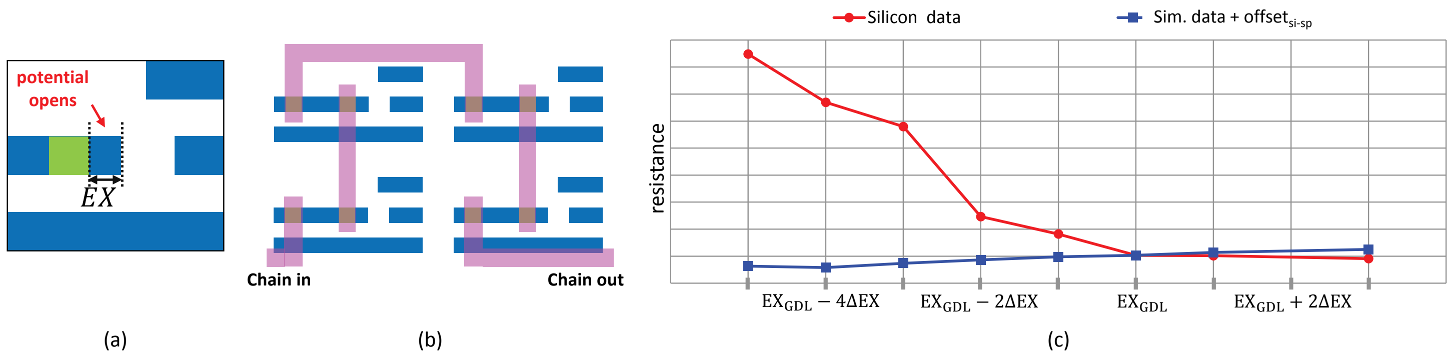


Figure 2: (a) The pattern (b) Chain based test structure (c) Experimental results from case study I

One might perceive this as a silicon to Spice modelling issue and propose to collect more silicon data, update the Spice models, and entirely remove the PM rule from the Design Manual (DM). However, this is not practicable because we cannot model a moving target. PM rule violations may show degradation only on a certain set of dice, on certain wafers which are affected by the process in a certain manner. Though systematic, such degradation is highly process dependent. Under some process conditions, some dice may show more aggressive degradation; in the worst-case scenario, they may even show hard-defects, or in the best-case scenario, they may not show any degradation at all. Hence, modelling such effects of PM rules is not a reliable option. They must be treated differently, and their violations must be fixed.

Similar analysis can be performed to observe capacitance degradation when the fail-mode is bridging (shorts).

B. Reliability Effects

Some of the PM rule violations may not show any electrical degradation at time zero, especially when the fail-mode is bridging. Due to the high quality Inter Metal Dielectric (IMD) used in newer technology nodes, even though two metal lines are printed very close to each other and have a very thin layer of dielectric separating them, the electrical shorts test may not show any change in leakage currents; hence, passing all electrical tests before the chip leaves the foundry. However, such thin IMD may break down sooner than expected and result in field returns. In some cases, such devices may be detected during post burn-in tests, but that still causes significant yield loss. In order to ensure high quality and prevent losses to the foundry, it is imperative to capture the reliability effects of PM rule violations and consider them during the ranking process.

Traditionally, reliability tests are expensive, time-consuming, and often destructive in nature. In this work, the objective is not to characterize the IMD or ascertain its exact lifetime; rather our intention is just to determine whether the PM rule violation affects reliability. Thus, we propose to use low cost in-line capacitance measurements as proxy to detect the impact on reliability. Adjacent metal lines act as parallel plates of a capacitor and their capacitance is inversely proportional to the space between them. If the metal lines are printed much closer to each other than expected, the reduction in space and the IMD is reflected as an increase in capacitance. Therefore, monitoring capacitance variation can provide insight into reliability effects of risky patterns.

III. Challenges And Key Differences From GRV

C1: Large Areas

Though the types of defects caused by PM rule violations are systematic, they may not occur on every instance of a violation and on every wafer. They are observed when a set of process variations (topography, litho focus/dose, etch rate etc.) occur together at certain magnitudes. Hence, we need Devices Under Test (DUTs) of significantly large areas in order to increase the probability of capturing such process variations.

C2: Defect Density (D_0) Test Structure Like Behavior

D_0 test structures are created with large areas to capture random defectivity, intra-die process variations etc. Since, PM rule test structures also need large areas, they may behave like D_0 test structures showing yield loss due to random defectivity which could be mistaken for systematic, pattern-related yield loss. Therefore, wherever applicable, the D_0 component in the data must be isolated by comparing the data from PM test structures to the corresponding D_0 data.

D1: Absolute values may not provide useful information

In traditional GRV, the main objective is to determine the value at which a Ground Rule (GR) breaks or becomes 'safe' for fabrication. DOEs are pushed to extremes to observe such behavior and this often leads to 'cliffs' in data. Therefore, the raw silicon data is, by itself, sufficient to obtain the necessary information in most cases. Whereas, in case of PM rule validation, patterns are inherently GR clean and most of the time, we may not see any cliffs in the data. Even a trend in the data could be due to changes in design itself. Hence, only the deviation of silicon data from Spice models provides usable information, based on which the process risk associated with the pattern can be determined.

D2: Process Window Qualification (PWQ)

PWQ is a process where the litho focus and dose values are varied to determine the process window. Since PM test structures represent a set of known weak-points of a technology node, they tend to have smaller process margins compared to regular GRV test structures. Hence, they make an

excellent choice for process window qualification or process window monitoring.

IV. Experimental Results

In this work, we have proposed a methodology to capture the parametric degradation and reliability issues caused by PM rule violations and use such information in the PM rule ranking process. The effectiveness of this method is demonstrated through the following case studies. All experiments are performed on a subset of PM rules specified for an advanced FD-SOI technology node[1].

A. Case study I

Consider the pattern shown in Figure 2a. This pattern tends to cause a Line End (LE) pull back as the metal extension past via (EX) is reduced below the guideline value. To detect the change in resistance or potential opens caused by this PM rule violation, the pattern is transformed into a chain-based test structure as shown in Figure 2b, and EX is the DOE parameter varied between the DUTs in the test structure. The resistance values obtained from this experiment are shown in Figure 2c. Simulation results with the $offset_{si-sp}$ component added to it are plotted as the blue line. The $offset_{si-sp}$ value is computed by taking the difference between the silicon and simulation data at the guideline value. The median values of the silicon data obtained from three Process Of Record (POR) wafers is plotted as the red line. From the plot, we can see that as we reduce EX below the specified guideline value, the silicon data shows a drastic deviation from the model, leading to an increase in resistance. As explained in section IIa, this deviation indicates the occurrence of some unexpected design process interactions, and hints at the fabrication risk associated with this PM rule violation.

B. Case study II

Consider the pattern shown in Figure 3a. In this pattern, the metal lines in the center tend to show bridging defects when the space (S) between them is reduced below a specified guideline value. The pattern is transformed into a comb-comb test structure as shown in Figure 3b. The Scanning Electron Microscopy (SEM) image of the bridging defect caused by this pattern is shown in Figure 4. The plot in Figure 5 shows the results from the electrical shorts test. These results show no indication of shorts or any risk associated with this pattern when S is reduced below the specified guideline value. Therefore, this data may lead to a low ranking of this PM rule. However, as explained in section IIb, violating this PM rule could cause latent defects. Hence, we performed a capacitance test on this test structure and the results are shown in Figure 6a. Simulated capacitance value, with $offset_{si-sp}$ component added to it, is plotted as the blue line. When S is varied as the DOE parameter, we expect to see a change in capacitance by design, and this trend is captured in the simulation data. The median of the silicon data obtained from three POR wafers is plotted as the red line. The plot shows that, as S is reduced below the guideline value, the capacitance increases, revealing a deviation from the simulation data. This deviation from the model shows that unexpected design process interactions have caused the two metal lines to be printed much closer than expected when $S < S_{GDL}$.

During technology development, the guideline value may require fine tuning based on changes to the process flow, design rules etc. The proposed methodology can also assist in deciding the correct guideline value. In this example, it appears that, with the currently specified guideline value, there is no process margin and, hence, this rule warrants a guideline change. Based on the available data, to ensure sufficient process margin, the guideline value can be updated from S_{GDL} to $S_{GDL} + 2\Delta S$.

We have used capacitance measurements as a proxy to indicate the degradation in reliability. To confirm our hypothesis that the observed change in capacitance was indeed due to the change in the amount of dielectric and not due to any other process parameters, we performed a 'V_{ramp} test' on one of the three POR wafers. V_{ramp} test is a quicker alternative to the TDDB test but still destructive in nature. In the V_{ramp} test, the voltage difference between the two metal lines is constantly increased until the dielectric between them breaks down. The breakdown voltage (V_{BD}) serves as an indicator of the quality, thickness, and other physical properties of the dielectric. V_{BD} per unit length (nm) of dielectric is a fixed value for a process. Therefore, the breakdown voltage of the DUT increases linearly with the increase in space between the metal lines. Thus, the expected breakdown voltage of the DUT

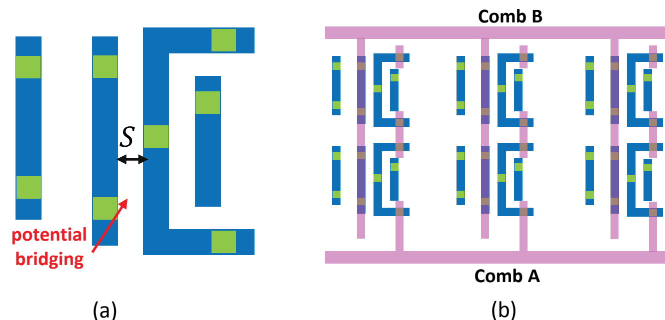


Figure 3: (a) The Pattern and (b) Comb-Comb test structure from case study II

Figure 4: Top down SEM image of the pattern related bridging defect discussed in case study II

[1] The exact dimensions of patterns, yield loss, and performance degradation numbers are proprietary information. Therefore, only the trend in the data is presented.

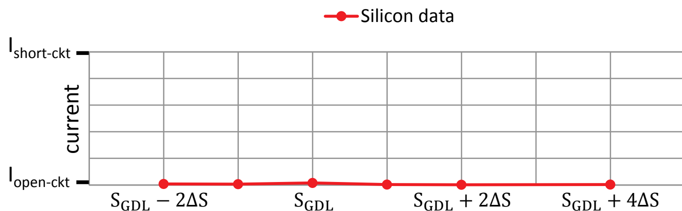
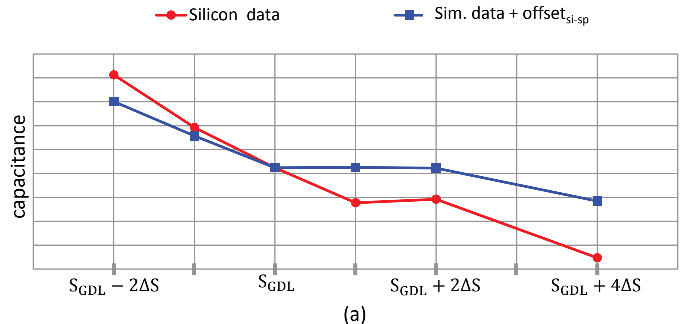


Figure 5: Measurements from the comb-comb shorts test of the pattern discussed in case study II



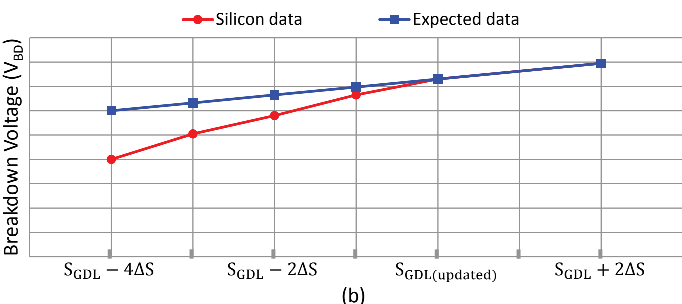


Figure 6: (a) Capacitance measurements and (b) Vramp test results of the pattern discussed in case study II

can be computed, and it appears to be a straight line with the slope V_{BD}/nm.

The Silicon data from this test is shown in the Figure 6b. The median values are plotted as the red line and the expected values are shown using the blue line. In this study, V_{BD}/nm is computed by taking the slope of the silicon data between the 'safer' DUTs (with $S > S_{GDL}$). The silicon data shows a non-linear curve, where DUTs with space $S < S_{GDL}$ show lower breakdown voltages than expected. Since, all DUTs received the same IMD, we can infer that the reduction in the breakdown voltage and the deviation from expected values is mainly due to the reduction in the quantity of dielectric, which is, in turn, caused by two metal lines printing much closer to each other than expected. Since, capacitance measurements also showed the same trend, they can be used as a low-cost alternative to capture the reliability effects of PM rule violations.

The main objective of this work is to demonstrate a methodology to generate the necessary information to rank PM rules in various advanced technology nodes, rather than publishing the rankings for a specific node[2]. Generally, PM rules within a node can be ranked relatively to each other by considering all the relevant information such as yield loss, parametric degradation, reliability effects, etc. It is difficult to define a unique mathematical expression which accepts this information and outputs a rank for every rule because the way this information is used and the threshold at which a pattern is flagged as risky, varies from foundry to foundry and across technology nodes.

V. Conclusions

We have discussed the importance of ranking PM rules in advanced technology nodes. We have shown that PM rule violations not only cause yield loss but may also cause performance degradation and reliability issues. We have demonstrated methodologies to capture such crucial information and include it in the PM rule ranking process. We have also shown that low cost capacitance measurements can be used in place of expensive and destructive reliability tests to learn about reliability effects of PM rule violations. In future, we need to investigate whether various other factors such as density, topological variation etc., also affect the criticality of a pattern and include them in the ranking process.

Acknowledgement

This research has been partially supported by the Semiconductor Research Corporation (SRC) through task 2709.001.

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