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An Analog Checker with Input-Relative Tolerance for Duplicate Signals

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Abstract. We discuss the design of a novel analog checker that monitors two duplicate signals and provides a digital error indication when their absolute difference is unacceptably large. The key feature of the proposed checker is that it establishes a test criterion that is dynamically adapted to the magnitude of its input signals, thus enhancing the accuracy of assessing their relative discrepancy. Consequently, when this checker is utilized in concurrent error detection, it diminishes the probability of both false negatives and false positives. Likewise, when employed for off-line test purposes, the checker supports both high yield and high fault coverage. In contrast, checkers implementing a static test criterion may only be tuned to achieve efficiently one of the aforementioned objectives.

Keywords: concurrent test, on-line test, analog test, analog checkers

1. Introduction

The numerous analog interfaces incorporated in modern systems have stimulated an increasing level of interest in analog test. The problem is particularly difficult mainly due to the continuous nature of analog signals and the necessity for accurate measurement of their values. Limitations of traditional functional test methods led to the development of Design for Test (*DFT*) techniques that aim to reduce the complexity of stimuli application and response evaluation and, by extension, to lessen the dependency on automatic test equipment. Current *DFT* techniques fall into one of the following categories: *reconfiguration for test* and *code-based test* [10]. The former consists of methods to reconfigure the circuit under test into an easily testable form or to establish access to internal nodes in order to reduce the test generation effort and to improve fault detection. The latter utilizes analog checkers to determine whether an inherent or explicitly generated invariant property, i.e. a code, is corrupted due to a circuit malfunction. An important advantage of analog checkers is that they alleviate the difficulty encountered in measuring the values of on-chip signals through external means. Moreover, they support not only manufacturing test but also concurrent error detection methods for analog circuits.

Several code-based methods, wherein two identical signals need to be *compared* have been recently proposed. In [3], the output of a programmable biquad that can mimic any biquad in a filter is compared successively to the output of every filter stage when both receive the same input stimulus. The use of continuous checksums for circuits with a state-variable representation is proposed in [1], where two duplicate signals are generated from internal nodes in two different ways and are subsequently compared to detect circuit malfunctions. A pseudo-duplication method is presented in [11], where a checker is used to compare two signals whose nominal values are identical during fault-free operation. In [8], the output of a linear analog circuit is compared concurrently to the output of an error

detection circuit, which converges to the actual output only under nominal conditions and diverges otherwise.

Comparators are extensively used in analog design, with their most important application occurring in analog-to-digital conversion. The sign of their output voltage indicates which of the input signals is larger. For test purposes, however, one is rather interested in the *correlation* between the two signals. Consider, for example, two signals that are expected to be identical when the circuit operates correctly. Since process variations may result in deviations from their nominal values, comparison of these signals cannot be made exact. Rather, a tolerance window within which they are deemed equal is required. Towards this end, the design of self-exercising analog checkers that establish a tolerance window has been studied extensively in [4].

In all the above references, the checker examines whether the inequality $|V_1 - V_2| < V_\delta$ holds, where V_1, V_2 are two expectedly identical input voltages and V_δ is a threshold voltage that accounts for process variations and is statically defined for a specific input value V_o. While this is acceptable for signal values within a narrow band, $V \in [V_o - \Delta V_o, V_o + \Delta V_o]$, $\Delta V_o > 0$, it is too constraining when $V > V_o + \Delta V_o$ or too lenient when $V < V_o - \Delta V_o$. For example, assume that the threshold is set to 10 mV. In this case, for a pair of signals of nominal magnitude 100 mV, a 12 mV deviation in one of them, i.e. a 12% signal discrepancy, is indicated as an error. Similarly, for signals of magnitude 500 mV, the same 12 mV deviation will also be flagged as an error, despite the fact that it constitutes only a 2.4% difference from the nominal value. On the other hand, for a signal of magnitude 50 mV, an 8 mV deviation, which corresponds to a 16% difference from the nominal value, will not be flagged as an error since this deviation is less than the statically defined error threshold of 10 mV. Consequently, when the checker is employed in on-line concurrent error detection, this predefined static threshold will result in inadvertent false positives or false negatives. Similarly, when the checker is employed in manufacturing test, it will incur loss of fault coverage or yield, unless the input voltage range is restricted within the interval $[V_o - \Delta V_o, V_o + \Delta V_o]$. Hence, in order to enhance the quality and accuracy of test, checkers with a *dynamically adjustable* error threshold are necessary.

This problem was first reported in [5], wherein a sample-and-compare circuit implementing a threshold relative to the magnitude of the input signal was proposed. In order to make the operation of this checker as synchronous with the circuit under test as possible, the sampling frequency of the former has to be significantly higher than the actual operational frequency of the latter. The slew-rate of the op-amps in the checker, however, limits the sampling frequency that can be achieved since the checker output has to settle before a new sample is obtained. Increasing the sampling frequency requires that high-performance amplifiers be used, which may increase prohibitively the area overhead. Moreover, charge imbalance in the transistor channels and the capacitor plates due to switching operations may cause erroneous evaluation of small signals.

The aforementioned limitations are resolved in a novel full-*CMOS* design described herein. The area overhead is significantly reduced. Furthermore, the lack of switching activity in the proposed circuit enables continuous signal monitoring, thus revoking the limitations that sampling imposes on the operational frequency of the circuit under test and on the magnitude of the evaluated signals.

The remaining of the paper is organized as follows. In Section 2, we define the relative threshold. In Section 3, we present the actual design of the proposed checker. In Section 4, we illustrate the operation of the checker and its advantages over checkers imposing a statically defined threshold through representative simulations. The properties of the proposed checker are discussed in Section 5.

2. Threshold Definition

The proposed checker monitors two nodes, which ideally, during correct operation, attain the same voltage value, and examines whether the following inequality holds:

$$|V_1 - V_2| < V_\delta \tag{1}$$

where

$$V_\delta = \varepsilon_r \frac{|V_1 + V_2|}{2} + V_{\delta,\min} \tag{2}$$

The threshold is defined as a percentage of the absolute average value of the input signals, plus a small constant, $V_{\delta,\min}$, which accounts for possible offsets. For input signals of zero magnitude, the threshold obtains the minimum value of $V_{\delta,\min}$. Whenever the above inequality is not satisfied, the checker indicates the unacceptable signal discrepancy.

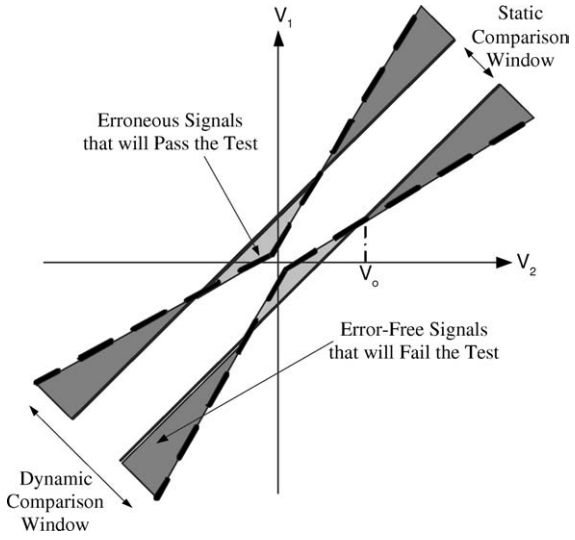

Fig. 1. Code space of duplicate signals considering static and dynamic tolerance.

The advantage of this approach over a statically defined error threshold is demonstrated in Fig. 1, where the space of two signals is represented by the entire plane. The area within the parallel dark lines corresponds to signals that are considered equal when a static threshold is established. In contrast, when a dynamic threshold is utilized, equivalent signals are contained within the dashed lines. Assuming that a percentile deviation is a fairer criterion, shaded regions indicate incorrect assessments when a static error threshold is utilized: signal pairs that are included in the shaded regions will erroneously fail the test if $|V| > V_o$ or will erroneously pass the test if $|V| < V_o$. Such incorrect assessments jeopardize the effectiveness of both concurrent error detection and manufacturing test methods that employ checkers. In concurrent error detection, an error-free signal pair failing the threshold test corresponds to a false negative, while an erroneous signal pair passing the threshold test correspond to a false positive, both of which are undesired. Similarly, in manufacturing test, error-free signal pairs failing the threshold test correspond to yield loss, while erroneous signal pairs passing the threshold test correspond to fault coverage reduction, which necessitates an increased test set.

We should emphasize at this point that the use of any threshold establishes an inherent bias when evaluating a signal pair, independent of the static or dynamic nature of the threshold. This happens because V_δ accounts for the probability of process variations in the circuit under test and the checker itself, as well as for possible small phase offsets between the evaluated signals. Since, the magnitude of these side effects is not known *a priori*, the assignment of V_δ inevitably introduces a bias towards accepting or rejecting a signal pair. For a statically defined threshold, however, the effect of this bias is amplified. In particular, for input test signals of magnitude $|V| > V_o$, the checker exhibits a bias towards rejecting signal pairs while for input test signals of magnitude $|V| < V_o$, the checker exhibits a bias towards accepting signal pairs. When the input voltage band is relatively narrow, the threshold could be defined as a percentage of the middle point of this band and still achieve a satisfactory probability of correct signal pair assessment. However, in most circumstances, where the possible input voltage band is not very narrow, such a statically defined threshold model would lead to an unacceptable probability of incorrect signal pair assessment. In contrast, a dynamically adjustable threshold that is defined relatively to the evaluated signals, moderates the bias and is, therefore, a more appropriate criterion for assessing a signal pair.

3. Circuit Design

The schematic of the proposed checker is shown in Fig. 2. In the following, transistors Q_{ia} and Q_{ib} are matched. The design is based on a fully differential folded-cascode amplifier used in an open-loop configuration (transistors Q_1–Q_6) [2]. The circuit operates as described below.

Transistors Q_7–Q_{12} form two bias chains, which establish consistent bias currents in the branches of the amplifier. The sizes of Q_9 and Q_{12} are chosen in conjunction with the aspect ratios of the other transistors in the bias chain, in order to set the currents and the dc voltage in the output nodes, V_{out}^{dc}, to the desired values. Small-signal analysis of the circuit yields:

$$\begin{aligned} V_{\text{out}}^{+} &= +A_{v1}(V_1 - V_2) \\ V_{\text{out}}^{-} &= -A_{v1}(V_1 - V_2) \end{aligned} \tag{3}$$

where

$$A_{v1} = \frac{g_{m1}}{\left(g_{d_1} + g_{d_4}\right) g_{d_5}/g_{m_5} + g_{d_6}} \approx \frac{g_{m_1}}{g_{d_6}}$$

and g_{m_i}, g_{d_i} are the transconductance and the incremental drain conductance of transistor Q_i, respectively. Each of the outputs of the amplifier is connected to an inverter (transistors Q_{14}–Q_{15}), which is biased to

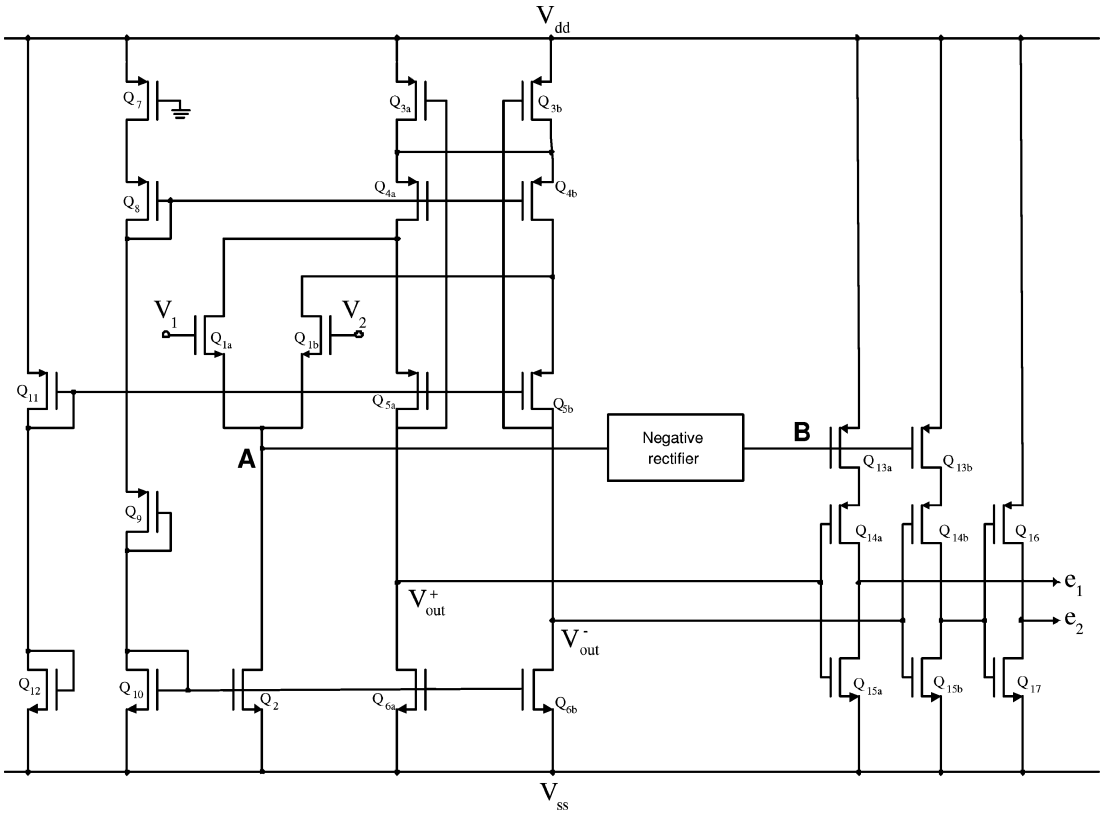

Fig. 2. Schematic of the proposed analog checker with dynamic error threshold.

$V_t > V_{\text{out}}^{dc}$. We define the distance α as:

$$\alpha = V_t - V_{\text{out}}^{dc} \tag{4}$$

Thus, an absolute voltage change of magnitude larger than α in the outputs V_{out}^{+} and V_{out}^{-} will cause one of the two inverters to change state. The distance α is chosen to set the desired test criterion. If

$$|V_1 - V_2| > \alpha A_{v1}^{-1} \tag{5}$$

then the circuit indicates that the discrepancy of the input signals exceeds the tolerance window. In this case, the outputs receive the values $e_1e_2 = 00$ or $e_1e_2 = 11$, depending on the sign of the difference between the input signals. One inverter is triggered by positive changes and the other by negative changes. In contrast, if the input signal deviation is acceptable, the checker indicates fault-free operation by setting $e_1e_2 = 10$.

The error threshold, $V_\delta = \alpha A_{v1}^{-1}$, is made relative to the input signals if the distance α is regulated by their magnitude. This is accomplished by adding a load transistor Q_{13} at each output inverter, as shown in Fig. 2. The voltage in node B regulates the current that flows through the inverters and therefore the bias voltage, V_t, when both transistors are in saturation. It can be shown that:

$$\begin{aligned} V_B &= V_\alpha - \sqrt{\frac{(W/L)_{Q_{15}}}{(W/L)_{Q_{13}}}}\alpha \\ &= V_\alpha - \sqrt{\frac{(W/L)_{Q_{15}}}{(W/L)_{Q_{13}}}}A_{v1}\left(\varepsilon_r \frac{|V_1 + V_2|}{2} + V_{\delta,\min}\right) \\ &= V_\alpha - \sqrt{\frac{(W/L)_{Q_{15}}}{(W/L)_{Q_{13}}}}A_{v1}V_{\delta,\min} \\ &\quad - \sqrt{\frac{(W/L)_{Q_{15}}}{(W/L)_{Q_{13}}}}A_{v1}\varepsilon_r \frac{|V_1 + V_2|}{2} \end{aligned} \tag{6}$$

where

$$V_\alpha = V_{dd} + V_{T_p} + \sqrt{\frac{(W/L)_{Q_{15}}}{(W/L)_{Q_{13}}}}\left(V_{ss} + V_{T_p} - V_{\text{out}}^{dc}\right)$$

Selecting appropriate sizes for the transistors Q_{13} and Q_{15} so that $V_\alpha - \sqrt{\frac{(W/L)_{Q15}}{(W/L)_{Q13}}} A_{v1} V_{\delta,\min} = 0$ Eq. (6) becomes:

$$V_B = -A_{v2} \frac{|V_1 + V_2|}{2} \tag{7}$$

where

$$A_{v2} = \sqrt{\frac{(W/L)_{Q15}}{(W/L)_{Q13}}} A_{v1} \varepsilon_r$$

We proved that the threshold assignment in (2) is achieved if the voltage V_B varies in accordance to (7). The average value of the two input signals is available on node A:

$$V_A = \frac{V_1 + V_2}{2}$$

A circuit that produces the required voltage V_B at the gates of transistors Q_{13} is a negative full-wave rectifier with gain A_{v2}, which accepts as input the voltage on node A(see Fig. 2). The schematic of a wide bandwidth negative rectifier is shown in Fig. 3. Transistors Q_{18}–Q_{22} form a differential output transconductance amplifier and transistors Q_{23}–Q_{24} constitute its bias circuit. The currents I_o^+ and I_o^- are proportional to the input voltage V_A and have equal magnitude and opposite polarity. The diodes D_{1a} and D_{2a} carry out the rectification. Negative output currents I_o^+ flow through diode D_{1a}. Similarly, when $I_o^- = -I_o^+ < 0$, I_o^- flows through diode D_{2a}. Positive output currents I_o^+, I_o^- flow through the clamp diodes, D_{1b} and D_{2b}. respectively, to the negative supply V_{BB}. The voltage source V_{BB} prepares all diodes for conducting at the beginning of their cycle and has a value approximately equal to the sum of the threshold voltages of diodes D_{ia} and D_{ib}, $i = 1, 2$. The combination of the actual diode, D_1, the clamp diode, D_2, and the source V_{BB} is referred to as a pre-biased diode. Due to this pre-bias condition, at high frequencies the rectifier recovers at a rate comparable to dV_A/dt and, thus, the distortion introduced during the zero crossing of V_A is minimal.

In our design, the pre-biased diodes are implemented by transistors [7], as illustrated in Fig. 4. This circuit is equivalent to the pre-biased diode circuit shown circled in Fig. 3. In essence, it is an AB common gate amplifier which operates as follows. The bias circuit Q_{32a}–Q_{33a} produces a very small current which also flows through the diode connected transistors Q_{30b}–Q_{31b}. This current generates a constant voltage drop between the gates of Q_{30}–Q_{31} which is approximately equal to the sum of their threshold voltages, $V_{BB} = V_{T_{Q_{30}}} + V_{T_{Q_{31}}}$. Therefore, V_{BB} keeps the transistors Q_{30a}–Q_{31a} ready for conduction. The input current is generated by the operational transconductance amplifier (transistors Q_{18}–Q_{22} in Fig. 3). Negative input currents flow from the output node through the transistor Q_{30a}, increasing $V_{GS_{Q_{31a}}}$ and driving transistor Q_{31a} into the cut-off region. In contrast, positive input currents flow through Q_{31a},

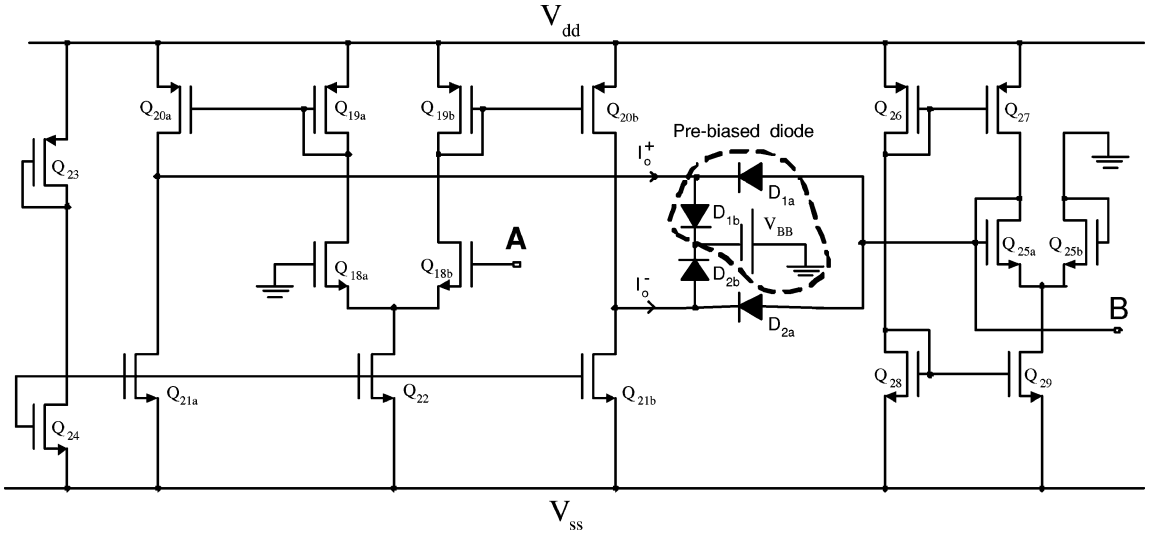

Fig. 3. Schematic of the negative full-wave rectifier.

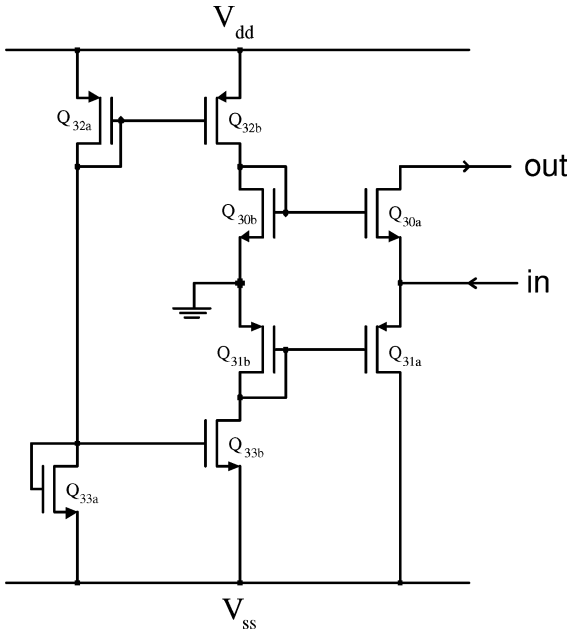

Fig. 4. Transistor level design of a pre-biased diode.

decreasing $V_{GS_{Q30a}}$ and driving, in this case, Q_{30a} into the cut-off region. Hence, $I_{\text{out}} = I_{\text{in}}$ only if $I_{\text{in}} < 0$; otherwise $I_{\text{out}} = 0$.

The output nodes of the two pre-biased diodes in Fig. 3 are connected to an active load (transistors Q_{25}–Q_{29} in Fig. 3). The output voltage of the full-wave rectifier is given by:

$$V_B = -\frac{1}{4} \cdot \frac{g_{m20} g_{m18}}{g_{m25} g_{m19}} \frac{|V_1 + V_2|}{2} \tag{8}$$

Therefore, we have to choose the geometry of Q_{18}, Q_{19}, Q_{20} and Q_{25} such that:

$$\frac{1}{4} \cdot \frac{g_{m20} g_{m18}}{g_{m25} g_{m19}} = A_{v2} \tag{9}$$

Due to the *AB* class operation of the *CMOS* diode circuit, the output of the transconductance amplifier does not saturate, preventing a delay. The internal nodes of the transconductance amplifier are also low impedance nodes. Regarding the fully differential amplifier in Fig. 2, since no voltage shift or differential to single-ended conversion are required, there are no internal high-impedance nodes. Thus, its output terminals settle very quickly. The response at high input frequencies is limited only by the switching characteristics of the inverters. In order to minimize the error detection latency, the checker is designed to be asymmetric, in the sense that the transition to an erroneous state due to an unacceptable input pair is rapid, while the transition into the error-free state is slower [4]. This is achieved by choosing the ratio $(W/L)_{Q_{15}}$ to be large, in order to speed up the falling time of the inverters. The geometry of Q_{13} and Q_{14} is chosen so as to set the desired value of the quiescent error threshold, $V_{\delta,\min}$, while maintaining a ratio $(W/L)_{Q_{14}}$ that is as large as possible, in order to reduce the rise delay of the inverters as well. In our design, the error detection latency starts becoming apparent above 100 KHz.

4. Experimental Results

In order to demonstrate the improved comparison accuracy of the relative threshold model for a wide range of inputs, we compare the response of the proposed checker with a dynamically adjustable threshold to the response of a checker with a statically defined threshold. The static checker is similar to the proposed one, yet without the full-wave rectifier that provides the dynamic adjustment of the threshold. Its threshold is set to 50 mV, which corresponds to a 10% change of $V_0 = 500$ mV. We present simulations for two input pairs that receive values outside the narrow band around 500 mV, in order to show that the static checker is prone to misclassification of the inputs, as opposed to the dynamic checker, which characterizes the inputs correctly. We designed and simulated the two circuits in *PSpice* for a 2 μm technology, using the *EKV* model [9] for the transistors. The circuits run from symmetrical bipolarity supplies of ± 3.3 V. In the following representative simulations, we set $\varepsilon_r = 0.1$, $V_{\delta,\min} = 20$ mV, and we experiment with signals of frequency 100 KHz.

Let us assume that the inputs of the checker are two sinusoidal signals of amplitude 0.8 V and 0.86 V respectively. Since their absolute difference is smaller than the relative threshold throughout their period, the proposed checker indicates correct operation, $e_1 e_2 = 10$, as shown in Fig. 5(a).[1] However, the checker with the statically defined threshold indicates (incorrectly) this nominal deviation of less than 10% as an error: the inverter outputs obtain the values $e_1 e_2 = 11$ and $e_1 e_2 = 00$ [2] around the positive and negative peaks respectively, where the absolute difference exceeds the static threshold of 50 mV, as shown in Fig. 5(b). Thus, false negative indications would occur during concurrent error detection. Likewise, the circuit would be

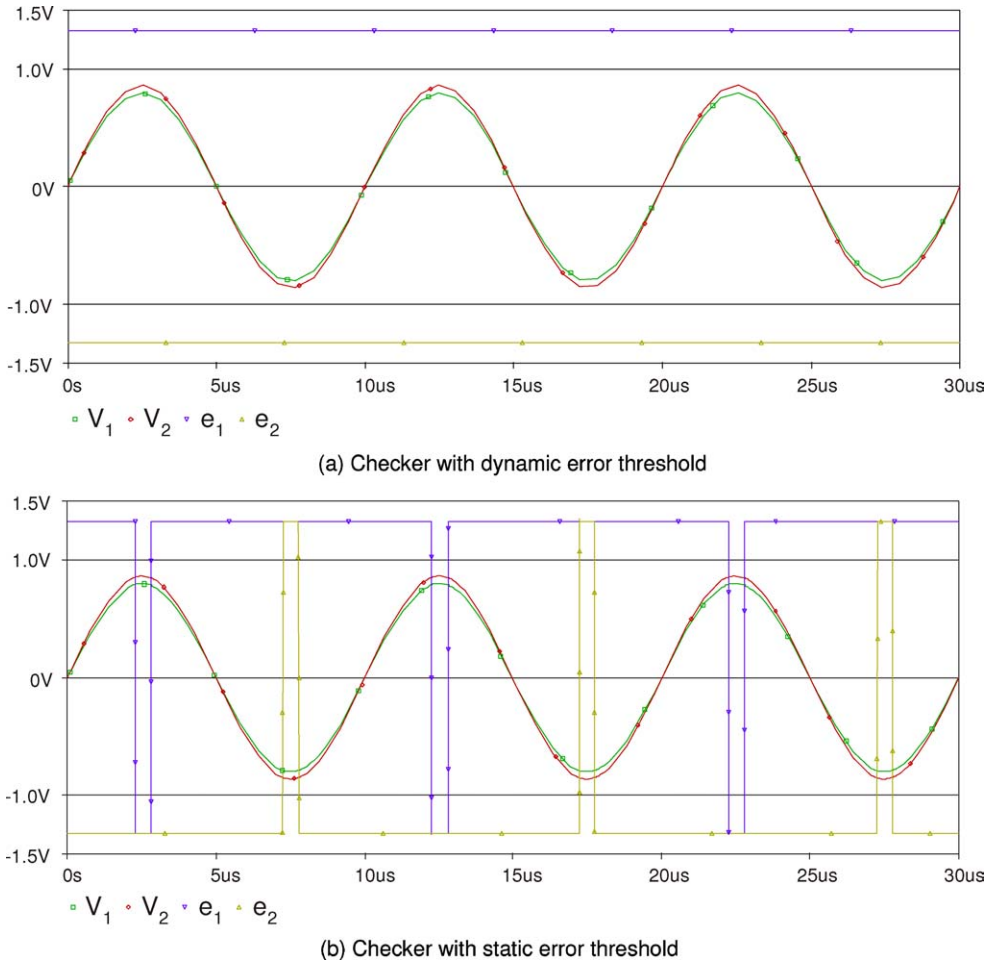

Fig. 5. Simulation of a sinusoidal pair with amplitudes $|V_1|_{\max} = 0.8$ V and $|V_2|_{\max} = 0.86$ V.

discarded as faulty during off-line test, resulting in yield loss.

Let now the inputs of the checker be two sinusoidal signals of amplitude 0.13 V and 0.1 V respectively. In this case, the proposed checker will correctly identify the unacceptably large signal difference, as shown in the simulation of Fig. 6(a). In contrast, as shown in Fig. 6(b), the checker with the statically defined error threshold of 50 mV will not detect the amplitude discrepancy, despite the fact that at the peak of the signals it reaches 26% of their average value. This example shows that false positive indications may occur during concurrent error detection when a static criterion is used. Similarly, it indicates how faulty circuits may evade detection during off-line test.

As a last example, we examine the response of the circuit to a transient error. Such errors inject a charge on a node that temporarily alters the form of the signals appearing at the inputs of the checker. In the simulation shown in Fig. 7, a transient error is manually inserted as a short bidirectional abrupt change in the first input signal, V_1, at 20 us. The checker detects the unacceptable deviation in both directions by raising e_1 or lowering e_2, respectively.

Similar results were obtained through numerous simulations of signal pairs of various shapes and magnitudes. The error detection threshold remains close to 10% of the average value for all of these signals. In order to validate the behavior of the proposed checker in general, we measured the boundary of the acceptance region that the checker projects onto the input signal space. This was carried out by assigning values for V_1 across the input range and measuring the respective value of V_2 for which the output inverters are triggered.

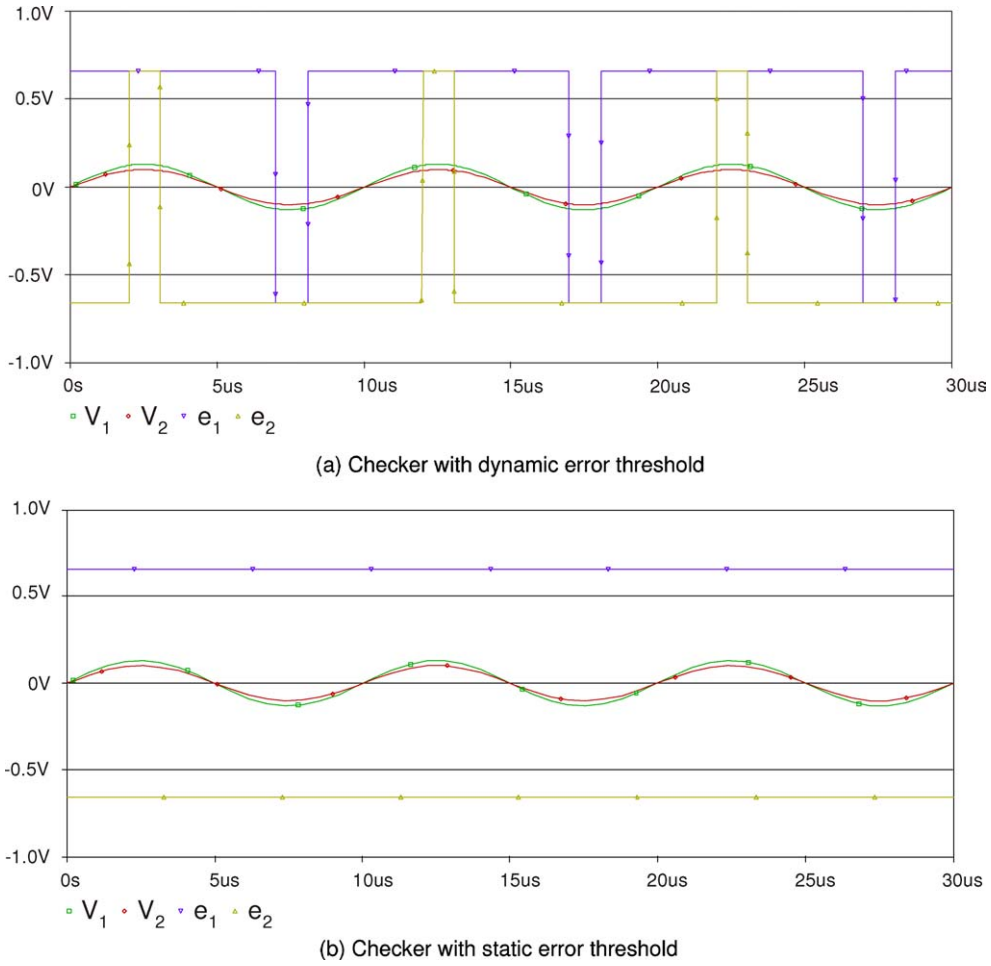

Fig. 6. Simulation of a sinusoidal pair with amplitudes $|V_1|_{\max} = 0.13$ V and $|V_2|_{\max} = 0.1$ V.

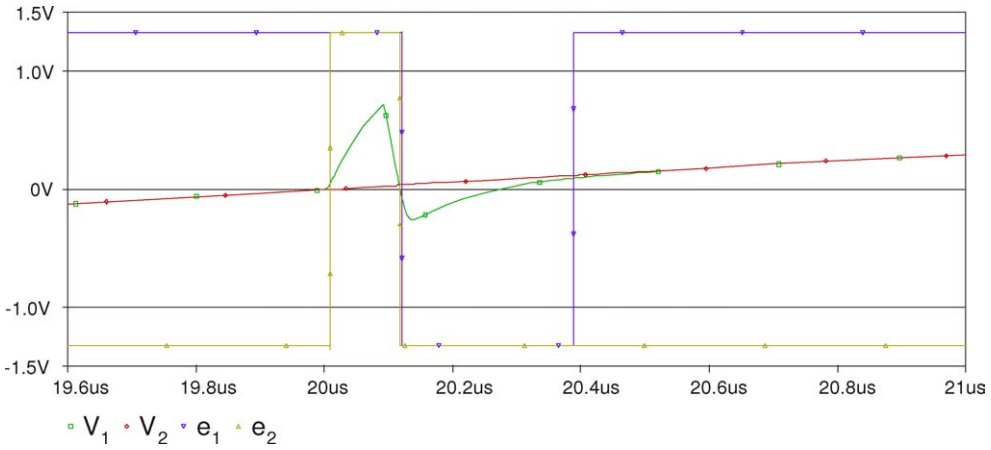

Fig. 7. Simulation of a transient error.

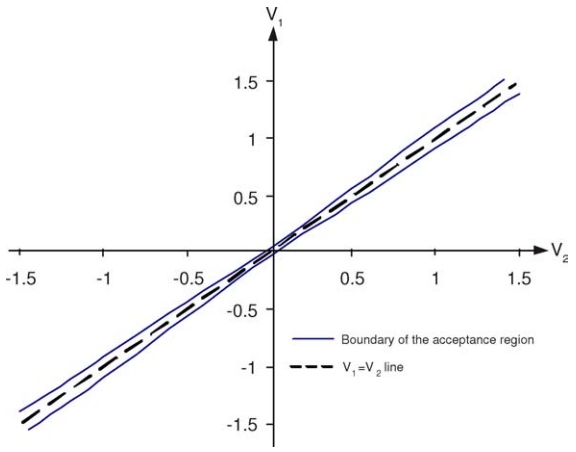

Fig. 8. The boundary that the designed checker projects onto the code space.

For every value of V_1, there are two values of V_2 that produce an error signal. One value corresponds to unacceptable positive changes of the difference $V_1 - V_2$ and the other to unacceptable negative changes of $V_1 - V_2$. It can be seen, that the measured response which is shown in Fig. 8, matches the theoretical boundary shown in Fig. 1. We stress that the acceptable percentile deviation, ε_r, can be set to any value by choosing appropriate transistor sizes.

5. Comments on the Properties of the Checker

As compared to the previous solution [5], the proposed circuit results in lower area overhead since it avoids using costly capacitors, resistors, and op-amps. Moreover, it monitors signals continuously and is able to assess any voltage pair, thus being independent of the circuit under test. In contrast, the switching operations in [5] will cause charge injection, which inevitably, after repetitive comparisons will result in misguided decisions, unless an autozeroing technique is used to discharge the capacitors. Even in this case, charge injection may be a serious limitation when processing low-voltage signals.

In order to achieve a reliable concurrent error detection scheme for the circuit under test, the checker must be code-disjoint [6]; i.e. input values should be mapped to the output code space if and only if they belong to the input code space. Therefore, the checker should indicate its own faults that violate the code-disjoint property. For this purpose, the method presented in [5] is followed, wherein potential faults in the checker are targeted in a short separate test phase, which is performed periodically.

6. Conclusion

Efficient analog circuit test through code-based *DFT* methods necessitates checkers wherein the comparison window is defined as a percentile deviation from the nominal value of the evaluated signals. Towards this end, we presented a low-cost checker that dynamically adjusts the error threshold to the magnitude of its input signals. As discussed theoretically and as demonstrated through simulation, during concurrent error detection, the proposed design resolves the problem of false positive and false negative signal assessments and operates continuously and in parallel with the circuit under test. Furthermore, when utilized in off-line test it results simultaneously in both high fault coverage and low yield loss. In short, the effectiveness of existing checker-based analog test solutions can be significantly enhanced by the accuracy of the proposed checker.

Notes

1. In all figures, the outputs of the inverters, e_1 and e_2, are scaled appropriately to make the waveforms more visible.
2. We remind that when the difference $V_1 - V_2$ exhibits a positive change exceeding the error threshold, the checker outputs obtain the values $e_1e_2 = 11$. Similarly, the outputs obtain the values $e_1e_2 = 00$ when a negative change exceeding the error threshold occurs.

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