-197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS

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Abstract

A 4.3-GHz voltage controlled oscillator (VCO) using an addressable array of cross-coupled minimum size NMOS transistor pairs for post fabrication selection is demonstrated in 65-nm CMOS. An algorithm based on Hamming distance using the phase noise measurements of ~1,500 array combinations was used to identify combinations that have record phase noise of -130dBc/Hz at 1-MHz offset from a 4.3-GHz carrier, while consuming 5.2 mW from a 1-V supply. The operating frequency of circuits using post fabrication selection in its high frequency path is increased to 5 GHz.

Keywords: CMOS, VCO, phase noise, array, cross-coupled transistor pair and process variations.

Introduction

The number of intended dopants and un-intended defects in a minimum sized device is reduced with technology scaling. One missing dopant or having an additional defect can have dramatic impact on device characteristics including threshold voltage, current and noise. The defect density related to 1/f noise in nano-scale CMOS is ~$1x10^{12}cm^{-2}$ or higher [1], which translates to on the average, one trap in ~100 nm^2. In the 65-nm or more scaled CMOS node, the minimum transistor gate oxide area could be on the order of 100 nm^2 or less. In this paper, a VCO topology that embraces the variability of nano-scale transistors to reduce the phase noise of VCO's by taking advantage of minimum sized transistors with a fewer defects or traps through post-fabrication selection [2] is presented.

VCO Design

Fig. 1 shows the VCO topology that uses an addressable array of NMOS cross-coupled transistor pairs for post

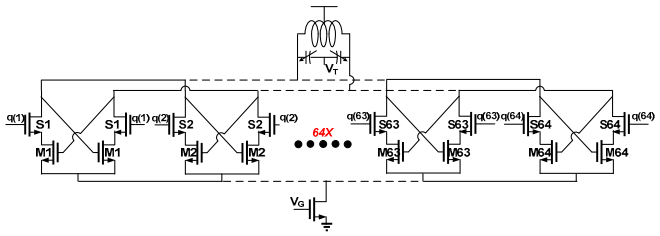

Fig. 1. Array of cross-coupled minimum NMOS transistors.

fabrication selection of pairs with lower noise. To develop this array based design, a conventional VCO using a cross-coupled NMOS pair (8-µm width) with an NMOS tail current source is first designed and then the 8-µm width core transistors are divided into arrays of cross-coupled pairs of minimum sized transistors in a 65-nm process. The top plate of varactors is connected to V_{DD} through the inductors. This minimizes the modulation of output common-mode level by the bias noise current and hence, reducing the phase noise contribution from the AM-PM modulation by the varactors [3]. The inductor is a 5-turn 2.1-nH circular symmetric center tapped structure. The inductor has Q of ~10 at 5GHz. The varactors are of an accumulation mode type implemented as an NMOS structure in an n-well. The tail current transistor channel length of 0.5µm is chosen to reduce the 1/f noise impact of tail current transistor [4].

The transistor forming a cross-coupled pair is divided into 32 transistors of width and length of 250nm and 60nm, respectively. To provide redundancy, 32 additional pairs are added. Each unit also includes 2.5-µm wide switches for selection of a given pair. The switch can be placed at the gate drain or source of the transistor as shown in Fig. 2 [5]. The

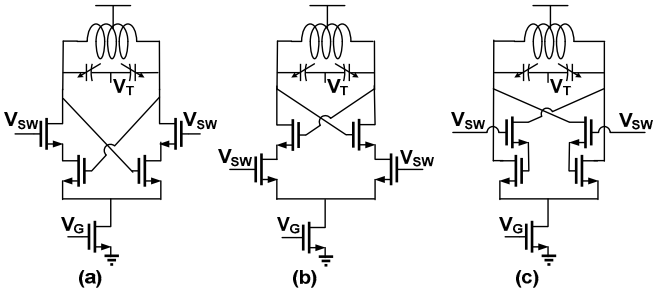

Fig. 2. (a) Drain switched core (b) source switched core (c) gate switched core for VCO.

phase noise with the switch at the gate of the transistor was at least 20 dB worse than that for the VCO with the switch at the drain of the transistor for the same switch size. The switch at the gate can be sized larger to reduce the series resistance but this however unacceptably increases parasitic capacitances of the switch as well as cell area. The switch at the source side of transistor was ruled out as the series resistance of the switch will degenerate the cross-coupled transistor and degrade phase noise by 2.5dB from that with the switch on the drain side. The switches are controlled by a 64-bit serial-in parallel-out falling edge triggered D-flip-flop chain.

Measurement Results

A setup for measuring the phase noise of VCO with different combinations of cross-coupled pair units is shown in Fig. 3. A set of 24/32/40/48 "1" bits is randomly sent through Labview to the DUT using an SPI/I^2C interface and the phase noise measured with a Keysight E4440A spectrum analyzer is collected using Labview. Around 500 combinations were measured for each count of "1" bits. Phase noise of VCO's using two NMOS cross-coupled transistors with 8-µm width were also measured. The minimum phase noise at 1-MHz offset is ~ -118 dBc/Hz. From the histograms (Figs. 4 & 5) of phase noise at 600-kHz and 1-MHz offset from the carrier two observations can be made: (i) variation of the phase noise is close to ~20 dB, and (ii) combinations of cross-coupled minimum sized transistors with lower phase noise than that of the conventional VCO do exist and they can be used to reduce phase noise.

A smart search using a Hamming-based algorithm on the data

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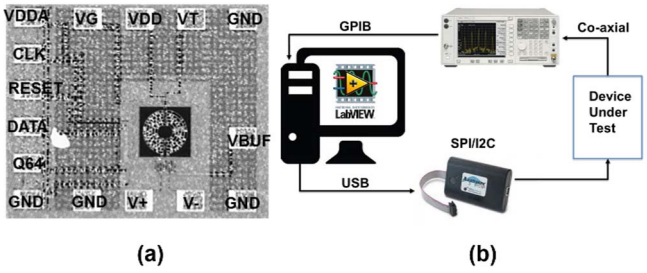

Fig. 3. (a) Die Photograph of chip. (b) Measurement setup.

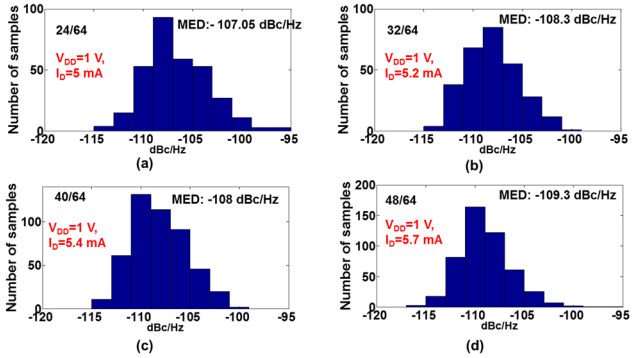

Fig. 4. Histograms of phase noise at 600-kHz offset from the carrier for (a) 24 (b) 32 (c) 40 (d) 48 randomly chosen set of cross-coupled transistor pairs.

is used to identify combinations with reduced phase noise. Using the commonly employed Hamming distance metric, four selection vectors with a minimum distance to the one which produces the lowest offset noise are identified, and then majority vote and absolute majority vote are employed to decide whether the i-th bit in the new selection vector should

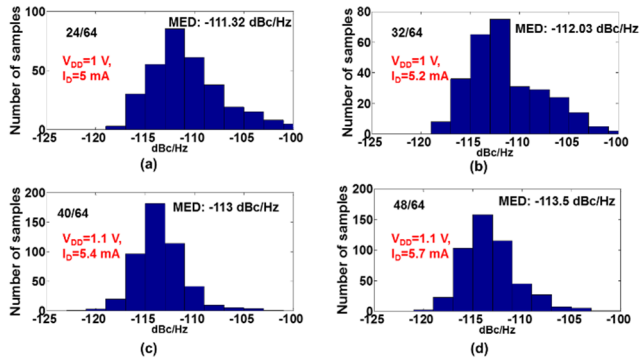

Fig. 5. Histograms of phase noise at 1-MHz offset from the carrier for (a) 24 (b) 32 (c) 40 (d) 48 randomly chosen set of cross-coupled transistor pairs.

be "0" or "1". This procedure is then repeated for the top five selection vectors according to their phase noise from the measurements of randomly generated combinations to create a new set of selection vectors that should result lower noise. Figs. 6(a) and (b) show the histograms of phase noise at 600-kHz and 1-MHz offset for the vectors generated by the proposed algorithm measured using a Keysight E5052B (Signal Source Analyzer). The median phase noise in Fig. 6 is ~7-8 dB lower than the lowest measured using a spectrum analyzer in Figs. 4 & 5. Around 4-5 dB of this difference is due to the use of Keysight E5052B, which better accounts for the drift of VCO output during measurements. The phase noise range is 17.5dB lower. If 32 arrays are randomly chosen from 64 possible arrays, then there are $1.8x10^{18}$ combinations. The 500 measured combinations is a tiny portion. The result in Fig. 6

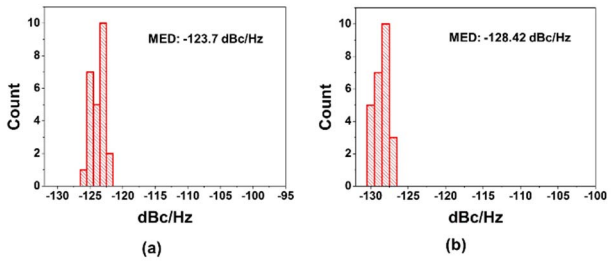

Fig. 6. Histograms of phase noise of combinations found using the hamming metric (a) @ 600 kHz (b) @ 1 MHz offset from the carrier

suggests that the number of measurements needed to select the combination with low phase noise is not impractically high.

The phase noise of VCO with one of the combinations selected by the Hamming distance-based algorithm is measured using an E5052B and shown in Fig. 7(a). The phase noise of VCO is -130dBc/Hz at 1-MHz offset from the carrier frequency of 4.3GHz. The commonly used Figure of Merit (FOM) [11] is plotted in Fig. 7(b). The performance of VCO in this work is compared to that of VCO's from the literature in Table I. The VCO has the lowest phase noise at 1-MHz offset among all VCO's operating around 5 GHz. The VCO has the state-of-art FOM across its tuning range and achieves the lowest FOM of -197dB at 4.3GHz. This work also demonstrated that the operating frequency of circuits using post fabrication selection in its high frequency signal path can be increased to 5GHz. Lastly, an on-chip phase noise measurement technique is needed.

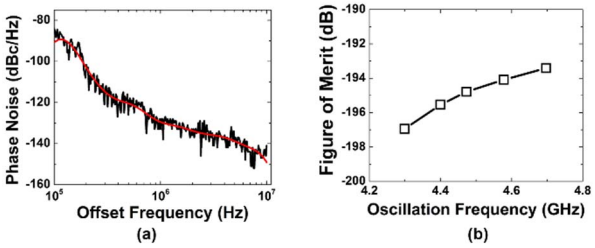

Fig. 7. (a) Phase noise plot of VCO. (b) Figure of Merit of VCO across the tuning range

TABLE I: VCO Measured Performance

	Freq. (GHz)	Tech (nm)	Power (mW)	Lowest Phase Noise at 1-MHz offset (dBc/Hz)	Minimum FOM (dB)
[6]	5-5.42	180	4.2	-127	-195
[7]	9.2-10.4	180	3.6	-115.7	-190.5
[8]	4.84-5.32	180	3.6	-125.8	-194
[9]	2-4-5.3	65	6	-119	-189
[10]	1.97-2.04	350	1	-122.4	-189
This work	**4.3-4.7**	**65**	**5.2**	**-130**	**-197**

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