An Analog Checker with Dynamically Adjustable Error Threshold for Fully Differential Circuits

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Abstract

We present a novel analog checker that adjusts dynamically the error threshold to the magnitude of its input signals. We demonstrate that this property is crucial for accurate concurrent error detection in analog circuits. Dynamic error threshold adjustment is achieved by regulating the bias point of the output stage inverters of the checker, which provide a digital indication of potential errors in the circuit under test. We discuss the theoretical foundation and we present simulations that validate the underlying principle of the design. As compared to previous solutions, the proposed checker reduces the incurred overhead, while significantly enhancing the quality of concurrent error detection.

1. Introduction

As the number of manufacturing steps and the density of integration increases, circuits become more prone to fluctuations that may cause one or more specifications to be failed. While several test methods have been successfully devised for digital circuits, the problem is much harder and existing solutions are not up to par for their analog counterparts. The difficulty arises mainly due to the continuous nature of analog signals and the necessity for accurate measurement of their values. Recent advances, such as the switched-capacitor and switched-current implementations, enable integration of digital and analog circuits on the same substrate. Additionally, as the operating frequency of circuits increases, systems incorporate more analog components. Therefore, developing efficient test solutions for analog circuits becomes essential.

While off-line test methods are capable of detecting manufacturing faults, wear-and-tear faults and transient errors require additional care. In high safety applications, it is desired that the circuit monitors itself and reports potential deviations from its correct functionality. This objective is an absolute necessity in systems where data integrity is vital. Recently, several research efforts address this problem for analog circuits. A comprehensive overview of the proposed methodologies can be found in [1]. In [2, 3], a checker that monitors the common-mode voltage at a conjugate pair of nodes in a fully differential circuit is presented. A balanced checker which examines whether a predefined signal encoding is violated is presented in [4]. In [5], a programmable biquad that can mimic any biquad in a filter is used for on-chip comparison to the transfer function of every filter stage. For circuits with a state-variable representation, the use of continuous checksums is proposed in [6]. A current-mode A/D converter with concurrent error detection capability is introduced in [7]. In [8], a formal theory of self-checking circuits and their properties is established.

The objective of concurrent test is to examine whether signals remain within an acceptable range around their nominal value. Ideally, a checker should be able to detect deviation from the nominal value for all realistic signals and should not interrupt the normal operation of the circuit or degrade its performance. Additionally, it should incur low area overhead and should be able to perform tests at the actual speed of operation. The checkers proposed in [2, 3, 4] implement a predefined, static error threshold. While this is acceptable for signal values close to the value for which the error threshold has been set, it may be too restrictive for larger signals or too lenient for smaller signals. For example, assume that the threshold is set to 10mV. In this case, for a sinusoidal signal of amplitude 100mV, a 12mV deviation, i.e. a 12% signal discrepancy, is indicated as an error. Similarly, for a signal of amplitude 500mV, the same 12mV deviation will also be flagged as an error, despite the fact that it constitutes only a 2.4% difference from the nominal value. On the other hand, for a signal of amplitude 50mV, an 8mV deviation, which corresponds to a 16% difference from the nominal value, will not be flagged as an error since this deviation is less than the statically defined error threshold of 10mV. Evidently, a static threshold may result in inadvertent false positives and false negatives; hence, to enhance the quality of concurrent test, it is crucial to implement a dynamic error threshold.

This problem was first reported in [4], wherein the proposed solution employs a sample-and-compare circuit. In order to make this checker as concurrent with the circuit under test as possible, the sampling frequency of the former has to be significantly greater than the actual operational frequency of the latter. The slew-rate of the op-amps in the checker, however, limits the sampling frequency that can be achieved. This implies that high-performance amplifiers must be used, a fact that may increase prohibitively the area overhead. Moreover, charge unbalance in the transistor channels and the capacitor plates due to switching operations may cause erroneous evaluation of small signals.

The aforementioned limitations are resolved in a novel checker design proposed herein. With the addition of a few

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transistors and diodes to the basic checking structure with static threshold [2, 3], the proposed checker provides the ability to dynamically adjust the error threshold to the magnitude of the examined signal. Since our circuit does not incorporate passive components, the area overhead is significantly reduced as opposed to the sample-and-compare checker [4]. Furthermore, the lack of switching activity in the proposed circuit enables continuous signal monitoring, thus revoking the limitations that sampling imposes on the operational frequency of the circuit under test and on the magnitude of the signal being evaluated.

The remaining of this paper is organized as follows. In section 2, we present the theoretical foundation and the actual design of the proposed checker. In section 3, we illustrate the operation of the checker through representative simulations. A detailed discussion of the advantages and the potential of the proposed checker is given in section 4.

2. Checker Theory and Implementation

We illustrate the underlying principles of the proposed checker for the class of fully differential circuits. In such circuits, the checker monitors both differential paths. The two monitored signals, V^+ and V^-, form a conjugate pair, in the sense that they are of equal magnitude and opposite sign. Thus, in fault-free operation, the common-mode voltage, $V_{com} = (V^+ + V^-)/2$, must remain at a constant value $V^+ + V^- = 2V_{bias}$, where V_{bias} is the bias voltage. The checker examines this inherent property and indicates an error whenever it is violated, i.e. $V_{com} \neq V_{bias}$. The checker, however, has to take into account that due to mismatches in transistors sizes and other non-idealities, there is a tolerance margin within which analog signals are deemed correct. In order to accomplish a margin relative to the amplitude of the signals, the checker has to examine whether the following condition holds:

$$\left| \frac{V^+ + V^-}{2} - V_{bias} \right| < V_\delta = e_r \left| V^m \right| \qquad (1)$$

where $|V^m| = min\{|V^+|, |V^-|\}$, $\varepsilon_r < 1$ and V_δ is the threshold voltage. Here, the threshold is defined as a percentage of the absolute value of the minimum signal, which is compatible to the threshold assignment given in [4]. If the inequality in (1) is not satisfied, the checker should indicate an error occurrence. For simplicity, in the following we will assume $V_{bias} = 0$.

The advantage of this approach over a statically defined error threshold is demonstrated in Fig. 1, where the space of differential signals is represented by the entire plane. The area within the parallel, dark lines corresponds to signals that are considered correct when a static threshold is utilized. In contrast, when a dynamic threshold is utilized, non-faulty signals are comprised within the dashed lines. Assuming that the error threshold is defined as a percentile of the signal magnitude, shaded regions indicate false negative and false positive assessments when a static error threshold is utilized. It is evident that in most circumstances, where the possible input voltage band is not very small, a relative tolerance is more appropriate for assessing the signal pair, whereas a static threshold model would lead to an unacceptable probability of circuit misclassification.

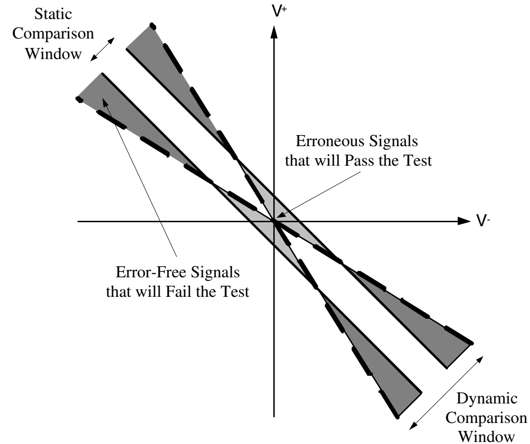

Figure 1. Code space of differential signals considering static and dynamic tolerance.

The basic checking structure with static threshold [2, 3], along with the proposed modification that establishes the desirable dynamic threshold, is illustrated in Fig. 2. Each differential signal is connected to a simple gain stage that reduces its amplitude so that all transistors remain in the saturation region within a safe margin. This is necessary since the linearity of the circuit must be preserved even for large signal amplitudes. The reference voltage V_{ref} is equal to the dc bias of nodes n_1 and n_2 and may be generated internally with some precision penalty. Small-signal ac analysis gives:

$$V_c \approx -A_v \frac{V^+ + V^-}{2}$$
$$V_c' \approx +A_v \frac{V^+ + V^-}{2} \qquad (2)$$

where $A_v = g_{m_1} g_{m_3} / g_{m_2} g_{m_4}$ and g_{m_i} is the transconductance of transistor m_i. A common-mode voltage different than the quiescent value changes the voltages V_c and V_c' from their dc bias V_c^{dc}. Suppose that the two inverters that are connected to the drains of the load transistors m_4 are biased to $V_t > V_c^{dc}$. We define the distance, α, as:

$$\alpha = V_t - V_c^{dc} \qquad (3)$$

The circuit provides a two-rail digital error indication on outputs $e_1 e_2$. During normal operation $e_1 e_2 = 10$. If the following inequality holds,

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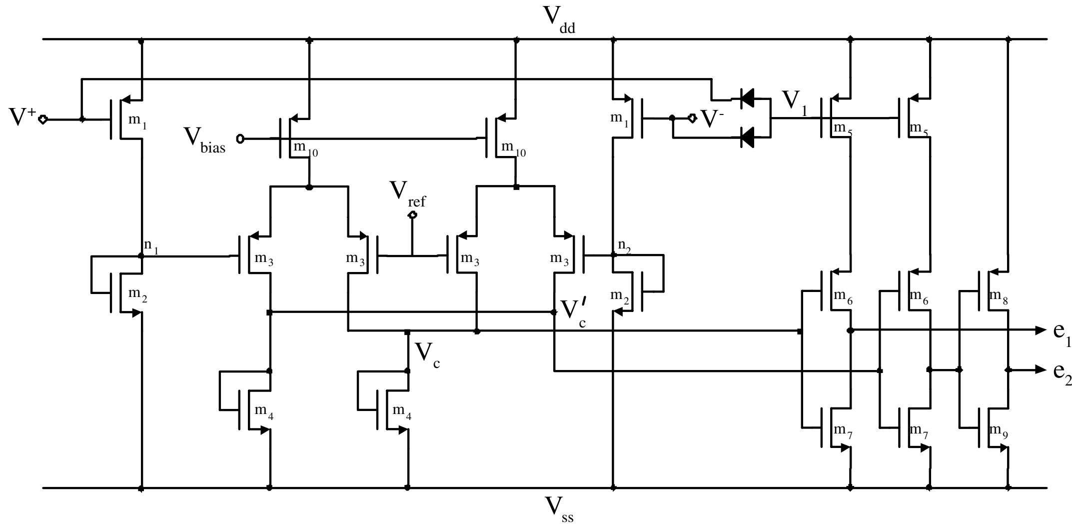

Figure 2. Schematic of the proposed analog checker with dynamic error threshold.

$$\left|\frac{V^+ + V^-}{2}\right| > A_v^{-1}\alpha \tag{4}$$

then the outputs will indicate a circuit malfunction, $e_1e_2 = 11$ or $e_1e_2 = 00$, depending on the sign of the common-mode voltage. One inverter reflects positive changes of V_{com}, while the other reflects negative changes.

Equation (3) shows that the distance, α, depends on the point at which the inverters are biased. This point is located in the middle of the steep region of the inverter's characteristic and corresponds to both transistors being in saturation. We propose to adjust the error threshold dynamically, by making α a function of the input signal magnitude. In order to achieve this, an additional transistor is connected between the positive supply, V_{dd}, and the source of the p-type transistor of each inverter. The gate voltage of these transistors sets the saturation current and, consequently, the distance α. In this case, it can be shown that

$$\alpha \approx V_{ss} - \sqrt{\frac{(W/L)_{m_7}}{(W/L)_{m_5}}}\left(V_1 - V_{dd} - V_{T_p}\right) - \frac{2I_{m_4}}{g_{m_4}} \tag{5}$$

where I_{m_4} is the bias current of m_4.

It remains now to define the mapping $V_1 = f\left(V^+, V^-\right)$. From (1) and (4) we obtain $\alpha = A_v\varepsilon_r|V^m|$. Substituting this value in (5) and solving for V_1 yields:

$$V_1 = -\sqrt{\frac{(W/L)_{m_7}}{(W/L)_{m_5}}}A_v\varepsilon_r|V^m| + V_a \tag{6}$$

where

$$V_a = \left[(V_{dd} + V_{T_p}) + \sqrt{\frac{(W/L)_{m_7}}{(W/L)_{m_5}}}\left(V_{ss} - \frac{2I_{m_4}}{g_{m_4}}\right)\right]$$

If we select the sizes of transistors m_5 and m_7 such that $V_\alpha = 0$ and we set the gain A_v such that $\sqrt{(W/L)_{m_7}/(W/L)_{m_5}}A_v\varepsilon_r = 1$, then it turns out that

$$V_1 = -|V^m| \tag{7}$$

Note that there is enough freedom in the design to achieve this linear relationship.

A simple full-wave rectifier is used to produce this voltage at the gates of transistors m_5, as shown in Fig. 2. Since it is not known in advance which branch carries the signal of minimum magnitude, both of them need to be monitored. The two differential signals are connected to the cathodes of the two diodes[1]. During one half of the signals' period, $V_1 = -|V^+|$, while during the other half, $V_1 = -|V^-|$. Thus, strictly, (7) is not satisfied during the entire period of the signals. However, this does not reduce the effectiveness of the error detection scheme. Indeed, assume, without loss of generality, that there is a time frame where $|V^-| < |V^+|$ and $V_1 = -|V^+|$. The only manner in which a small deviation in V_{com} will not be detected, despite (1) being violated, is when $\varepsilon_r|V^-| < |V_{com}| < \varepsilon|V^+|$. For example, for an allowed percentage deviation of $\varepsilon_r = 0.05$, this yields $1.1|V^-| < |V^+| < 1.11|V^+|$. Therefore, the input voltage band for which a deviation will not be detected is very narrow; this implies that, practically, it may be sufficient to make V_1 dependent on just one of the differential paths. Indeed, in the above example, making V_1 screen any of the two differential paths is sufficient for detecting a deviation $||V^-| - |V^+|| > 0.11|V^-|$. Note that according to the threshold that was set initially, a deviation of up to $||V^-| - |V^+|| = 0.1|V^-|$ is acceptable.

We emphasize that the proposed checker does not rely on any assumptions regarding the type of potential faults. The only faults that will not be detected by our checker are those that cause errors of identical magnitude and opposite sign in the conjugate pair. Yet, the number of such faults is very

[1]For simplicity, we assume that the quiescent common-mode voltage of the conjugate pair is set to analog ground. If a nonzero value is assumed, two simple dc voltage-shifters may be used between the differential signals and the cathodes of the diodes so that V_1 tracks only the ac signals [9].

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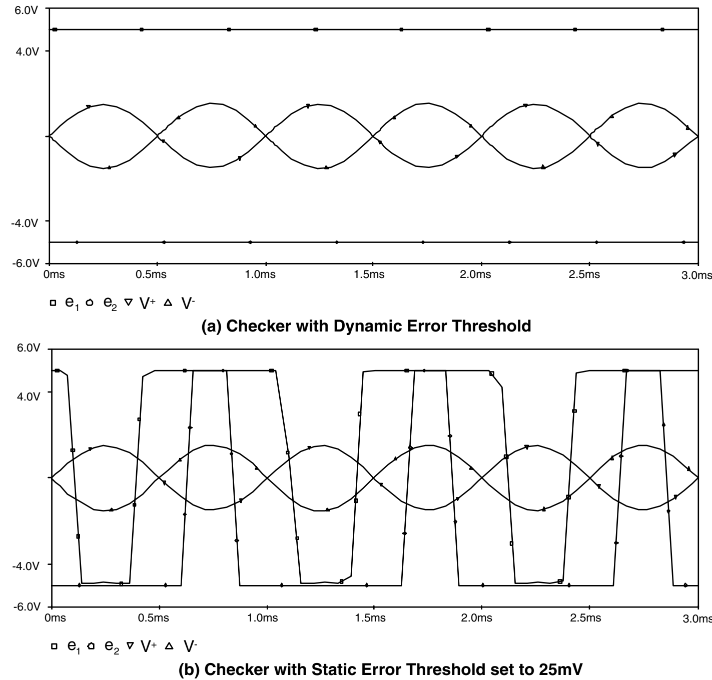

Figure 3. Simulation of a differential sinusoidal pair with amplitudes $|V^{+}|_{max} = 1.5V$ and $|V^{-}|_{max} = 1.54V$.

small and the probability of their appearance may be diminished by redesigning some parts of the circuit under test [2].

3. Simulation Results

In this section, we present SPICE simulations that demonstrate the ability of the proposed checker to establish a more accurate assessment criterion than previously reported checkers with static error thresholds. In the following simulations, we set the error threshold to $\varepsilon_r = 0.05$ and we experiment with signals of frequency 1 kHz.

Let us assume that the error-free response of a circuit under test consists of two sinusoidal signals of amplitude 1.5V and opposite polarity. Let us also assume that the static error threshold of a checker is set to 5% of a signal of amplitude 0.5V, i.e. to 25mV. Suppose now that a fault in the circuit under test causes an amplitude deviation of 40mV in one of the two waveforms. Since this deviation is less than 5% of the nominal value, the proposed checker indicates correct operation - $e_1e_2 = 10$ -, as shown in Fig. 3(a). However, the checker with the statically defined error threshold indicates (incorrectly) this nominal deviation of less than 5% as an error - $e_1e_2 = 11$ and $e_1e_2 = 00$[2] -, as shown in Fig. 3(b).

Let us now assume that the error-free response consists of two sinusoidal signals of amplitude 0.1V and opposite polarity, and that a fault causes an amplitude deviation of 20mV in one of the two waveforms. In this case, the proposed checker will correctly identify the occurrence of an error, as shown in the simulation of Fig. 4(a). In contrast, the checker with the statically defined error threshold of 25mV will not indicate the error despite the fact that the deviation amounts to 20% of the nominal amplitude, as shown in Fig. 4(b).

As demonstrated through the above examples, accurate error identification, invariably defined as a percentile deviation from the nominal value, requires that the error threshold be adjusted dynamically to the amplitude of the evaluated signal. Similar results were obtained through numerous simulations of signals of various shapes and magnitudes within the 5V differential range. The error detection threshold remains close to 5% for all these values, that is, it is dynamically adjusted. We stress that the threshold can be set to any value by choosing the appropriate transistor sizes.

The last example accounts for the occurrence of transient errors. Such errors inject a charge on a node that temporarily alters the form of the signals appearing at the inputs of the checker. In the simulation depicted in Fig. 5, a transient error is manually inserted as a bidirectional abrupt change in the inverting signal V^- at around 2ms. The checker indicates the erroneous common-voltage change in both directions. As explained in [2], a latch is necessary in this case, in order to hold the error indication until it is reset, thus providing a steady error detection signal.

4. Discussion

An important characteristic of the proposed checker is its low area overhead as compared to the previous solution [4],

[2]We remind that when the common-mode voltage shows a positive change exceeding the error threshold, the checker outputs obtain the values $e_1e_2 = 11$. Similarly, when a negative change exceeding the error threshold occurs the outputs obtain the values $e_1e_2 = 00$. When the two signals are close to zero, the common-mode voltage does not exceed the error threshold and the outputs obtain the correct operation values, i.e $e_1e_2 = 10$.

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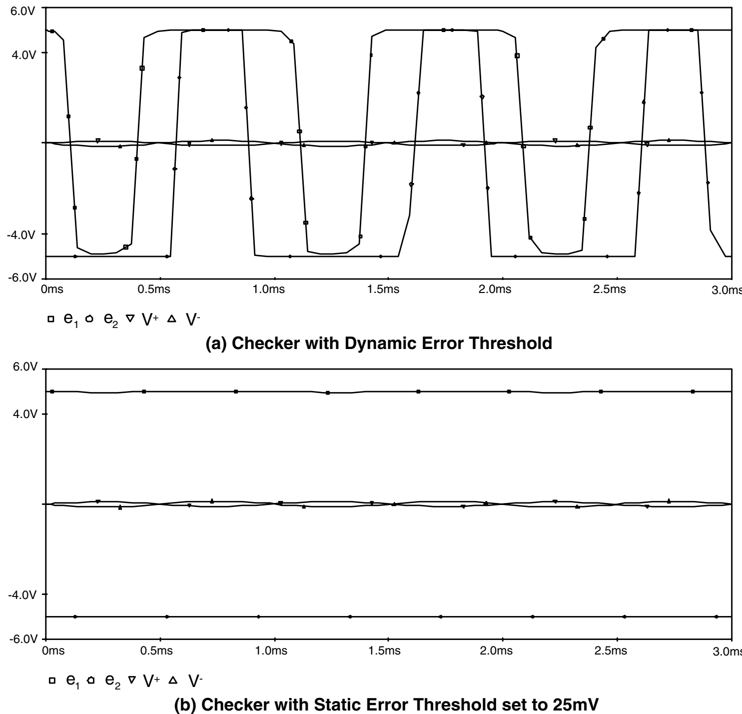

Figure 4. Simulation of a differential sinusoidal pair with amplitudes $|V^{+}|_{max} = 0.1V$ and $|V^{-}|_{max} = 0.12V$.

which incorporated costly capacitors and op-amps. The dynamic error threshold is obtained through minor additions to the basic balanced checker with static error threshold proposed in [2, 3]. More specifically, our design comprises two additional transistors to modify the output-stage inverters, two diodes to rectify the input signals and, if necessary, four transistors to implement the dc-level voltage shifters. These modifications incur an insignificant area increase over the low-cost checker with static error threshold [2].

Another important feature of the proposed checker is that it is independent of the circuit under test. Its properties are described at an abstract level in terms of fault-free and faulty output functions. Moreover, the checker evaluates correctly actual stimuli which may obtain any value within a wide range and is, therefore, appropriate for concurrent error detection. In contrast, an implementation with static error threshold will inevitably result in many false alarms, unless the range of the input signals is restricted to a narrow band around the signal to which the error threshold is preset.

Unless a fault occurs in the proposed checker, it is code-disjoint [8], i.e. input values are mapped to the output code space if and only if they belong to the input code space. As a result, fault-security is achieved for the circuit under test. In order to also achieve the finite totally self-checking (TSC) property [8] for the functional circuit, the first erroneous signal needs to be detected by the checker. Therefore, in the presence of a fault, the checker must either retain the code-disjoint property or indicate its own faults that violate it. For this purpose, the method presented in [4] is followed, wherein an off-line test phase is applied periodically to the checker. Fault simulation of a pair of non-differentially encoded pulses of magnitude 0.12V reveals their ability to detect all faults that were inserted in the checker. The fault list includes all possible shorts (drain-gate, drain-source, gate-source) as well as all possible opens (drain, gate, source) in all transistors. A short is modelled by a small resistor 10Ω and an open by a large resistor $1\text{M}\Omega$. Several parametric faults were also simulated and detected by these waveforms.

In the past, checkers implementing a static error threshold have been employed to enhance the off-line testability of fully differential circuits [2, 3, 10]. These methods were applied to filters, wherein it is demonstrated that all target faults within op-amps are detected by placing a checker at their outputs [2]. Regarding faults external to the op-amps, it is more effective to place checkers at their inputs, as variations of the common-mode signal are substantially larger at the inputs than at the outputs. This happens because a differential amplifier has the capability to suppress the output common-mode voltage, which it compensates for by a small change of the input common-mode voltage. However, the reported results show a very small coverage of *parametric* faults. Apparently, unless a parametric fault causes one of the outputs of the op-amp to hit the supply rails, the change of the input common-voltage will not be sufficient for the checker to detect this fault, except when a very small V_{com} swing is allowed. The side effect of a very small V_{com}, however, is that it may lead to inadvertent yield reduction. In [11], it is reported that by setting the threshold such that the yield of the test process is approximately 90%, the method results in a very small parametric fault coverage of only 8.1%.

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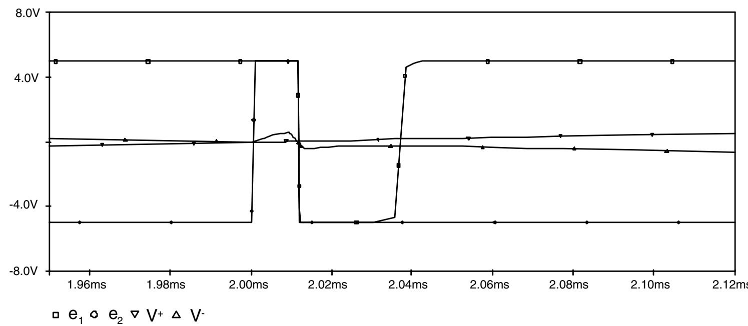

Figure 5. Simulation of a transient error.

Conversely, employing the proposed checker with dynamically adjustable threshold for off-line test would result in both high yield and high parametric fault coverage. In the presence of a parametric fault, the common-mode voltage shift in the inputs or outputs of the op-amps is expected to be smaller than the respective shift in a conjugate pair of nodes that are neither inputs nor outputs of op-amps. Thus, a checker becomes more sensitive to the occurrence of a fault if it monitors such a conjugate pair. The proposed checker takes advantage of this point, since it has the ability to respond accurately to any input stimulus and may, therefore, be used to assess any conjugate pair. In contrast, a checker with static error threshold restricts the evaluated signals within a narrow band so as to avoid circuit misclassification. When such a checker monitors a conjugate pair other than inputs or outputs of op-amps, the selection of its error threshold requires a priori knowledge of the nominal value of the signals in these nodes. In this case, the checker depends on the circuit under test, a fact that is unacceptable. This limitation is alleviated if instead we employ the proposed checker with dynamically adjustable threshold. Hence, in addition to the accuracy that the proposed scheme achieves in concurrent error detection, it can also be used effectively for off-line test purposes.

Finally, while concurrent error detection with dynamic error threshold was demonstrated on the class of fully differential circuits, the underlying principle has the potential to be applied to checkers that monitor other codes as well.

5. Conclusion

Accurate concurrent error detection in analog circuits requires that the comparison window be defined as a percentile deviation from the nominal value of the evaluated signal. Towards this end, we presented a fully symmetric checker that dynamically adjusts the error detection threshold to the output signals of the circuit under test. As discussed theoretically and as demonstrated through simulation, the proposed design resolves the problem of false positives and false negatives occurring when concurrent test is performed by checkers with a statically defined error threshold. The proposed checker operates continuously and in parallel with the circuit under test and, therefore, ensures concurrent error detection. Furthermore, it incurs low area overhead and does not impact the performance of the circuit. Finally, the error detection accuracy achieved by the proposed checker facilitates off-line test, providing new directions for enhancing test generation and simplifying test application for analog circuits.

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