Objective
In this assignment, you are asked to simulate the CMFB circuits discussed in class and determine their sensitivity to process variations and component mismatch. Please follow these steps in your work.

1. FD amplifier. Design a five-transistor FD amplifier shown in class. You can set the overdrive voltages of all transistors in your design to 100-200 mV and the tail current source to 2 mA and size your transistors accordingly. This will serve as your test bench for many other assignments of this semester. Use the 2.5-V, 250-nm process file posted on the course web for this design. You should also assume a 10-pF capacitive loading on each of the output nodes. Set the input and output CM levels to $V_{DD}/2$.

2. Biasing circuit. You are allowed for one ideal floating current source of 0.1 mA. You can construct current mirrors using this ideal source.

3. CMFB circuits. You are asked to design all three CMFB circuits discussed in class, i.e., the CT replica amplifier type, the CT amplifier with triode transistors, and the switched-capacitor one. For the second, you can set $V_B$ to around 50 mV, while for type 3, you may assume a 10-MHz two-phase clock to drive the SC. Use real transistors instead of ideal models for the switches.

4. Simulate the large-signal voltage transfer functions (VTFs) of $a_{cmc}$ path and $a_{cmfb}$ path. Plot the two VTFs on the same graph and determine the CM operating point (OP) of your amplifier and CMFB circuit.

5. Close the CMFB loop. Does $V_{OC}$ stabilize at the solution you determined in part 4? If so, determine the exact value of $a_{cmc}$ and $a_{cmfb}$ at this OP. Verify that all transistors are working properly in the right operation regions.

6. Repeat parts 4 and 5 for all three types of CMFB circuit you designed in part 3.

7. Add an offset voltage to the gate of the tail current transistor to emulate a threshold voltage mismatch and sweep this offset in the range of [-50 mV, 50 mV]. Show the graph in part 4 of the OP trajectory for all three CMFB circuits.

8. Vary the width of the tail current transistor by ±10% and repeat the simulation in part 7.

Report Guideline
Write a concise report, not exceeding 3 pages for text and 2 pages for figures. Please typewrite your report with simulation results/figures attached. **Attach your SPICE decks in an appendix.**

Teamwork Policy
Individual work is expected. Discussion with others in class is encouraged. However, please submit a genuine report and design. **No sharing of SPICE decks.**