**Objective**

In this assignment, you are to perform return-ratio (RR) and loop-gain (LG) simulations on the fully differential amplifiers you designed before. The closed-loop configuration of your amplifier is shown below. The total capacitive loading should be close to 10 pF. The CT CMFB loop should be always connected to ensure proper CM levels at the output (and at the summing nodes). Use real-transistor CMFB circuits instead of ideal level shifters. You are free to choose the input CM bias (at $V_{id}$ side); the output CM bias (at $V_{od}$ side) must be set to close to $V_{DD}/2$.

1. Take the 5-transistor amplifier you designed in HW #1 and bias its input (at $V_{id}$ side) to set the output swing (at $V_{od}$ side) to 0 V. Break the loop open at the summing nodes, properly set up the DC bias of the circuit and simulate the generalized return ratio of the loop.

2. Repeat part 1 by breaking the loop open at the output nodes and record the RR again.

3. Simulate the loop-gain of the differential loop and compare with the RR’s.

4. Plot the Nyquist diagrams of the RR’s and LG obtained in steps 1-3.

5. Repeat parts 1-4 for the active-cascode amplifier you designed in HW #4.

6. Devise a simulation to obtain the RR of the common-mode feedback loop. You might want to break the loop open either at the output nodes or at the gate of the tail current transistor. Repeat this simulation with the main differential feedback loop open/closed. Does it make any difference for the RR measured? Why or why not? In this part, you only need to deal with the amplifier you designed in HW #4.
Report Guideline

Write a concise report, not exceeding 3 pages for text and 2 pages for figures. Please typewrite your report with simulation results/figures attached. Attach your SPICE decks in an appendix.

Teamwork Policy

Individual work is expected. Discussion with others in class is encouraged. However, please submit a genuine report and design. No sharing of SPICE decks.