

# Modern ASIC Design

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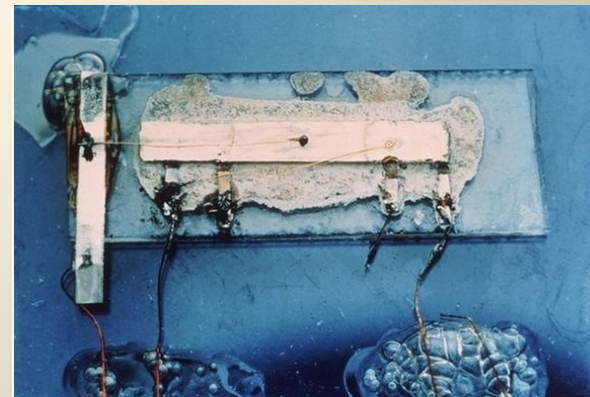
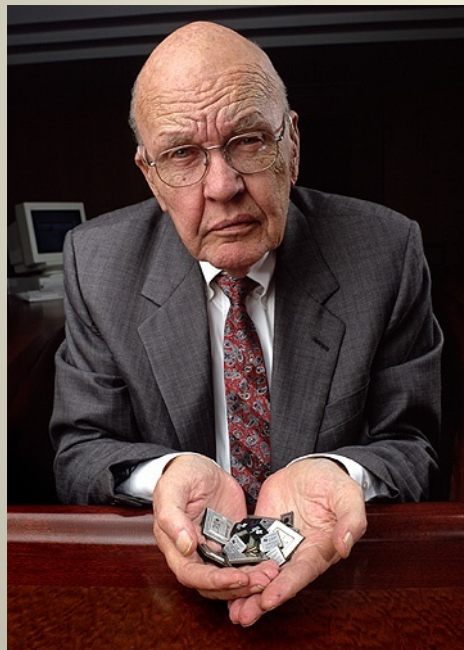
# Chapter 1 Introduction

- Objectives
  - History and road map of integrated circuits
  - Application specific integrated circuits
  - Design flow and tasks
  - Electric design automation tools
  - ASIC project MSDAP

# History of Integrated Circuits

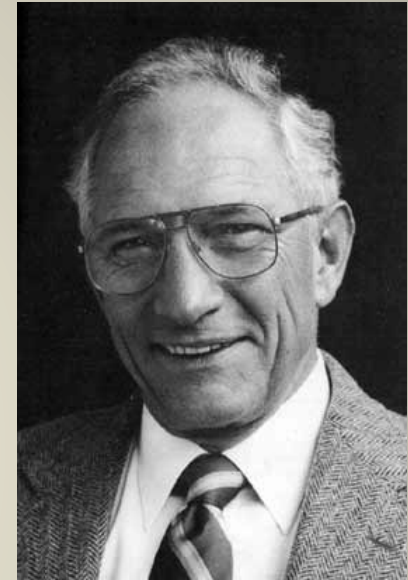
- In 1951 William Shockley developed the world first junction transistor.
- One year later Geoffrey W. A. Dummer published the concept of the integrated circuits (IC).
- In 1958 Jack Kilby at Texas Instruments suggested the integration of circuit elements such as resistors, capacitors, and transistors into a single chip made of the same material.

- By September 12th of the same year, Kilby had built a simple oscillator IC with five integrated components. This marked the beginning of the modern IC industry.



- In 2000, the importance of the IC was recognized when Kilby shared the Nobel Prize in physics with Zhores I. Alferov and Herbert Kroemer. Kilby was cited by the Nobel committee “for his part in the invention of the integrated circuit”.

- Robert Norton Noyce is also credited for the invention of the integrated circuits. In 1957 Noyce and several other engineers founded Fairchild Semiconductor, where in 1959 he developed the integrated circuit.
- In 1968 Noyce and his two Fairchild colleagues founded Intel, with Noyce as president and chief executive officer.

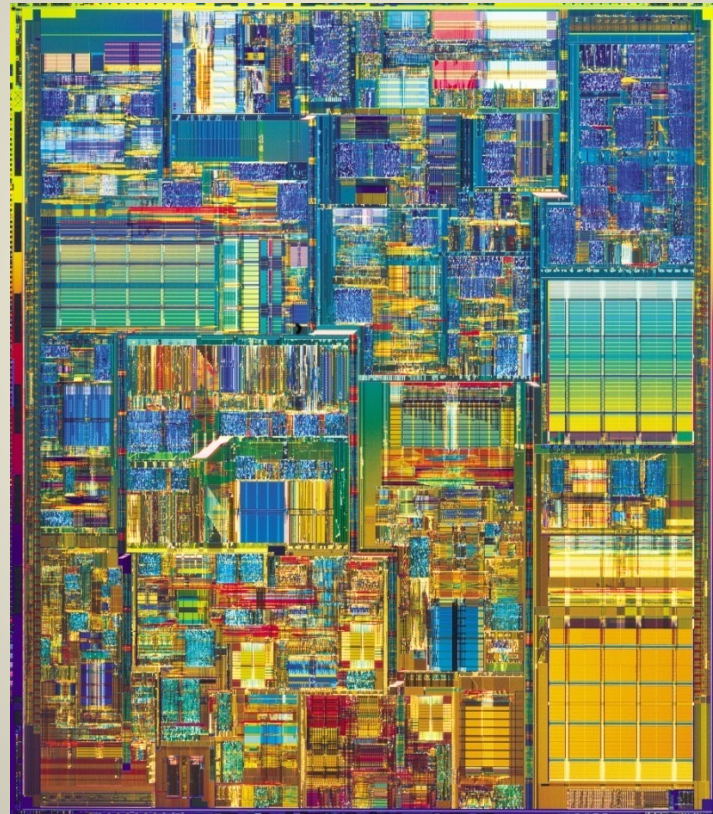


- The understanding of semiconductor physics as well as twentieth century technological advancements in semiconductor device fabrication contribute to the rapid and continuous development of modern IC industry.
  - The integration of large numbers of semiconductor transistors into a small silicon chip was an enormous improvement over the manually assembled circuits, which used discrete electronic components.
- The integrated circuits' mass production capability, reliability, and computer-aided design tools propelled the rapid adoption of ICs in replacing designs using discrete transistors.

- The advantages of ICs over discrete circuits are primarily cost and performance.
  - Cost is low because the chips, with all of their components, are printed via a photolithography process, and millions of transistors can be manufactured and connected at the same time.
- Smaller feature size leads to a high performance because the components switch quicker and consume less power, due to the fact that the components are small and close together

- Among the most advanced integrated circuits are the microprocessors, which control everything from computers and cellular phones to digital microwave ovens.
- In the last decade, 32- and 64-bit microprocessors with cache memory, floating-point arithmetic units, and multi-million transistors on a single piece of silicon have been made popular, marking the era of very large-scale integration (VLSI).

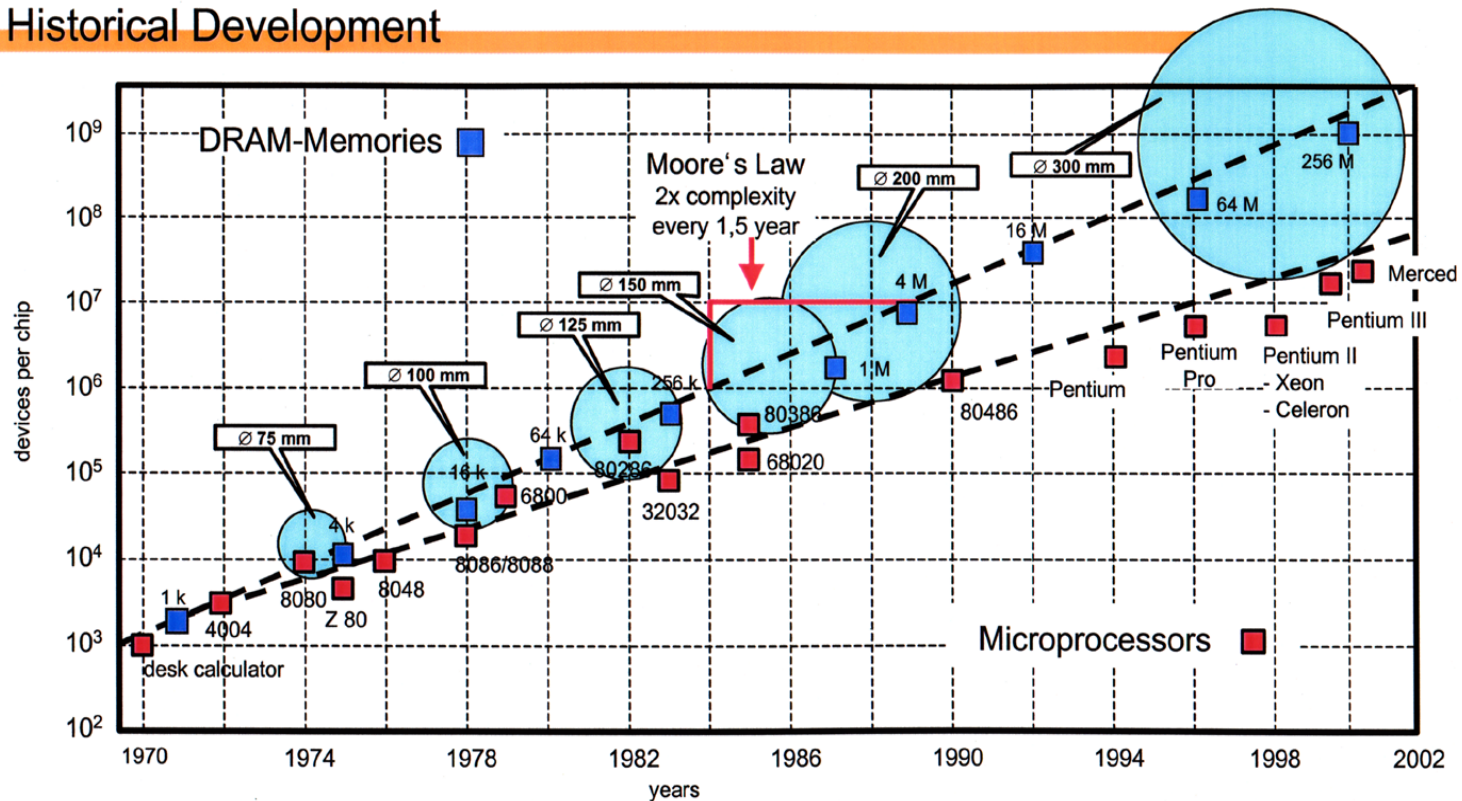
- Pentium 4 microprocessor



- The speed and power consumption gains achieved by narrowing feature size are apparent in almost all applications.
- The state-of-the-art technology for the massive production has reached feature sizes as fine as  $22nm$  and below (ITRS 2009).
- Moore's law: the number of components per IC doubles every year.
  - Moore's law was later amended to: the number of components per IC doubles every 18 months.

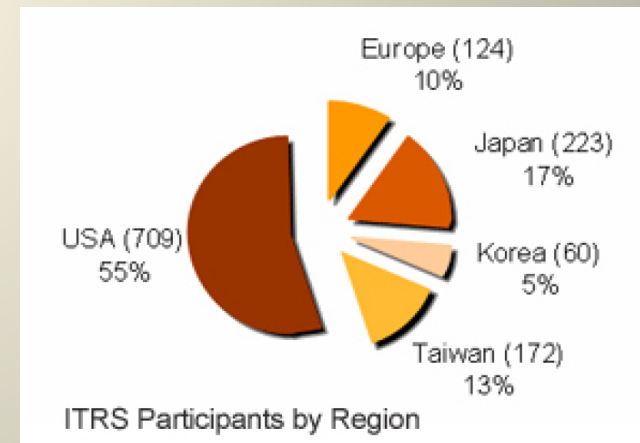
- Historical development of ICs during the period from 1970 to 2002

## Historical Development



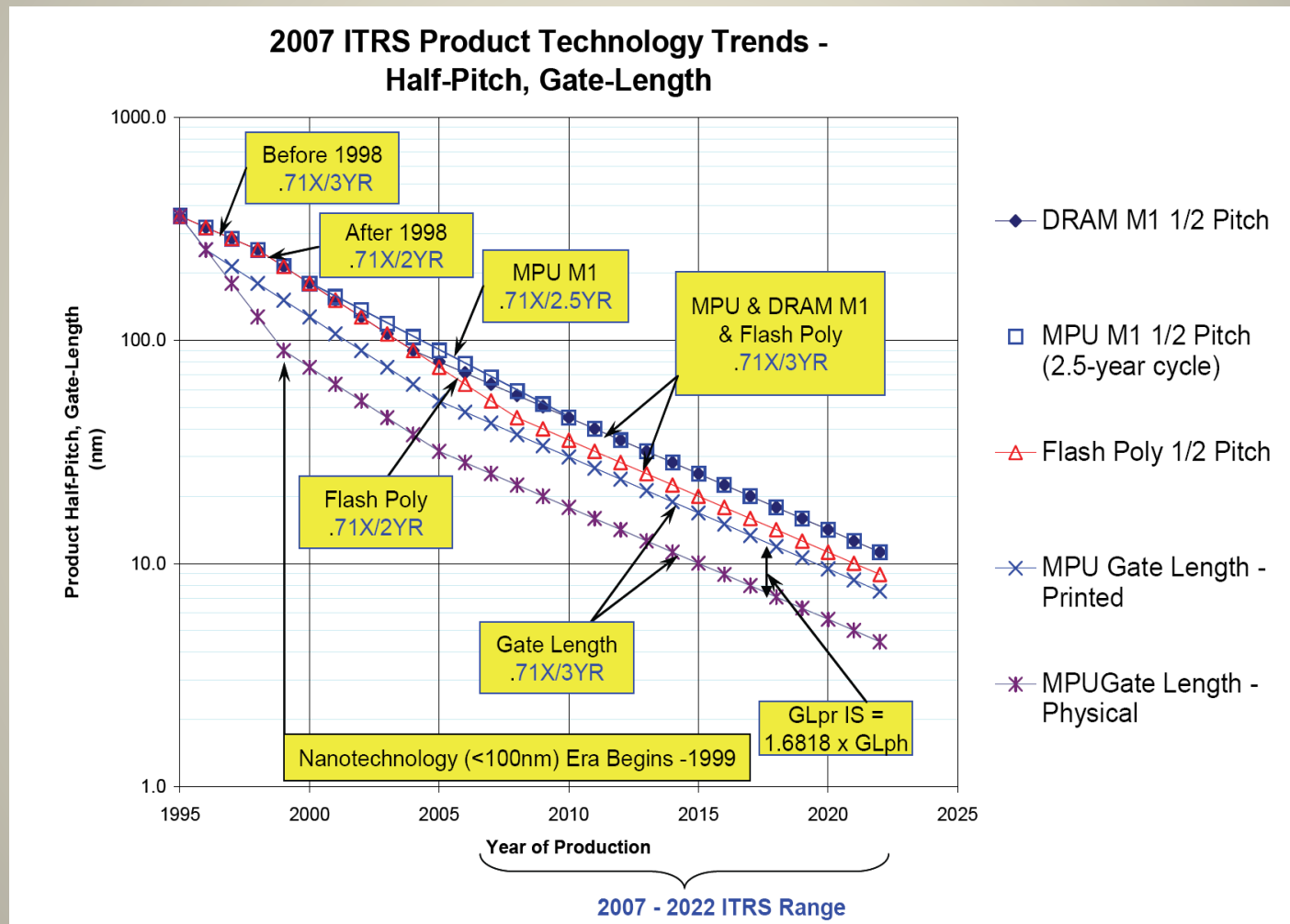
# Roadmap of IC Technology

- International Technology Roadmap for Semiconductors, known throughout the world as the ITRS, collects and analyses the information from major IC companies, and provides a roadmap of technology milestone targets for the years to come.
- The International Technology Roadmap for Semiconductors is sponsored by five leading chip manufacturing regions in the world: Europe, Japan, Korea, Taiwan, and the United States.



- The objective of the ITRS is to ensure cost-effective advancements in the performance of the integrated circuits and the products that employ such devices, thereby continuing the health and success of this industry.
- Through the cooperative efforts of the global chip manufacturers and equipment suppliers, research communities, and consortia, the roadmap teams identify critical challenges, encourage innovative solutions, and welcome participation from the semiconductor community.
- Road map is the most valuable source based on which we plan, explore and “guess” the future of IC industry.

- Roadmap of product half-pitch and gate length (ITRS 2009)



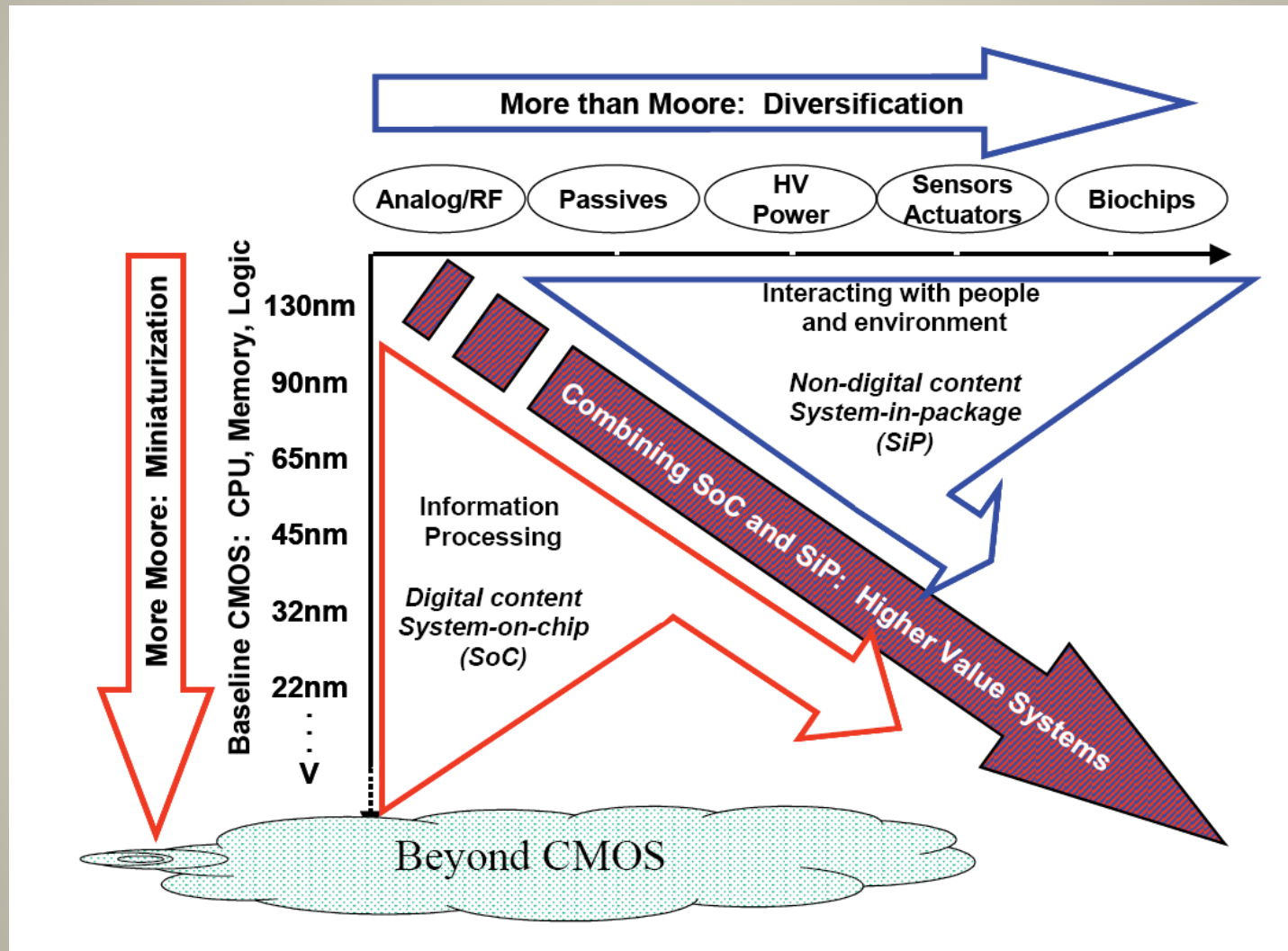
- Roadmap versus actual trend numbers (DRAM Product Trend Example)

<i>YEAR OF PRODUCTION</i>	1995	1998	2000	2002	2003	2004	2006	2007	2009	2010	2012	2013	2015	2016	2018	2019	2022
<i>Calculated Trend Numbers (nm)</i>	<b>360</b>	<b>255</b>	<b>180</b>	<b>127.3</b>	<b>101</b>	<b>90</b>	<b>71.4</b>	<b>63.6</b>	<b>50.5</b>	<b>45</b>	<b>35.7</b>	<b>31.8</b>	<b>25.3</b>	<b>22.5</b>	<b>17.9</b>	<b>15.9</b>	<b>11.3</b>
<i>ITRS Rounded Numbers (nm)</i>	<b>350</b>	<b>250</b>	<b>180</b>	<b>130</b>	<b>100</b>	<b>90</b>	<b>70</b>	<b>65</b>	<b>50</b>	<b>45</b>	<b>36</b>	<b>32</b>	<b>25</b>	<b>22</b>	<b>18</b>	<b>16</b>	<b>11</b>

- DRAM introduction product generations and chip size model

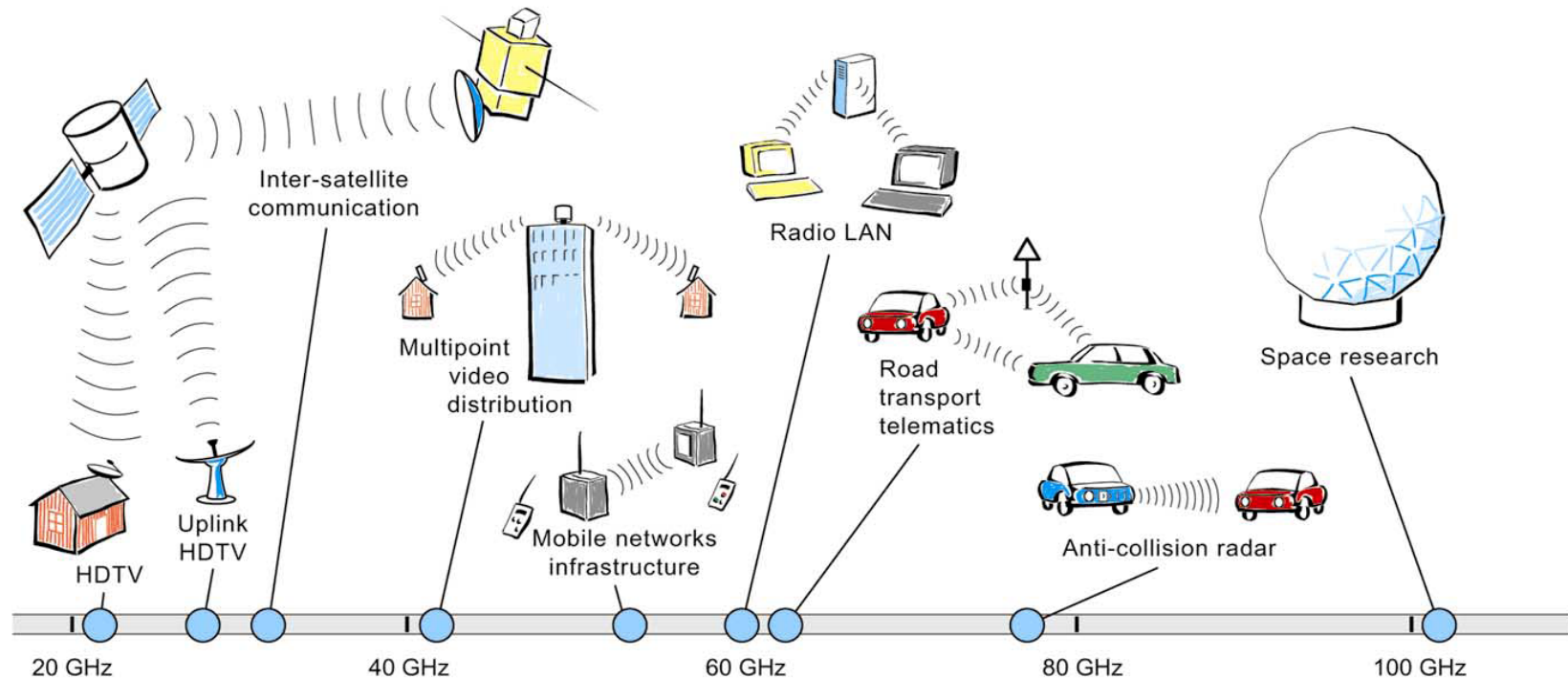
<i>Year of Production</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>	<i>2014</i>	<i>2015</i>
<i>DRAM ½ Pitch (nm) (contacted)</i>	65	57	50	45	40	36	32	28	25
<i>MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)</i>	68	59	52	45	40	36	32	28	25
<i>MPU Physical Gate Length (nm)</i>	25	23	20	18	16	14	13	11	10
<i>Cell area factor [a]</i>	<b>6</b>	<b>6</b>	<b>6</b>	<b>6</b>	<b>6</b>	<b>6</b>	<b>6</b>	<b>6</b>	<b>6</b>
<i>Cell area [<math>Ca = af^2</math>] (<math>\mu\text{m}^2</math>)</i>	<b>0.024</b>	<b>0.019</b>	<b>0.015</b>	<b>0.012</b>	<b>0.0096</b>	<b>0.0077</b>	<b>0.0061</b>	<b>0.0048</b>	<b>0.0038</b>
<i>Cell array area at introduction (% of chip size) §</i>	<b>73.52%</b>	<b>73.76%</b>	<b>73.97%</b>	<b>74.16%</b>	<b>74.30%</b>	<b>74.47%</b>	<b>74.61%</b>	<b>74.70%</b>	<b>74.83%</b>
<i>Generation at introduction §</i>	<b>16G</b>	<b>16G</b>	<b>16G</b>	<b>32G</b>	<b>32G</b>	<b>32G</b>	<b>64G</b>	<b>64G</b>	<b>64G</b>
<i>Functions per chip (Gbits)</i>	<b>17.18</b>	<b>17.18</b>	<b>34.36</b>	<b>34.36</b>	<b>34.36</b>	<b>68.72</b>	<b>68.72</b>	<b>68.72</b>	<b>68.72</b>
<i>Chip size at introduction (<math>\text{mm}^2</math>) §</i>	<b>568</b>	<b>449</b>	<b>711</b>	<b>563</b>	<b>446</b>	<b>706</b>	<b>560</b>	<b>444</b>	<b>351</b>
<i>Gbits/<math>\text{cm}^2</math> at introduction §</i>	<b>3.03</b>	<b>3.82</b>	<b>4.83</b>	<b>6.10</b>	<b>7.70</b>	<b>9.73</b>	<b>12.28</b>	<b>15.49</b>	<b>19.55</b>

# Moore's Law and more



# Application-Specific Integrated Circuits

## Applications >20 GHz in Europe year 2008

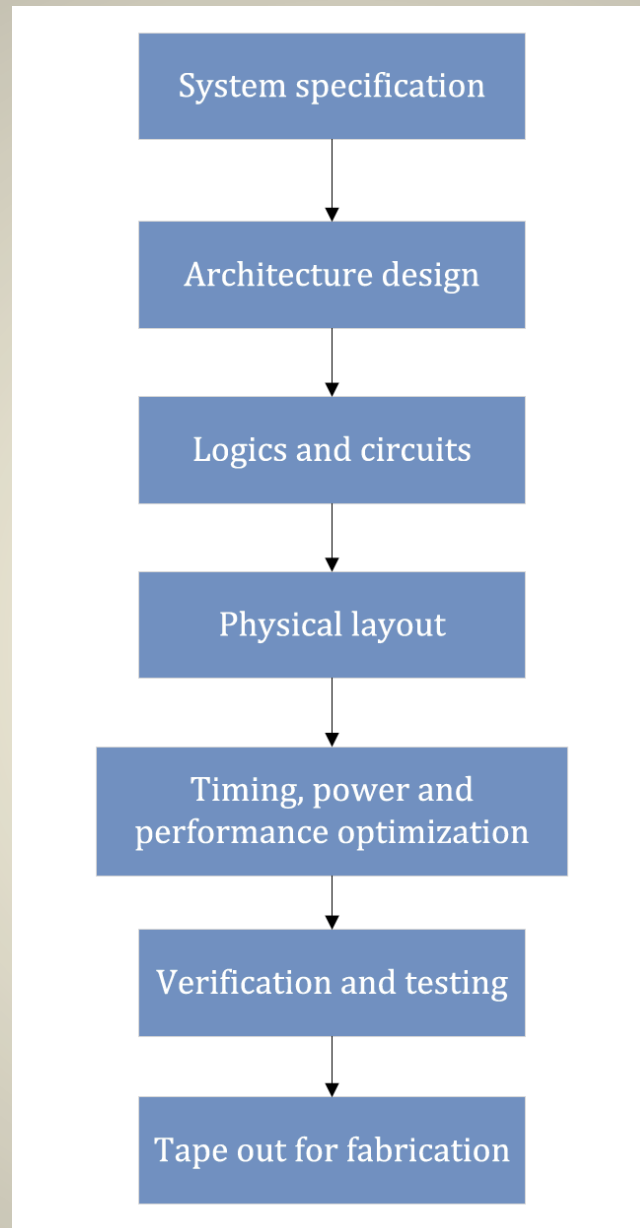


# IC classification

- According to the type of application, development and manufacturing process, and behavioral criteria, ASICs can be classified as:
  - Full-custom ASICs: Some or all of the logic cells, circuits and layouts are specifically designed for an intended application.
  - Semi-custom ASICs: All of the logic cells are pre-designed and required interconnects for specific functions are done by customizing a few mask layers.
  - Non-custom ASICs: All logic cells and interconnecting wire segments are pre-designed. The chip is even packaged before any specific application. Only the switches connecting the wire segments need to be turned on (or off) according to the application logic.

# Design Flow

- Of all aspects of an ASIC project, design flow places the heaviest demand on a design engineer and requires the closest teamwork between the customer and provider.
- Design flow provides the sequence of tasks and the interplay among them.
- The following figure shows a simplified design flow that demonstrates the basic design tasks and the process.

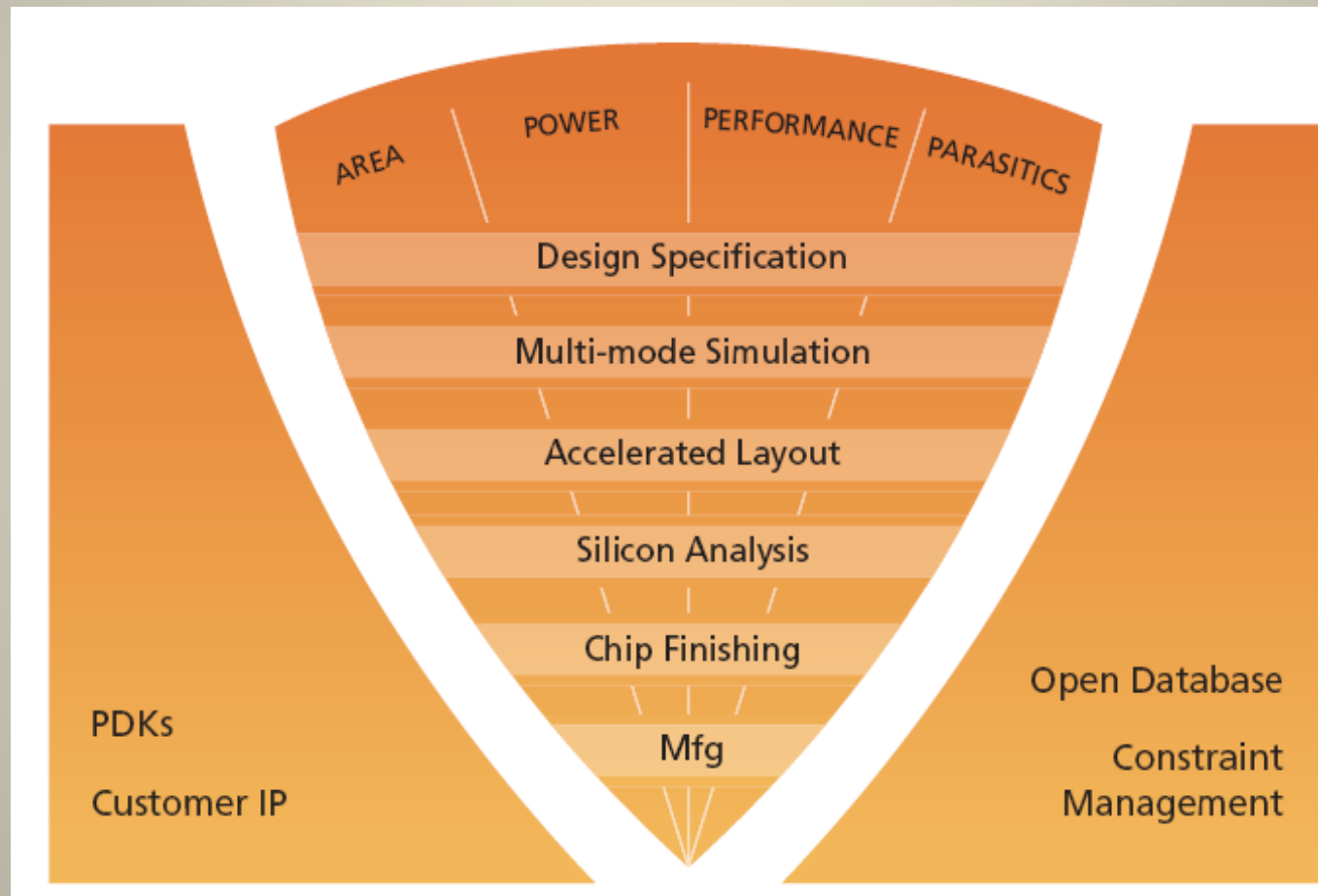


# Computer-Aided-Design (CAD) Tools

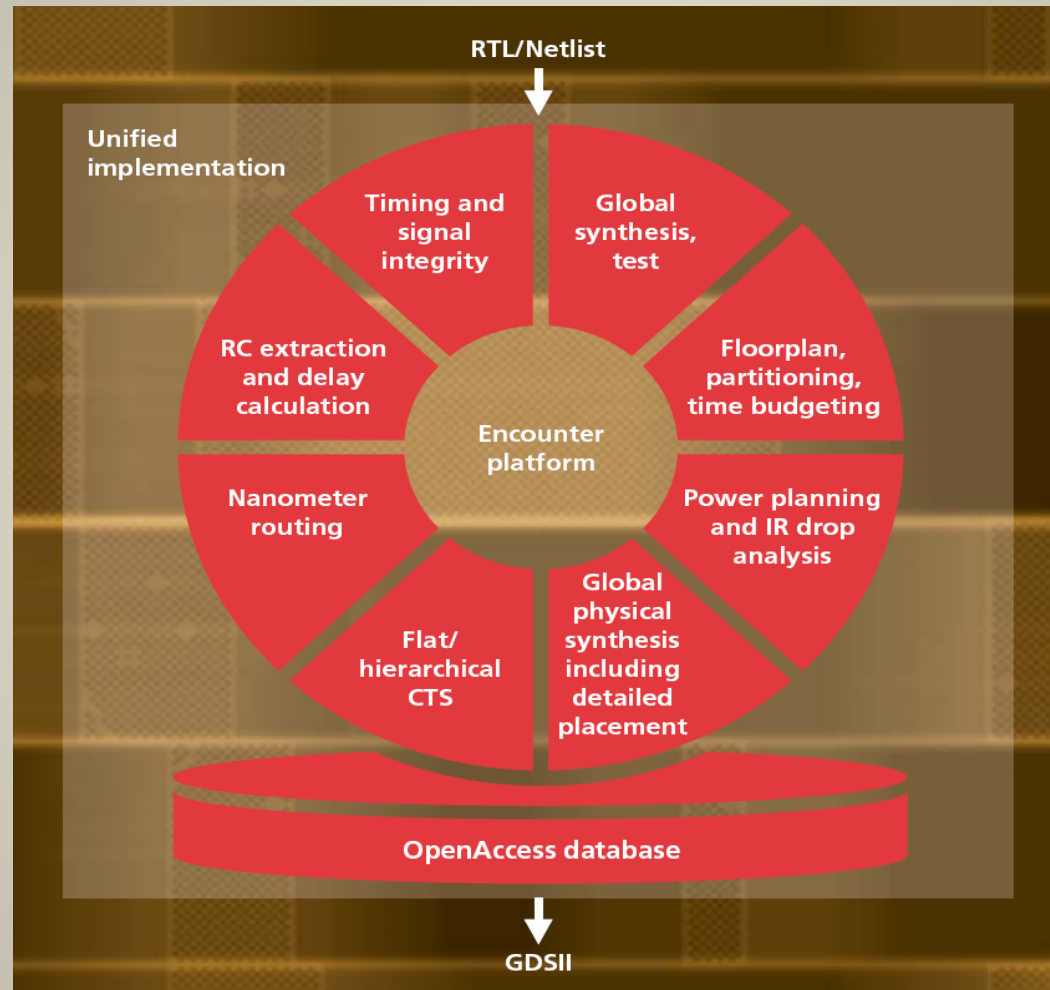
- Computer-aided-design (CAD) uses a wide range of computer-based tools to assist engineers, architects and other design professionals in their design activities.
- CAD is used throughout the engineering process from conceptual design to layout, i.e., through designing methods to the detailed engineering and analysis of components.
- It is impossible today to design design an IC without using CAD tools.

# Cadence Virtuoso Custom Design Platform

- Cadence Virtuoso platform and its functional components

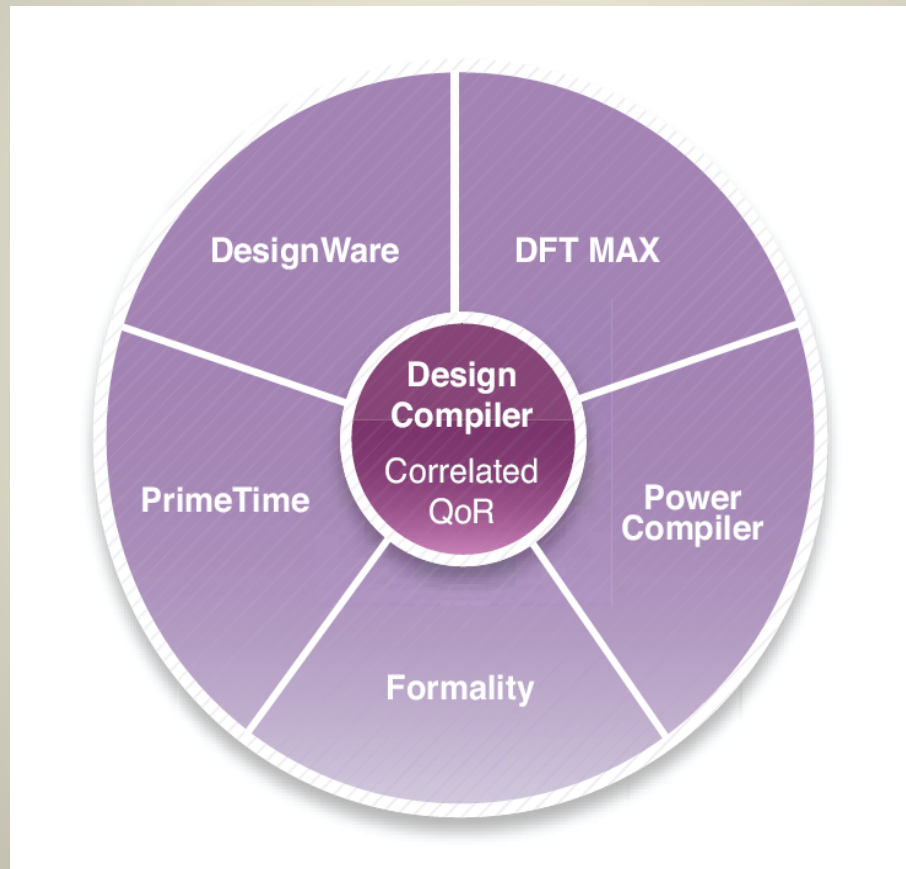


- Cadence Encounter Digital IC Design Platform

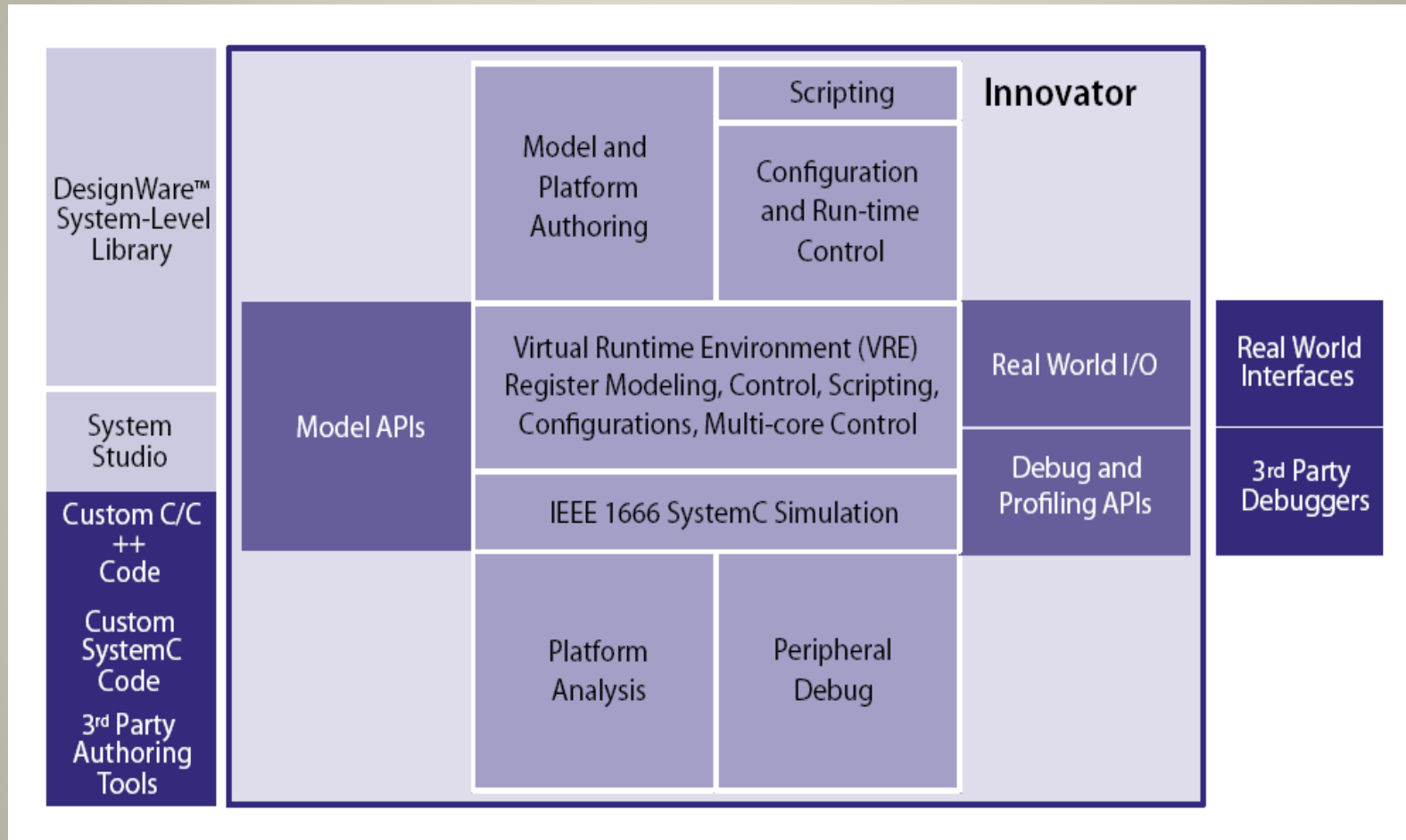


# Synopsys Design Compiler

- The comprehensive synthesis solution



- Synopsys Innovator



# An ASIC Design Project MSDAP

- The best way to learn ASIC design is to design a “real” ASIC chip.
- By going through each task in the entire design flow one not only obtains the knowledge of individual tasks, but also understands the interplay among them.
- Most existing text books/courses mainly focus on the logic functions, circuit components, system control, interface and synthesis method, and treat them as separated subjects.
- The subjects of properly defining system settings and connecting individual design tasks have not received adequate attention.

- This book/class presents a “real” ASIC design project (Mini Stereo Digital Signal Processor: MSDSP) and guides the reader/student through the whole design process (Appendix A).
- The project is to design an ASIC chip which implements an IRF filter used in a hearing-aid device.
  - The device is intended to be disposable, and therefore it needs to be low power and inexpensive at the same time.
- Designers have the opportunity to “understand” a custom specific requirement, which usually posts a challenge for many ASIC designers.

- This project requests the designer to develop a complete specification based on an application about which information is usually “incomplete” from a VLSI design perspective.
- Commonly, most applications are presented with application field terminologies, and terms such as clock rate, supply voltage, and interface protocol are usually not used.
- This ASIC project offers a special value for readers to mimic a relatively real design environment.
- At the end of the semester, students need to complete the design and hand in a project report.

# Required background knowledge

- Knowledge of digital circuit and entry level VLSI design.
- Knowledge of hardware description language VHDL.
- The class focus on the system level design and design flow.
- This class uses
  - Synopsis synthesis tool to automatically transfer the RTL level VHDL design into the logic circuits.
  - Cadence layout tool for the physical design.

# Summery

- In this chapter we have presented the invention of the integrated circuit (IC) and its history.
- As pointed out, the roadmap from ITRS will be a major information source predicting VLSI future development trend.
- Capability of using modern CAD tools is a necessary skill for any digital circuit designer.
- In the following chapter, we shall explore VLSI design perspective and develop its design flow.

# Homework

1. Write a survey of digital IC design CAD tools from major EDA companies.
2. Explain the difference between the digital, analog, and mixed signal circuits. Give an example of each type.
3. What is VHDL and give an example. Explain where a designer uses VHDL?
4. Write a VHDL code of a 2-bit adder in both structure and behavior manner.
5. What are the concerns of after Moore's Law?
6. What is an IP in digital system design?
7. Study the roadmap and identify the trend of digital ICs in the next five years.